10 MHZ TURBO MAINBOARD USER'S MANUAL

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CHAPTER 1 THE SYSTEM BOARD

1-1 Introduction

The 10MHz – TURBO system board fits horizontally in the base of the system unit and is approximately 8½ x 12 inches. It is a double sided P.C.B., DC power and a signal from the power supply enter the board through two six-pin connectors. Other connectors on the board are for attaching the keyborad and speaker. Eight 62-pin card edge-sockets are also mounted on the board. The I/O channel is bussed across these eight I/O slots.

A "Dual-in-Line Package (DIP) switch (SWI) (one eight switch pack) is mounted on the board and can be read under program control. The DIP switch provides the system software with information about the installed options, how much storage the system board has, what type of the display adapter is installed, what operation modes are desired when power is switched on (color or black-and-white, 80- or 40-character lines), and the number of diskette drive attached.

The system board consists of five functional area: the processor subsystem and its support elements, the Read-Only Memory (ROM) subsystem, the Read/Write (R/W) Memory subsystem, integrated I/O adapters, and the I/O channel. All are desired in this section.

The heart of the 10MHZ Turbo system board is the INTEL 8088-1 or qualified 8088-2 microprocessor. This processor is an 8-bit external bus version of INTEL'S 16 bit 8086 processor, and it's softwarecompatible with the 8086. Thus, the 8088 supports 16 bit operations, including multiply and divide, and supports 20 bits addressing (1 megabyte of storage).

It also operates in a maximum mode, so a coprocessor can be added as a feature. The processor operates in two mode, which can be switched, called Normal mode and Turbo mode. When the processor operating at 4.77 MHZ called Normal mode, the frequency, which is derived from a 14.318 MHZ crystal, is devided by 3 for the processor clock, and by 4 to obtain the 3.58 MHZ color burts signal required for color television. When processor operating at 10 MHZ called Turbo mode, the frequency is derived from 30 MHZ.

– DMA –

Three of the four DMA channels are available on the I/O bus and support high speed data transfers between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic memory. This is done by programing a channel of the timer-counter device to periodically request a dummy DMA transfer. This action creates a memory-read cycle, which is available to refresh dynamic storage, both on the system board and in the system expansion slots. All DMA data transfers, except the refresh channel, take five processor clocks of 210 ns, or 1.05, μs if the processor ready line is not deactivated. Refresh DMA cycles take four clocks or 840 ns.

– TIMER –

The three programmable timer/counters are used by the system as follows: Channel o is used as a general purpose timer, providing a constant time base for implementing a time-of-day clock; Channel 1 is used to time and request refresh cycles from the DMA channel; and Channel 2 is used to support the tone generation for the audio speaker. Each channel has a minimum timing resolution of 1.05 μs.

– INTERRUPT –

Of the eight prioritized levels of interrupt, six are bussed to the system expansion slots for use by features cards. Two levels are used on the system board. Level 0, the highest priority, is attached to Channel 0 of the timer/counter and provides a periodic interrupt for the time-of-day clock. Level 1 is attached to the keyboard adapter circuits and receives an interrupt for each scan code sent by the keyboard. The Non-Maskable Interrupt (NMI) of the 8088 is used to report memory parity errors.

– MEMORY –

The system board supports both ROM/EPROM and R/W memory. it has space for 32k x 1 & 8k x 1 of ROM or EPROM. this ROM contains the power-on self-test, I/O drivers, dot patterns for 128 characters in graphics mode, and a diskette.

The system board also has from 256k to 640k of R/W memory. A minimum system would have 256k of memory.

– KEYBOARD –

The system board contains the adapter circuits for attaching the serial interface from the keyboard. These circuits generate an interrupt on to the processor, when a complete scan code is received. The interface can request execution of a diagnostic test in the keyboard.

The keyboard interface is a 5-pin DIN connector on the system board, that extends through the rear panel of the system unit.

– SPEAKER –

The system units has an 2¼ inch audio speaker. The speaker's control circuits and driver are on the system board. The speaker connects through a 2-wire interface that attaches to a 3-pin connector on the system board.

The speaker drive circuit could be capable of providing approximately ½ watt of power. The control circuits allow the speaker to be driven three different ways: 1) a direct program control register bit may be toggled, to generate a pulse train; 2) the output from Channel 2 of the timer counter, may be programed to generate a wavefrom to the speaker; 3) the clock input to the timer counter, can be modulated with a program controlled I/O register bit. All three methods may be performed simultaneously.

1-2 Expansion I/O Channel

The I/O channel is an extension of the 8088 microprocessor bus. It is, however, demultiplexed, repowered, and enhanced by the addition of interrupts and Direct Memory Access (DMA) functions.

The I/O channel contains an 8 bit, bidirectional data bus, 20 address lines, 6 levels of interrupt, control lines for memory and I/O read or write, clock and timing lines, 3 channels of DMA control lines, memory refresh timing control lines, a channel check line, and power and ground for the adapters. Four voltage levels are provided for I/O card: +5Vdc, –5Vdc, +12 Vdc, and –12dc. These functions are provided in a 62-pin connector with 100-mil card tab spacing.

A "ready" lines is available on the I/O channel, to allow operation with slow I/O or memory devices. If the channel's ready line is not activated by an addressed device, all processor-generated memory read and write cycles takes four 210-ns clock or 840-ns/byte. All processor-generated I/O read and write cycles require five clocks for a cycle time of 1.05 µs/byte. Refresh cycles occur once every 72 clocks (approximately 15 µs) and require four clocks or approximately 7% ofthe bus bandwidth.

I/O devices are addressed using I/O mapped address space. The channel is designed so that 768 I/O device addressed are available to the I/O channel cards.

A channel check line exists for reporting error conditions to the processor Activating this line results in a Non-Maskable Interrupt (NMI) to the 8088 processor. Memory expansion options use this line to report parity errors.

The I/O channel is repowered, to provide sufficient drive, to power all eight (J1 through J8) expansion slots, assuming two Low-Power Schorttky (LS) loads per slot. The I/O adapters typically use only one load.

1-3 I/O Channel Description

The following is a description of the PC/XT I/O Channel. All lines are TTL-compatible.

Singal I/O Description

OSC, Oscillator:

High; speed clock with a 70-ns period (14.31818 MHz). It has a 50% duty cycle.

CLK, System Clock:

It is divide-by-three of the oscillator and has a period of 210 ns (4.77 MHz). The clock has a 33% duty cycle.

RESET:

This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.

AO-A19, Address Bits 0 to 19:

These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. AO is the Least Significant Bit (LSB) and A19 is the Most Significant Bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.

DO-D7, I/O Data Bits 0 to 7:

These lines provide data bus bits 0 to 7 for the processor,

memory, and I/O devices. DO is the Least Significant Bit (LSB) and D7 is the Most Significant Bit (MSB). These lines are active high.

ALE, Address Latch Enable:

This line is provided by the 8288 Bus Controller and is used on the system board to latch valid addresses from the processor. It is available to the I/O channel as an indicator of a vilid processor address (when used with AEN). Processor addresses are latched with the failing edge of ALE.

I/O CH CK, I/O Channel Check:

This line provides the processor with parity (error) information on memory or devices in the I/O channel. When this signal is active low, a parity error would indicated.

I/O CH RDY, I/O Channel Ready:

This line, normally high (ready), can be pulled low (not ready; by a memory or I/O device to lengthen I/O or memory cycles. It allows slower devices to attach to the I/O channel with a minimum of difficulty. Any slow device using this line should drive it low immediately upon detecting a valid address and a read or write command. This lines should never be held low, longer than 10 clock cycles. Machine cycles (I/O or memory) are extended by an integral number of CLK cycles.

IRQ2-1RQ7, Interrupt Request 2 to 7:

These lines are used to signal the processor, that a I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An Interrupt Request are gener-

ated by raising an IRQ line (low to high) and holding it high, until it was acknowledged by the processor (interrupt service routine).

IOR, I/O Read Command:

This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

IOW, I/O Write Command:

This command line instructs an I/O device, to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMR, Memory Read Command:

This command line instructs the memory to drive its data into the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

MEMW, Memory Write Command:

This command line instructs the memory to store the data present on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.

DRQ1-DRQ3, DMA Request 1 to 3:

These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (high). A DRQ line must be held high until the corresponding DACK

line goes active.

DACKO – 3 – DAM Acknowledge 0 to 3:

These lines are DACK3 used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACKO). They are active low.

AEN, Address Enable:

This line is used to degate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).

T/C, Terminal Count:

This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

CARD SLCTD, Card Selected:

This line is activated by cards in expansion slot J8. It signals, "THE SYSTEM BOARD", that the card has been selected and that appropriate drivers on the system board should be directed to either read from, or write to, expansion slot J8. Connectors J1 through J8 are tied together at this pin, but the system board should be driven by an open collector device.

The following voltages are available on the system board I/O channel:

+5 Vdc + – 5%, located on 2 connector pins
–5 Vdc + –10%, located on 1 connector pin
+ 12 Vdc + – 5%, located on 1 connector pin
– 12 Vdc + –10%, located on 1 connector pin
GND (Ground), located on 3 connector pins

1-4 Speaker Interface

The sound system has a small, permanent-magnet, 2¼ inch speaker. The speaker can be driven from one or two sources:

* An 8255A-5 PPI output bit. The address and bit are defined in the "I/O Address Map"

* A timer clock channel, the output of which is programmable within the founctions of the 8253-5 timer when using a 1.19-MHz clock input. The timer gate also is controlled by an 8255A-5 PPI output-port bit. Address and bit assignment are in the "I/O Address Map".

The speaker connection is a 4-pin berg connector, See "System Board Component Diagram", earlier in this section, for speaker connection or placement.

CHAPTER 2
THE NORMAL/TURBO MODE OPERATION

2-1 ADVENTAGES OF THE 10MHZ TURBO

The difference between PIM-TB10 and other PC/XT main boards is the PIM-TB10 main board allows an increase at about 90% in speed of program execution. As the 8088-1 or qualified 8088-2 processor operates at a quicker speed at 10 MHZ. In other PC/XT main board, the clock speed is only 4.77 MHZ. Of course, it is faster than 8MHZ Turbo, too.

The PIM-TB10 consists of dual clock system, in Normal mode, the clock speed is only 4.77MHZ cycle. In Turbo mode, the clock speed increases to 10 MHZ cycle.

Note No. 1: Please do not make use of RAM memory on interface card. Because its original design may be not compatible with 10 MHZ high speed CPU at access time. *Please use memory on mainboard and use 4164 and 41256 & 4464 access time within 150 ns.

For Example:

	4164	41256	4464
NEC	D4164C	D41256C	D4464C
HITACHI	HM4846	HM50256	HM50464
MITSUBISHI	MSK4164	MSM4256P	MH6404AND1
PANASONIC	MN4164	MN41256	MN4464

Note No. 2: Use NEC 70108-10 to enable speed up to 340% faster than normal XT

2-2 To Obtain Turbo Mode at 10 MHZ

The system board suports both software switch as well as hardware switch to allow transaction from Normal mode (4.77 MHZ) to Turbo mode (10 MHZ) and software switch, hardware switch can be used at the same time to select each of them by jumper is not necessary.

A) Software Switch:

Software switch is available when using "ERSO/DTK TURBO" BIOS only.

1) Turn on Turbo Mode:

Press and hold down the "CTRL" (CONTROL) and "ALT" (ALTERNATIVE) Keys and then press the "–" (MINUS) key then the cursor on screen display will appres as a'BOX' Now, you are ready to use Turbo mode and the Turbo LED is on.

2) Press and hold down "CTRL" (CONTROL) and "ALT" (ALTERNATE) keys and then press the "–" (MINUS) key to come back to Normal mode at 4.77 MHZ. You will see on screen display that the cursor shows up as a "–" (DASH) and the Turbo LED is off.

* ERSO/DTK BIOS is registered copyright under ERSO.
* ERSO: short form from "Electronics Research & Service Organization"

B) Hardware Switch:

1) Jumper Setting

a) Turn on Turbo Mode

Push the Turbo switch into "ON" position to turn on Turbo mode at 10 MHZ and the Turbo LED is on to indicate system being in Turbo Mode now.

b) Return to Normal Mode:

Push the Turbo switch into "OFF" position to come back to Normal mode at 4.77 MHZ and the Turbo LED is off.

Note : 1. The Push button leads to JP6 on main-board. When the botton is pushed in, JP6 i shorted.

2. If you use software switch and hardware switch at the same time, which means you use these two change methods exchange-able, the cursor on the screen display does not indicate the exact execution mode any more.

   Because cursor does not change by hard-ware switch, you mix these two changes methods, then the cursor is confused. At this time, the Turbo LED is the only way that you can distinguish normal and Turbo mode.

3. 10MHZ Turbo board can run Lotus 1-2-3, CP/M 86, DBASE III and many other famous IBM package programs. Please use Normal mode (4.77 MHZ) when running Copy Write.

CHAPTER 3
CONNECTORS AND SWITCH SETTING

3-1 Connectors

The system board has the following connectors:

Two power-supply connectos (P1 and P2)

- Speaker connector (JP1)
- Keyboard connector (JP2)
- Keylock connector (JP3)
- Reset connector (JP4)
- Power LED and Turbo LED connector (JP5)

A) Power Supply Connectors (P1 and P2)

Pin	Assignments	Connector
1	Power good	P1
2	Not used	
3	+ 12 Vdc	
4	– 12 Vdc	
5	Ground	
6	Ground	
1	Ground	P2
2	Ground	
3	– 5 Vdc	
4	+ 5 Vdc	
5	+ 5 Vdc	
6	+ 5 Vdc	

B) Speaker Connector (JP1)

The speaker connector is a 2-pin, keyed, 90 degree. The pin assignments as following:

Pin	Function
1	Data out
2	+ 5 Vec

C) Keyboard Connector (JP2)

The keyboard connector is a 5-pin, 90-degree Printed Circuit Board (PCB) mounting, DIN connector. The pin assignments as following:

Pin	Assignments
1	Keyboard clock
2	Keyboard data
3	Keyboard reset
4	Ground
5	+ 5 Vdc

D) Keylock Connector (JP3)

The keylock connector is a 2-pin, keyed, berg strip. When this connector (JP3) is open, keyboard is locked. When this connector (JP3) is shortted, keyboard is unlocked.

E) Reset Connector (JP4)

The reset connector is a 2-pin, keyed, berg strip. When this connector (JP4) is open, system is in regular operation. When this connector (JP4) is shortted for a while, system restarts.

F) Power LED and Turbo LED Connector (JP5)

The power LED and LED connector is a 4-pin Berg strip Its pin assignments as following:

Pin	Assignments
1	Turbo LED (1)
2	Turbo LED (2)
3	Power LED
4	Ground

pin 1 & pin 2 to turbo LED pin 3 & pin 4 to power LED.

3-2 THE SYSTEM BOARD SWITCH SETTING

The DIP Switch (SW1) is used to set the system configuration and specify the amount of memory installed on the system board. Generally the memory switch is useless now.

Position	Function
1	Normal operation off
2	Use for 8087-2 co-processor
3-4	Amount of memory on system board
5-6	Type of display adapter
7-8	Number of 5¼ inch diskette drives

Switch (SW1):

1 = OFF	(NORMAL OPERATION)
2 = ON	W/O 8087-2 co-processor
3 = OFF	W/ 8087-2 co-processor

Memory Switch Settings:

3 = OFF	4 = ON	128K MEMORY INSTALLED
3 = ON	4 = OFF	192K MEMORY INSTALLED
3 = OFF	4 = OFF	256K MEMORY INSTALLED

Display Adapter Switch Settings:

5 = ON	6 = ON	NO DISPLAY ADAPTER
5 = OFF	6 = ON	COLOR/GRAPHICS (40x20 Mode)
5 = ON	6 = OFF	COLOR/GRAPHICS (80x25 Mode)
5 = OFF	6 = OFF	MONOCHROME DISPLAY ADAPTER OR BOTH

Display Dirve Switch Setting:

7 = ON	8 = ON	1 DRIVE INSTALLED
7 = OFF	8 = ON	2 DRIVES INSTALLED
7 = ON	8 = OFF	3 DRIVES INSTALLED
7 = OFF	8 = OFF	4 DRIVES INSTALLED

4-2 ROM CHIPS INSTALLATION

The 10MHZ Turbo Mainboard provides 2 ROM chips space for system.

U38 must be installed 2764 for ROM BIOS.

U49 must be installed 27256 for ROM BASIC.

CHAPTER 4
MEMORY RAM/ROM CHIPS INSTALLATION

4-1 RAM Chips Installation

The 10MHZ Turbo mianboard provides 4 banks of memory

BANK 0 is made up of 9 pieces of 41256 ir U90 through U57.

BANK 1 is made up of 9 pieces of 41256 in U89 through U56.

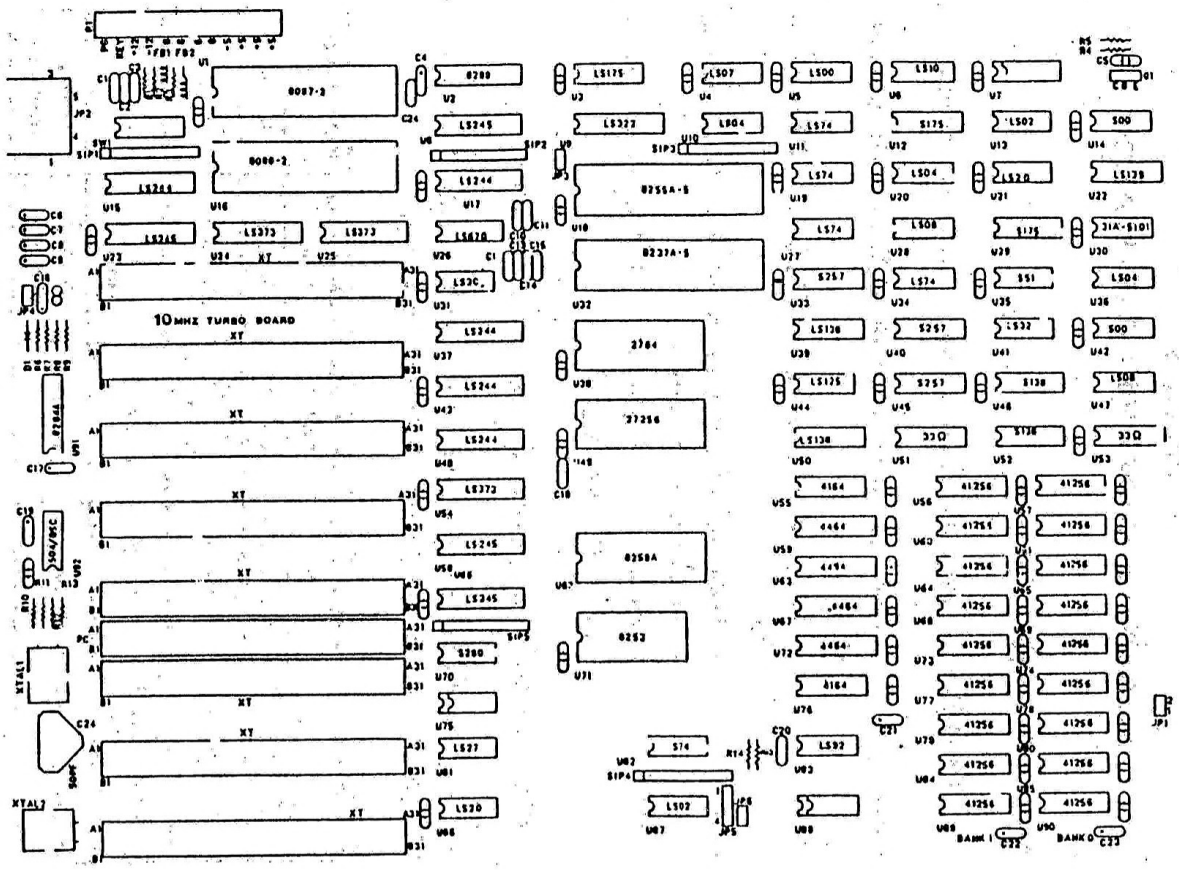
BANK 2 is made up of 2 pieces of 4464 in U63, U59 & 1 piece of 4164 in U55.

BANK 3 is made up of 2 pieces of 4464 in U72, U67 & 1 piece of 4164 in U76.

* 4164 in BANK 2 and BANK 3 is used for parity checking.

4 potions of memory configuration can be installed on board. Follow the instructions below for proper installation:

Option	RAM chips on Bank ϕ	RAM chips on Bank 1	RAM chips on Bank 2	RAM chips on Bank 3
256K RAM	41256 x9	No chip	No chip	No chip
512k RAM	41256x9	41256x9 No chip	No chip	No chip
576K RAM	41256x9	41256x9	4464x2 +4164x1	No chip
640K RAM	41256x9	41256x9	4464x2 +4164x1	4464x2 +4164x1


10MHZ TURBO BOARD
XT
PC
8087-2
8088-2
8255A-5
8237A-5
2764
27256
8259A
8253
41256
BANK 1
BANK 0