128MByte (16M x 72) DRAM Module - 16Mx4 based
168-pin DIMM, Buffered, ECC

Features

- Standard : JEDEC
- Configuration : ECC
- Access Time : 50/60/70ns
- Operation Mode : FPM/EDO
- Operating Voltage : 3.3/5.0V
- Refresh : 4K/8K
- Device Physicals : 400mil SOJ/TSOP
- Lead Finish : Gold
- Length x Height : 5.250" x 1.250"
- No. of sides : Double-sided
- Mating Connector (Examples)
  Vertical : AMP-390052-1 (5.0V)/390052-4 (3.3V)

Part Numbers

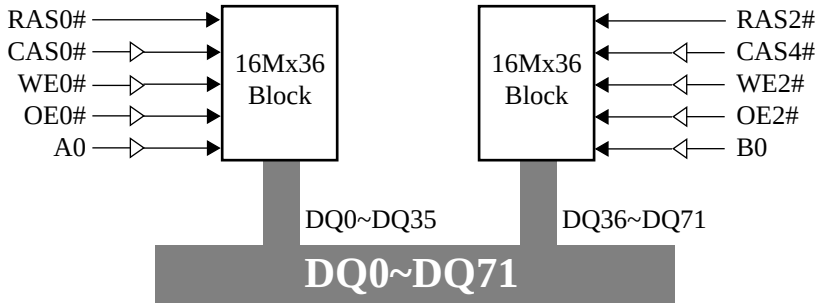
SM57216400UEUGU	:	FPM, 5.0V
SM57216401UEUGU	:	FPM, 3.3V
SM57216408UEUGU	:	EDO, 5.0V
SM57216409UEUGU	:	EDO, 3.3V

Note: Refer last page for all "U" options.

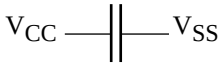
Related Products :

SM5721680UUEUGU	:	16Mx72, 8Mx8 based.

Functional Diagram



Notes : 1. A0~A11/A12 are connected to all DRAMs through buffers (A12 is NC for 4K refresh module).
2. All signals including PDs (with exception of RAS#, Data and IDs) are buffered.
3. Each 16x36 Block comprises of nine 16Mx4 DRAMs.



Decoupling capacitors to all devices.

(All specifications of this device are subject to change without notice.)

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Pin Name

A0, B0~A11	Row and Column Addresses for 4K Refresh Module	WE0#, WE2#	Write Enable Inputs
A0, B0~A12	Row Addresses for 8K Refresh Module	PDE#	PD Enable Input
A0, B0~A10	Column Addresses for 8K Refresh Module	PD1~PD8	Presence Detect Inputs
DQ0~DQ71	Data Inputs/Outputs	ID0, ID1	ID Inputs
RAS0#, RAS2#	Row Address Strobe Inputs	V_{CC}	Power Supply
CAS0#, CAS4#	Column Address Strobe Inputs	V_{SS}	Ground
OE0#, OE2#	Output Enable Inputs	NC	No Connection

Presence Detect Pins

Mode

Pin	FPM	EDO
PD5	V_{OL} †	NC

Access Time

Pin	50ns	60ns	70ns
PD6	V_{OL} †	NC	V_{OL} †
PD7	V_{OL} †	NC	NC

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	OE2# †	86	DQ36	128	NC
3	DQ1	45	RAS2#	87	DQ37	129	NC
4	DQ2	46	CAS4# †	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	V_{CC}	48	WE2# †	90	V_{CC}	132	PDE#
7	DQ4	49	V_{CC}	91	DQ40	133	V_{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V_{CC}	101	DQ49	143	V_{CC}
18	V_{CC}	60	DQ24	102	V_{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	V_{SS}	65	DQ25	107	V_{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	WE0# †	69	DQ28	111	NC	153	DQ64
28	CAS0# †	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	RAS0#	72	DQ31	114	NC	156	DQ67
31	OE0# †	73	V_{CC}	115	NC	157	V_{CC}
32	V_{SS}	74	DQ32	116	V_{SS}	158	DQ68
33	A0 †	75	DQ33	117	A1 †	159	DQ69
34	A2 †	76	DQ34	118	A3 †	160	DQ70
35	A4 †	77	DQ35	119	A5 †	161	DQ71
36	A6 †	78	V_{SS}	120	A7 †	162	V_{SS}
37	A8 †	79	PD1 (NC)	121	A9 †	163	PD2 (NC)
38	A10 †	80	PD3 (NC)	122	A11 †	164	PD4 (NC)
39	A12 (Note) †	81	PD5	123	NC	165	PD6
40	V_{CC}	82	PD7	124	V_{CC}	166	PD8 (V_{OL}) †
41	NC	83	ID0 (V_{SS})	125	NC	167	ID1 (V_{SS})
42	NC	84	V_{CC}	126	B0 †	168	V_{CC}

Notes : 1. Signals marked with "†" are buffered. 2. A12 is NC for 4K refresh module

DC Characteristics

FPM & EDO-based Modules

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		Vcc=3.3V	Vcc=5.0V	
Voltage on any pin relative to V_{SS}	V_T	- 0.5 to +4.6	- 1.0 to +7.0	V
Power Dissipation	P_T	20	20	W
Operating Temperature	T_{opr}	0 to +70	0 to +70	°C
Storage Temperature	T_{stg}	- 55 to +150	- 55 to +150	°C
Short Circuit Output Current	I_{OS}	50	50	mA

Recommended DC Operating Conditions

(T_A = 0 to +70°C)

Parameter	Symbol	Vcc=3.3V			Vcc=5.0V			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{CC}	3.0	3.3	3.6	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	2.4	-	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	-1.0	-	0.8	V

Capacitance

(V_{CC} = 3.3V±10%/5.0V±10%, T_A = +25°C)

Parameter	Symbol	Max	Unit
Input Capacitance (Address, CAS#, WE#, OE#)	C_{I1}	17	pF
Input Capacitance (RAS#)	C_{I2}	73	pF
Input/Output Capacitance (DQ0~DQ71)	$C_{I/O}$	17	pF

Notes : Capacitance is sampled per Mil-Std-883.

DC Characteristics (cont'd)

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	50ns		60ns		70ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.3V$	-90	90	-90	90	-90	90	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 2mA	-	0.4	-	0.4	-	0.4	V

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	50ns		60ns		70ns		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{CC}+0.5V$	-90	90	-90	90	-90	90	µA
Output Leakage Current	I_{LO}	$0V \le V_{out} \le V_{CC}$ D_{out} = Disable	-10	10	-10	10	-10	10	µA
Output High Voltage	V_{OH}	High I_{out} = -5mA	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	Low I_{out} = 4.2mA	-	0.4	-	0.4	-	0.4	V

DC Characteristics (cont'd)

FPM-based Modules

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 50ns	Max. 60ns	Max. 70ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	4K	2710	2530	2350	mA	1, 2
		t_{RC} = min.	8K	1810	1630	1450	mA	1, 2
Standby Current	I_{CC2}	LVTTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		46	46	46	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		28	28	28	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=VIH; RAS#, Address cycling @ t_{RC}=min.	4K	2710	2530	2350	mA	2
			8K	1810	1630	1450	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	4K	2710	2530	2350	mA	
			8K	2710	2530	2350	mA	
Fast Page Mode Current	I_{CC5}	RAS#=VIL, CAS#, Address cycling @ t_{PC}=min.	4K	1450	1270	1180	mA	1, 3
			8K	1270	1090	1000	mA	1, 3

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 50ns	Max. 60ns	Max. 70ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	4K	2764	2584	2404	mA	1, 2
		t_{RC} = min.	8K	1864	1684	1504	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		100	100	100	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		82	82	82	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	4K	2764	2584	2404	mA	2
			8K	1864	1684	1504	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	4K	2764	2584	2404	mA	
			8K	2764	2584	2404	mA	
Fast Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{PC}=min.	4K	1504	1324	1234	mA	1, 3
			8K	1324	1144	1234	mA	1, 3

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS# = V_{IL} .
3. Address can be changed once or less while CAS# = V_{IH} .

DC Characteristics (cont'd)

EDO-based Modules

(V_{CC} = 3.3V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 50ns	Max. 60ns	Max. 70ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	4K	2710	2530	2350	mA	1, 2
		t_{RC} = min.	8K	1810	1630	1450	mA	1, 2
Standby Current	I_{CC2}	LVTTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		46	46	46	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		28	28	28	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	4K	2710	2530	2350	mA	2
			8K	1810	1630	1450	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	4K	2710	2530	2350	mA	
			8K	2710	2530	2350	mA	
Hyper Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{HPC}=min.	4K	2170	1990	1810	mA	1, 3
			8K	1990	1810	1630	mA	1, 3

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Conditions	Refresh	Max. 50ns	Max. 60ns	Max. 70ns	Unit	Note
Operating Current	I_{CC1}	RAS#, CAS# cycling;	4K	2764	2584	2404	mA	1, 2
		t_{RC} = min.	8K	1864	1684	1504	mA	1, 2
Standby Current	I_{CC2}	TTL Interface RAS#, CAS# ≥ V_{IH} D_{out} = High-Z		100	100	100	mA	
		CMOS Interface RAS#, CAS# ≥ V_{CC} - 0.2V D_{out} = High-Z		82	82	82	mA	
RAS#-only Refresh Current	I_{CC3}	CAS#=V_{IH}; RAS#, Address cycling @ t_{RC}=min.	4K	2764	2584	2404	mA	2
			8K	1864	1684	1504	mA	2
CAS#-before-RAS# Refresh Current	I_{CC4}	RAS#, CAS# cycling @ t_{RC}=min.	4K	2764	2584	2404	mA	
			8K	2764	2584	2404	mA	
Hyper Page Mode Current	I_{CC5}	RAS#=V_{IL}, CAS#, Address cycling @ t_{HPC}=min.	4K	2244	2044	1864	mA	1, 3
			8K	2044	1864	1684	mA	1, 3

Notes: 1. Values depend on output load condition when the device is selected. Maximum values are specified at the output open condition.
2. Address can be changed once or less while RAS# = V_{IL} .
3. Address can be changed once or less while CAS# = V_{IH} .

AC Characteristics

FPM-based Modules

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Common to Read and Write Cycles									
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Row address set-up time	t_{ASR}	5	-	5	-	5	-	ns	
Column address hold time	t_{CAH}	10	-	10	-	15	-	ns	
CAS# pulse width	t_{CAS}	13	10000	15	10000	20	10000	ns	
CAS# to output in Low-Z	t_{CLZ}	5	-	5	-	5	-	ns	3
CAS# to RAS# precharge time	t_{CRP}	10	-	10	-	10	-	ns	
CAS# hold time	t_{CSH}	49	-	59	-	69	-	ns	
RAS# to column address delay time	t_{RAD}	14	20	14	25	14	30	ns	10
Row address hold time	t_{RAH}	9	-	9	-	9	-	ns	
RAS# pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
Random read/write cycle time	t_{RC}	90	-	110	-	130	-	ns	
RAS# to CAS# delay time	t_{RCD}	19	32	19	40	19	45	ns	4
RAS# precharge time	t_{RP}	30	-	40	-	50	-	ns	
RAS# hold time	t_{RSH}	18	-	20	-	25	-	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
Read Cycle									
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Access time from CAS#	t_{CAC}	-	18	-	20	-	25	ns	3, 4, 5
Output buffer turn-off delay	t_{OEA}	-	18	-	20	-	25	ns	
Output buffer turn-off delay	t_{OEZ}	1	18	1	20	1	25	ns	
Output buffer turn-off delay	t_{OFF}	1	18	1	20	1	25	ns	6
Access time from RAS#	t_{RAC}	-	50	-	60	-	70	ns	3, 4
Column address to RAS# lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command hold time referenced to CAS#	t_{RCH}	0	-	0	-	0	-	ns	8
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Read command hold time referenced to RAS#	t_{RRH}	-1	-	-1	-	-1	-	ns	8
Write Cycle									
Write command to CAS# lead time	t_{CWL}	13	-	15	-	20	-	ns	
Data-in hold time	t_{DH}	15	-	15	-	20	-	ns	9
Data-in set-up time	t_{DS}	-1	-	-1	-	-1	-	ns	9
Write command to RAS# lead time	t_{RWL}	20	-	20	-	25	-	ns	
Write command hold time	t_{WCH}	10	-	10	-	15	-	ns	

AC Characteristics (cont'd)

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
Write command pulse width	t_{WP}	10	-	10	-	15	-	ns	
Fast page Mode Cycle									
Access time from CAS# precharge	t_{ACP}	-	35	-	40	-	45	ns	3, 11
CAS# precharge time	t_{CP}	10	-	10	-	10	-	ns	
Fast page mode cycle time	t_{PC}	30	-	40	-	45	-	ns	
RAS# pulse width	t_{RASP}	50	200000	60	200000	70	200000	ns	12
RAS# hold time from CAS# precharge	t_{RHCP}	35	-	40	-	45	-	ns	
Refresh Cycle									
CAS# hold time (CBR refresh)	t_{CHR}	9	-	9	-	14	-	ns	1
CAS# set-up time (CBR refresh)	t_{CSR}	15	-	15	-	15	-	ns	1
Refresh period	t_{REF}								
4K refresh		-	64	-	64	-	64	ms	
8K refresh		-	64	-	64	-	64	ms	
RAS# precharge to CAS# hold time	t_{RPC}	4	-	4	-	4	-	ns	

EDO-based Modules

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Common to Read and Write Cycles									
Column address set-up time	t_{ASC}	0	-	0	-	0	-	ns	
Row address set-up time	t_{ASR}	5	-	5	-	5	-	ns	
Column address hold time	t_{CAH}	8	-	10	-	15	-	ns	
CAS# pulse width	t_{CAS}	13	10000	15	10000	20	10000	ns	
CAS# to output in Low-Z	t_{CLZ}	8	-	8	-	8	-	ns	3
CAS# to RAS# precharge time	t_{CRP}	10	-	10	-	10	-	ns	
CAS# hold time	t_{CSH}	37	-	44	-	49	-	ns	
RAS# to column address delay time	t_{RAD}	14	20	14	25	14	30	ns	10
Row address hold time	t_{RAH}	9	-	9	-	9	-	ns	
RAS# pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
Random read/write cycle time	t_{RC}	84	-	104	-	124	-	ns	
RAS# to CAS# delay time	t_{RCD}	19	32	19	40	19	50	ns	4
RAS# precharge time	t_{RP}	30	-	40	-	50	-	ns	
RAS# hold time	t_{RSH}	18	-	20	-	25	-	ns	
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	2

AC Characteristics (cont'd)

(V_{CC} = 3.3V±10%/5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	50ns		60ns		70ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle									
Access time from column address	t_{AA}	-	30	-	35	-	40	ns	3, 10
Access time from CAS#	t_{CAC}	-	18	-	20	-	25	ns	3, 4, 5
Output buffer turn-off time to CAS#	t_{CEZ}	4	18	4	18	4	20	ns	6
CAS# hold time to OE#	t_{CHO}	5	-	5	-	5	-	ns	
OE# to CAS# hold time	t_{OCH}	5	-	5	-	5	-	ns	
OE# access time	t_{OEA}	-	18	-	20	-	25	ns	
OE# precharge time	t_{OEP}	5	-	5	-	5	-	ns	
Output buffer turn off delay time from OE#	t_{OEZ}	4	18	4	18	4	20	ns	
Access time from RAS#	t_{RAC}	-	50	-	60	-	70	ns	3, 4
Column address to RAS# lead time	t_{RAL}	30	-	35	-	40	-	ns	
Read command hold time referenced to CAS#	t_{RCH}	0	-	0	-	0	-	ns	8
Read command set-up time	t_{RCS}	0	-	0	-	0	-	ns	
Output buffer turn-off delay to RAS#	t_{REZ}	3	13	3	15	3	20	ns	
Read command hold time referenced to RAS#	t_{RRH}	-1	-	-1	-	-1	-	ns	8
Write Cycle									
Write command to CAS# lead time	t_{CWL}	13	-	15	-	20	-	ns	
Data-in hold time	t_{DH}	13	-	15	-	20	-	ns	9
Data-in set-up time	t_{DS}	-1	-	-1	-	-1	-	ns	9
Write command to RAS# lead time	t_{RWL}	18	-	20	-	25	-	ns	
Write command hold time	t_{WCH}	10	-	10	-	15	-	ns	
Write command set-up time	t_{WCS}	0	-	0	-	0	-	ns	7
Write command pulse width	t_{WP}	10	-	15	-	15	-	ns	
Hyper Page Mode Cycle									
Access time from CAS# precharge	t_{ACP}	-	33	-	40	-	45	ns	3, 11
CAS# precharge time	t_{CP}	8	-	10	-	10	-	ns	
Hyper page mode cycle time	t_{HPC}	20	-	25	-	30	-	ns	
RAS# pulse width	t_{RASP}	50	200000	60	200000	70	200000	ns	12
RAS# hold time from CAS# precharge	t_{RHCP}	35	-	40	-	45	-	ns	
Refresh Cycle									
CAS# hold time (CBR refresh)	t_{CHR}	9	-	9	-	14	-	ns	1
CAS# set-up time (CBR refresh)	t_{CSR}	10	-	10	-	10	-	ns	1
Refresh period	t_{REF}								
4K refresh		-	64	-	64	-	64	ms	
8K refresh		-	64	-	64	-	64	ms	
RAS# precharge to CAS# hold time	t_{RPC}	4	-	4	-	4	-	ns	

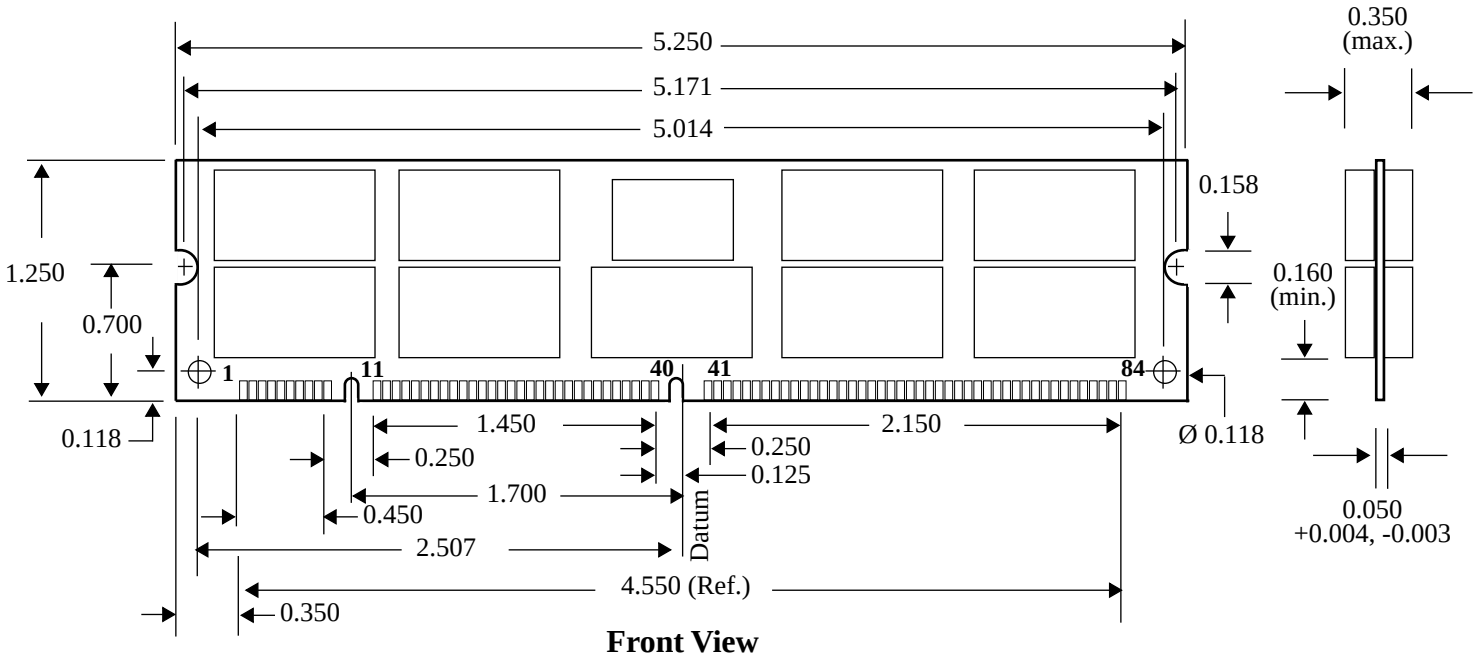
Notes:

1. An initial pause of atleast 200µs is required after power-up followed by any eight RAS# cycles before device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measure with a load equivalent to 2 TTL(5V device)/1 TTL(3.3V device) loads and 100pF.
4. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) limit can be met; t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS# leading edge in early write cycles.
10. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA} , t_{CAC} or $t_{ACP.}$
12. t_{RASP} defines RAS# pulse width in fast page mode cycles.
13. $t_{AR,}$ $t_{WC,}$ t_{DHR} are referenced to t_{RAD}(max).

Physical Dimensions

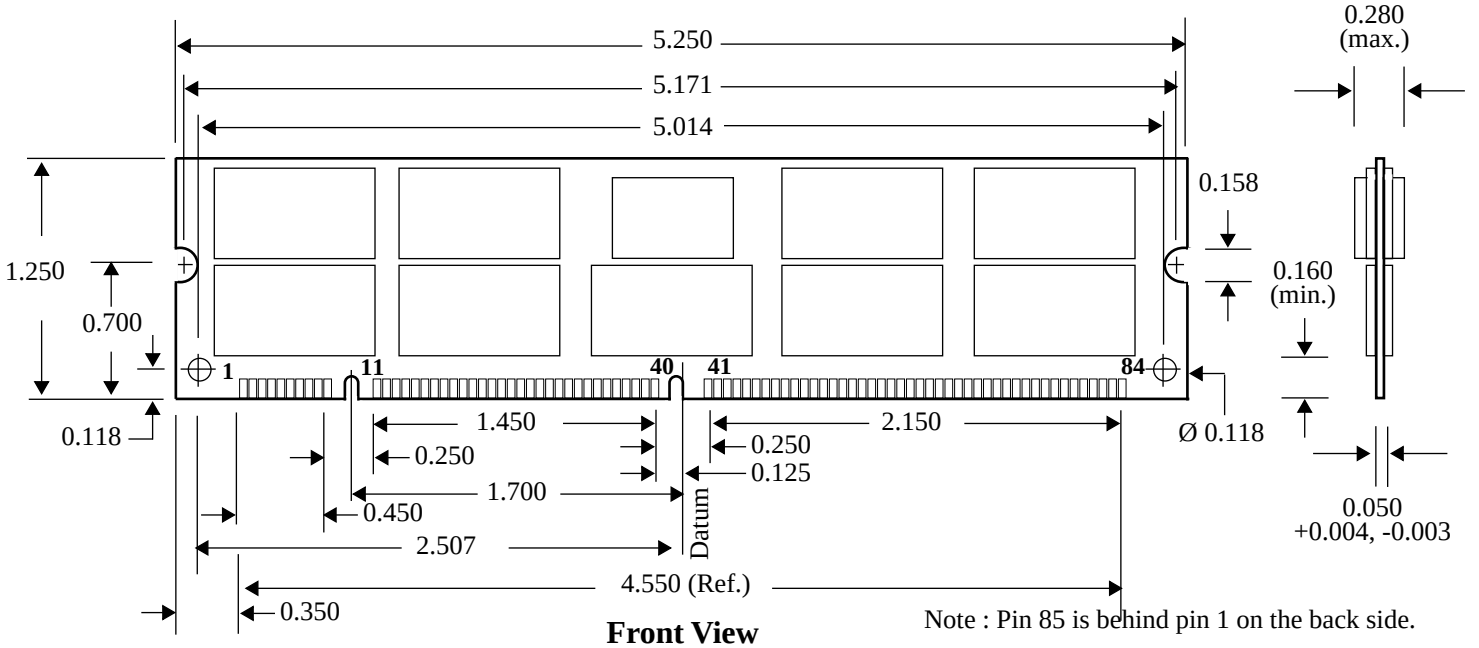
168-pin 5.0V DIMM Module

SOJ Based



Front View

TSOP Based



Front View

Note : Pin 85 is behind pin 1 on the back side.

(All dimensions are in inches with ±0.005" tolerance unless specified otherwise.)

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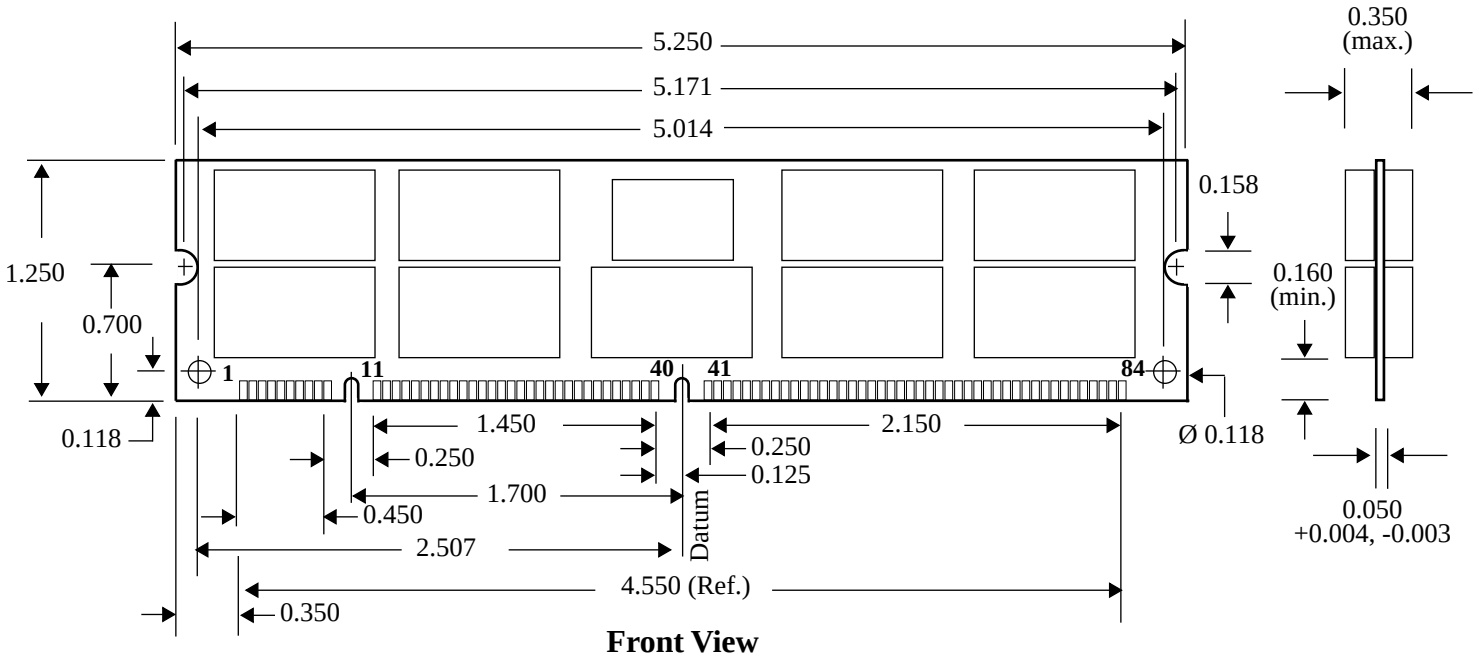
Physical Dimensions

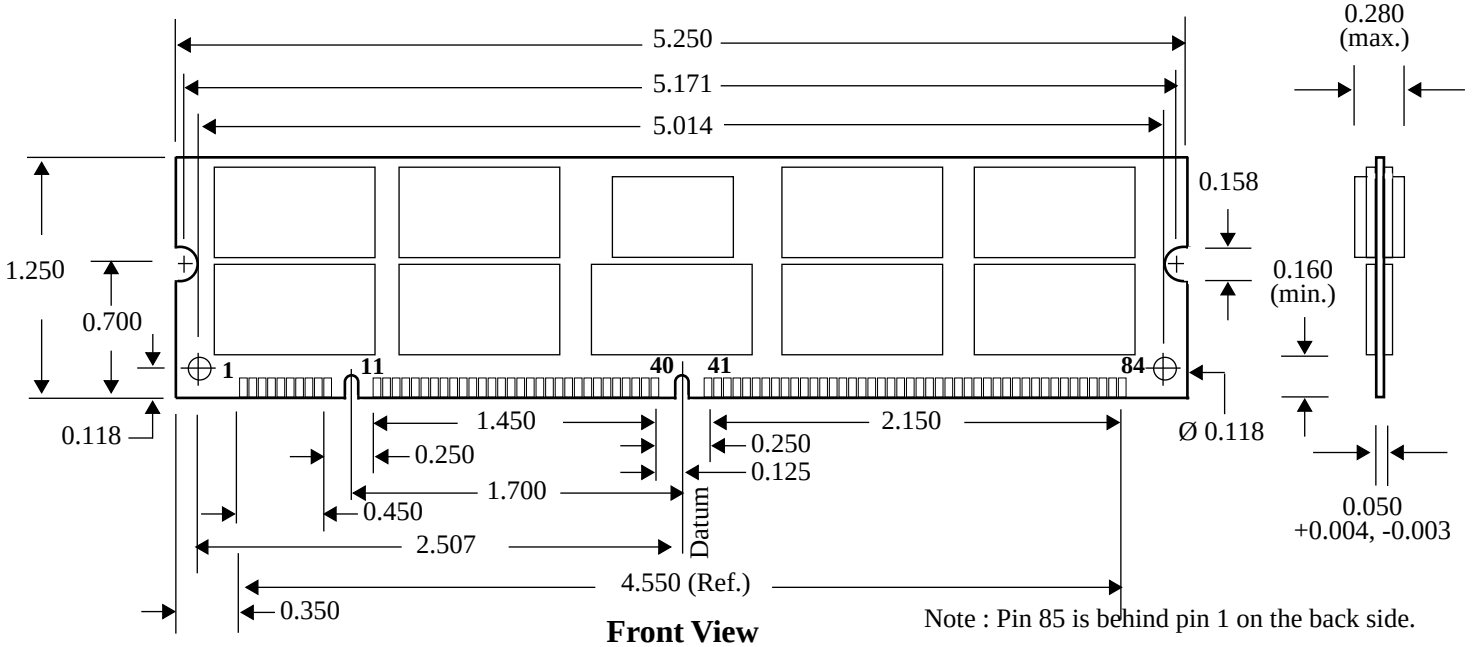
168-pin 3.3V DIMM Module

SOJ Based



Front View

TSOP Based



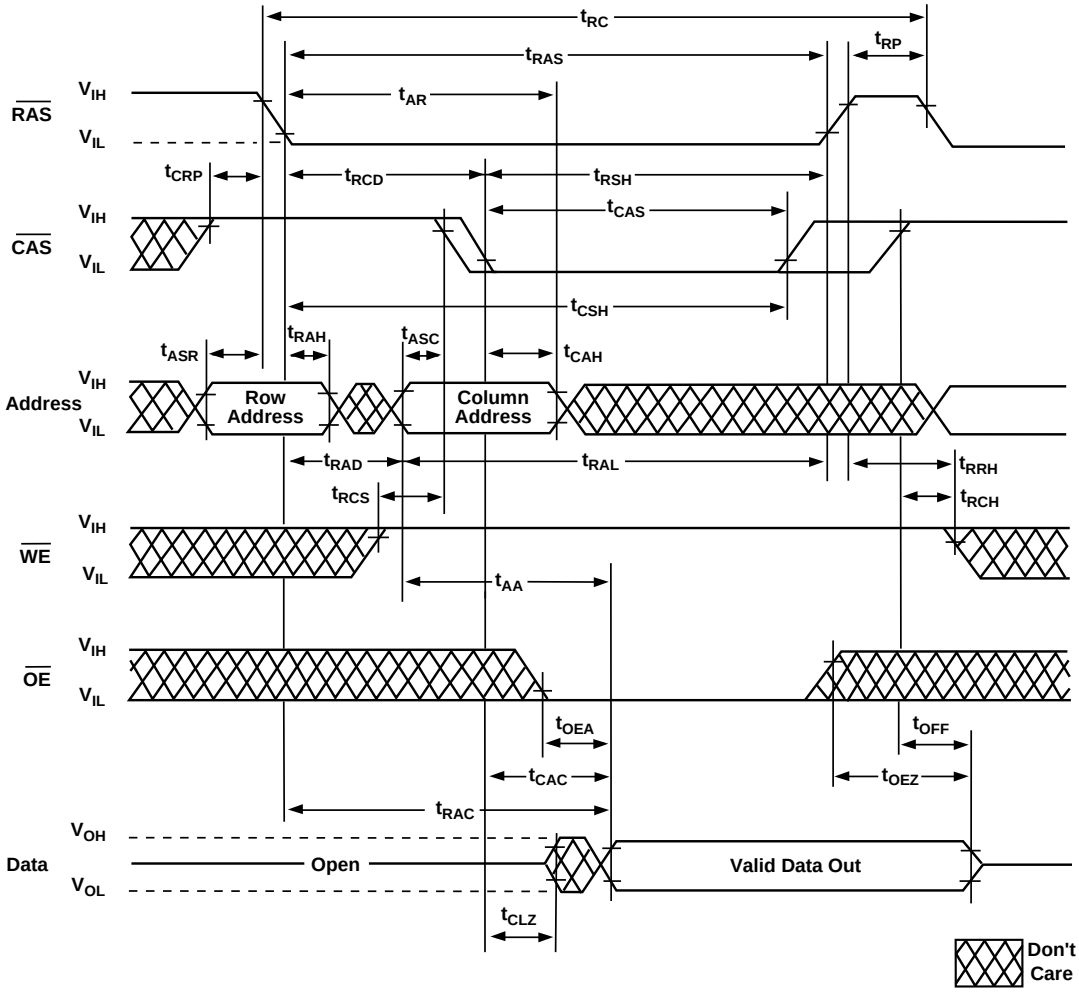
Front View

Note : Pin 85 is behind pin 1 on the back side.

(All dimensions are in inches with ±0.005" tolerance unless specified otherwise.)

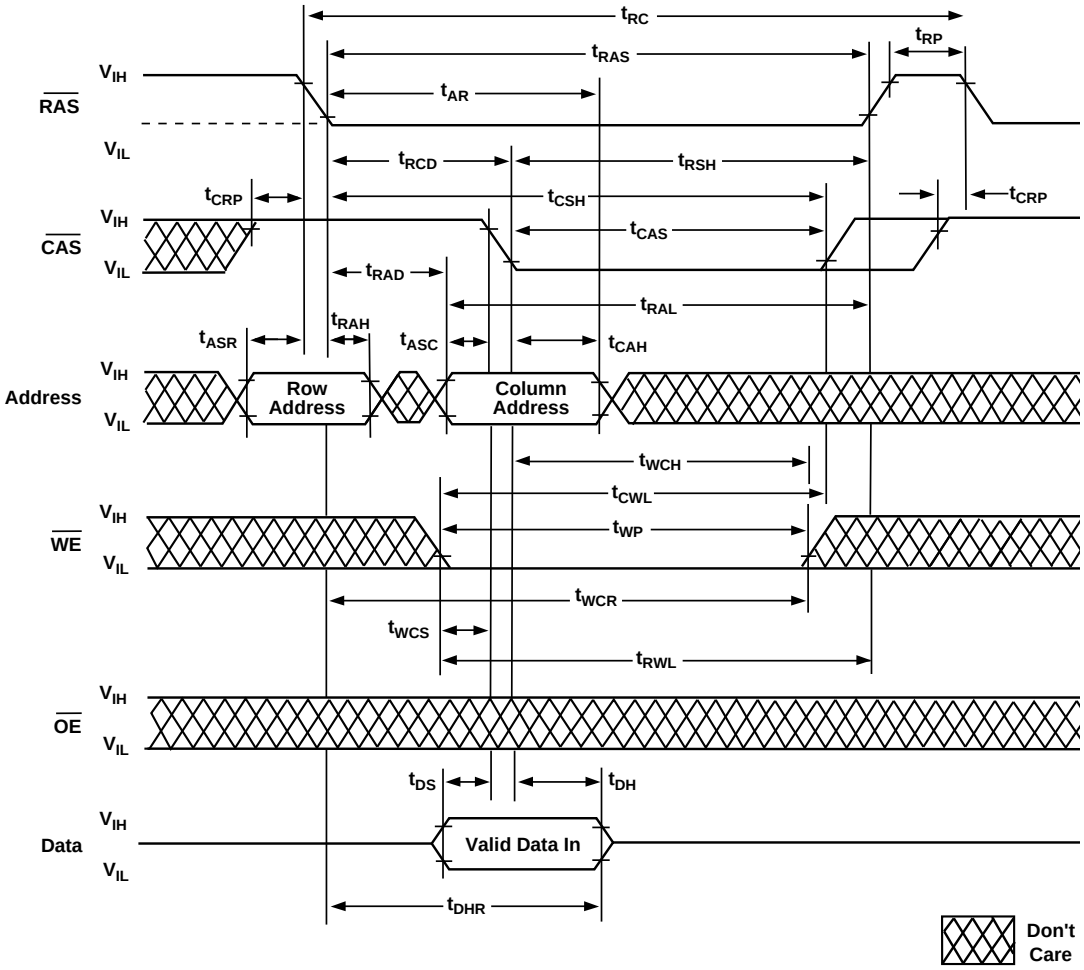
FPM-based Module Timing Waveforms

Read Cycle



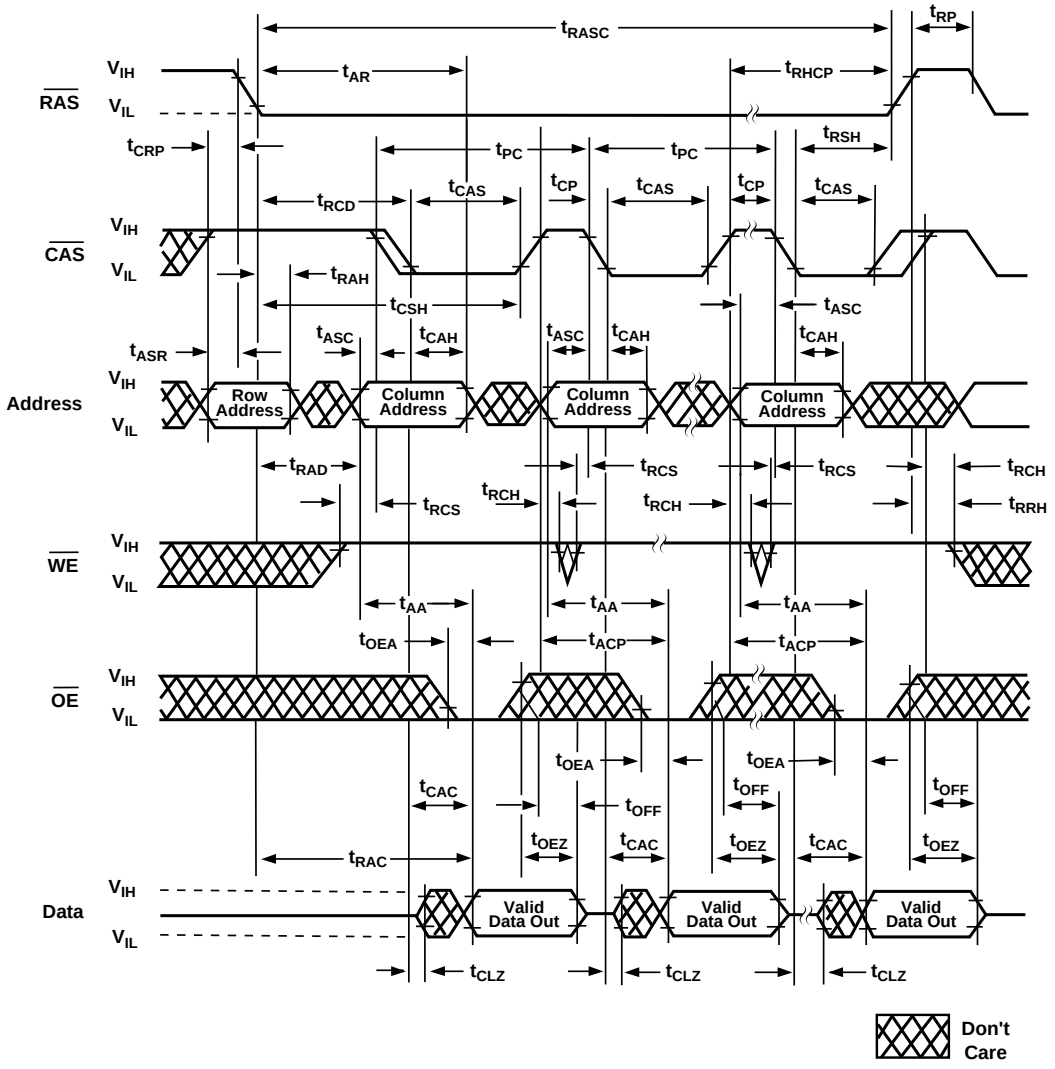
FPM-based Module Timing Waveforms (cont'd)

Write Cycle (Early Write)



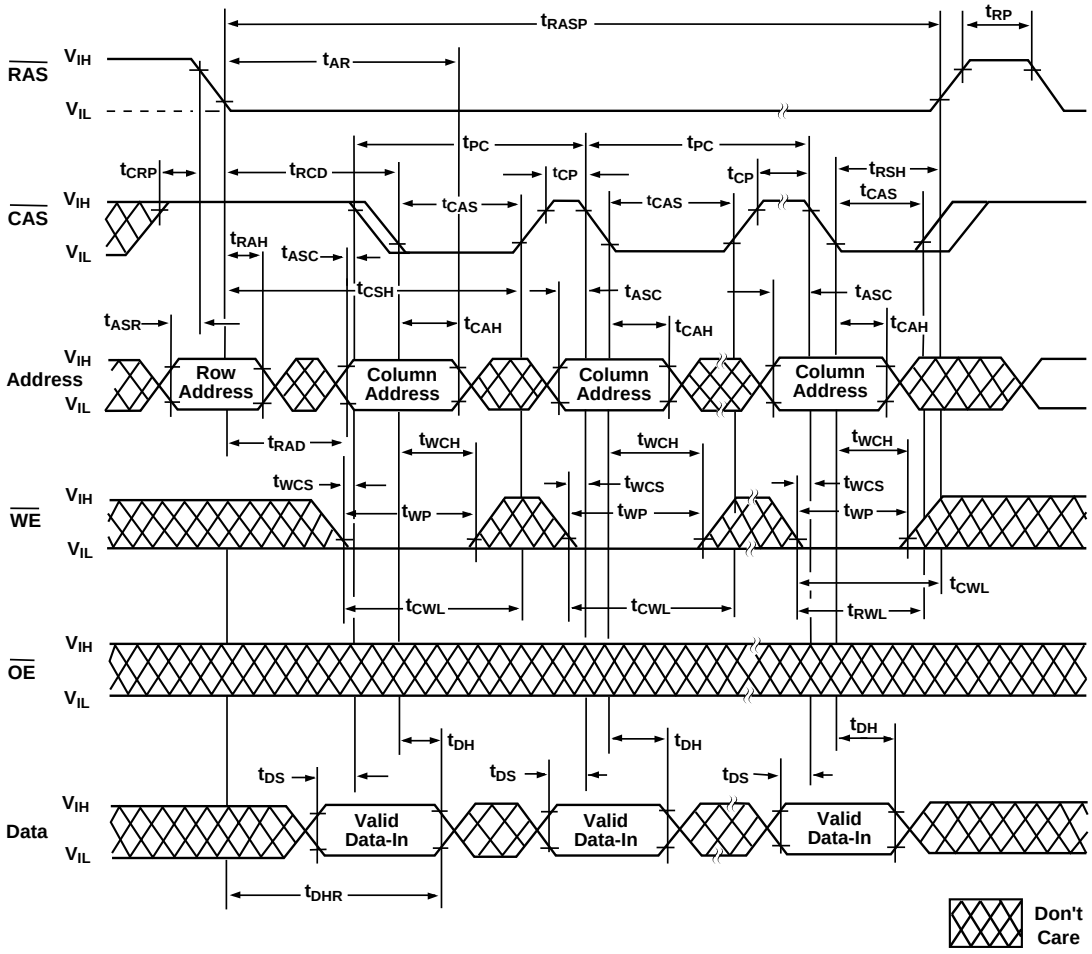
FPM-based Module Timing Waveforms (cont'd)

Fast Page Mode Read Cycle



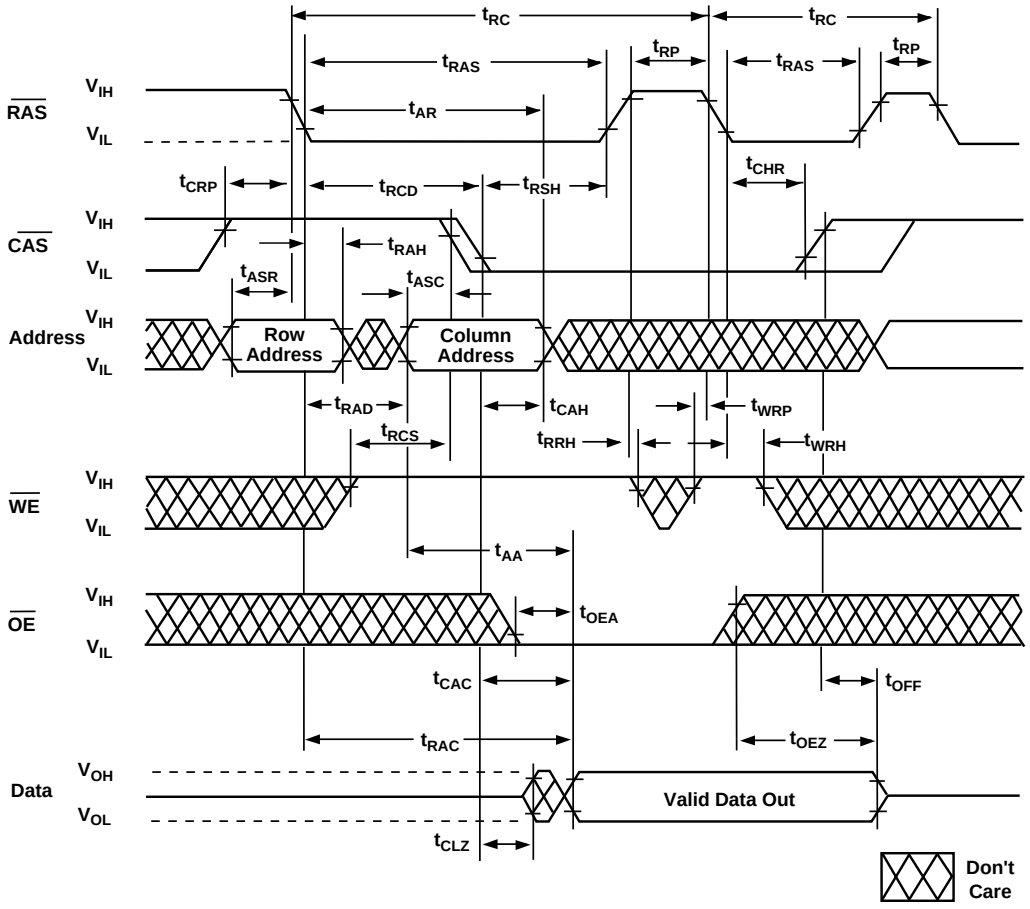
FPM-based Module Timing Waveforms (cont'd)

Fast Page Mode Write Cycle (Early Write)



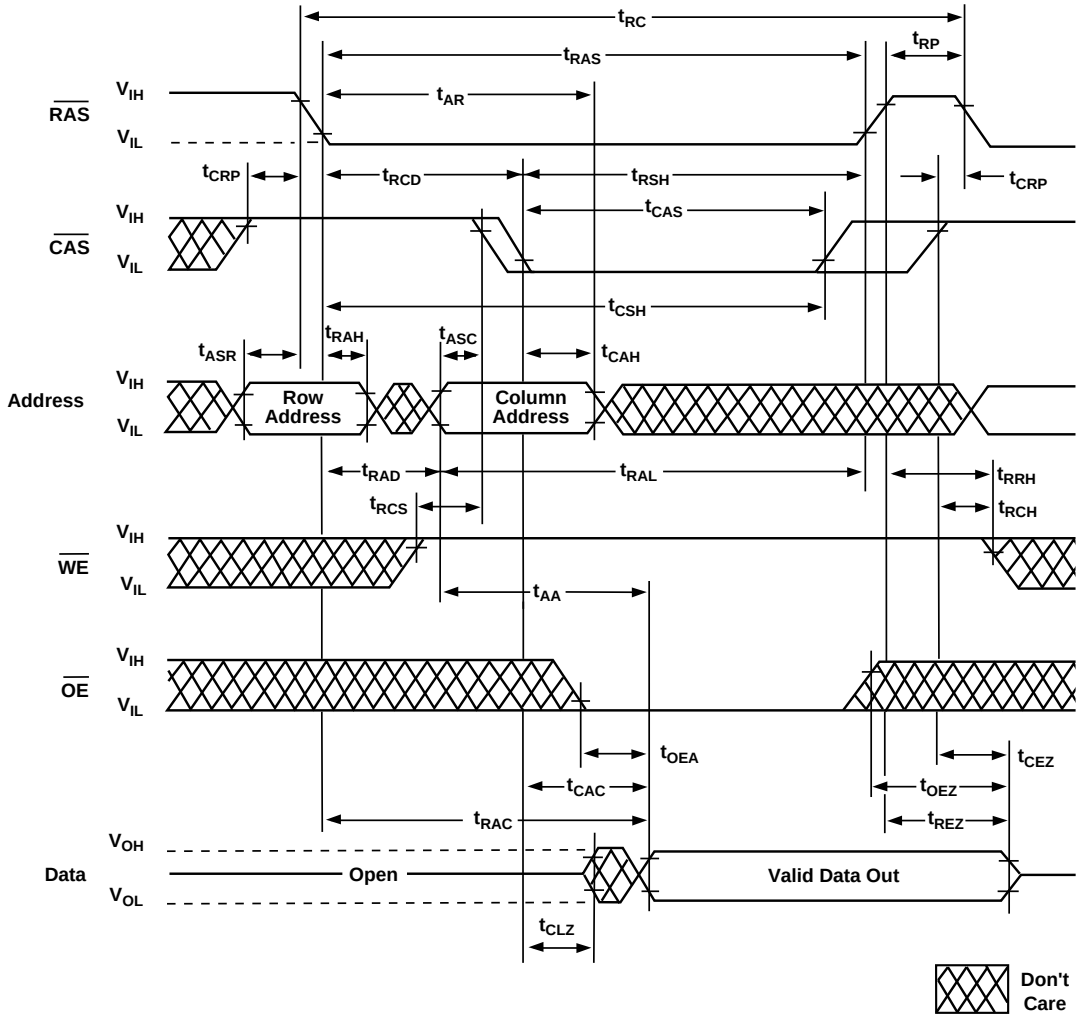
FPM-based Module Timing Waveforms (cont'd)

Hidden Refresh Cycle



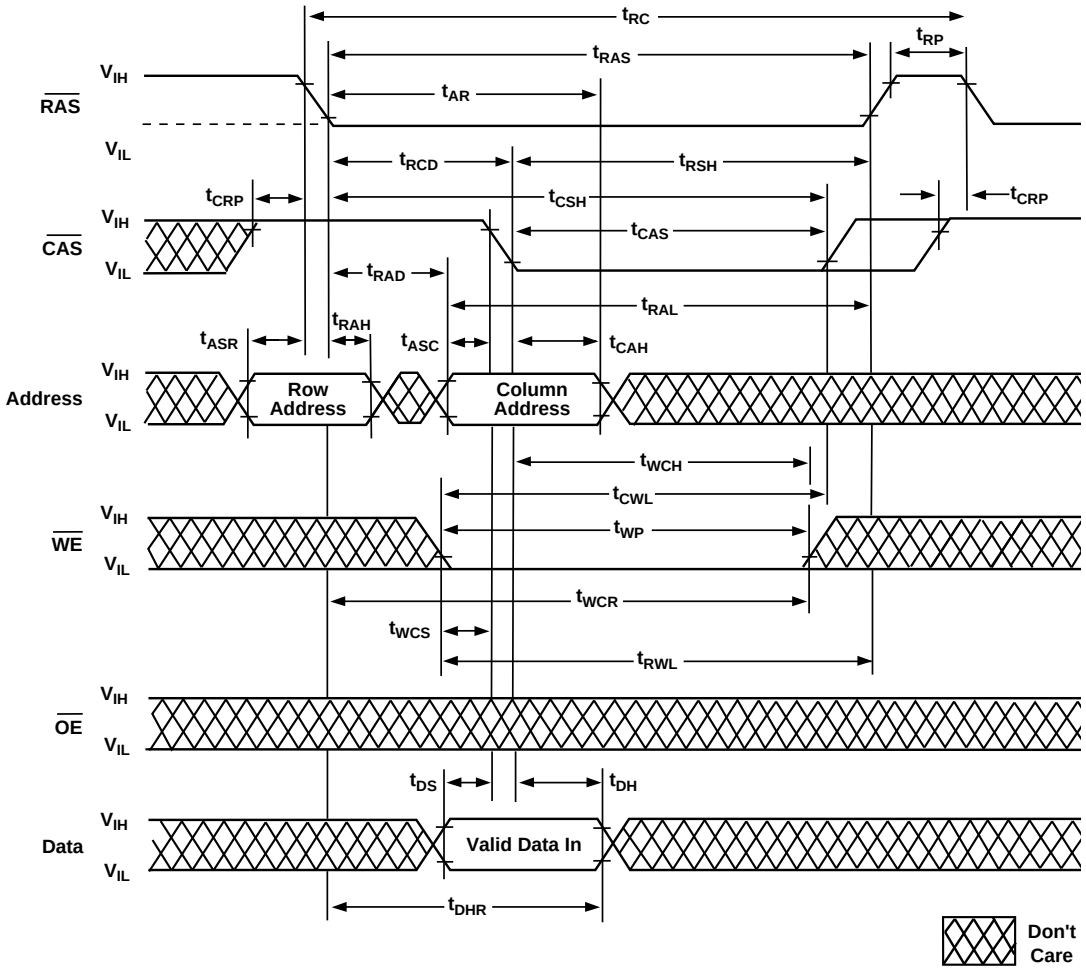
EDO-based Module Timing Waveforms

Read Cycle



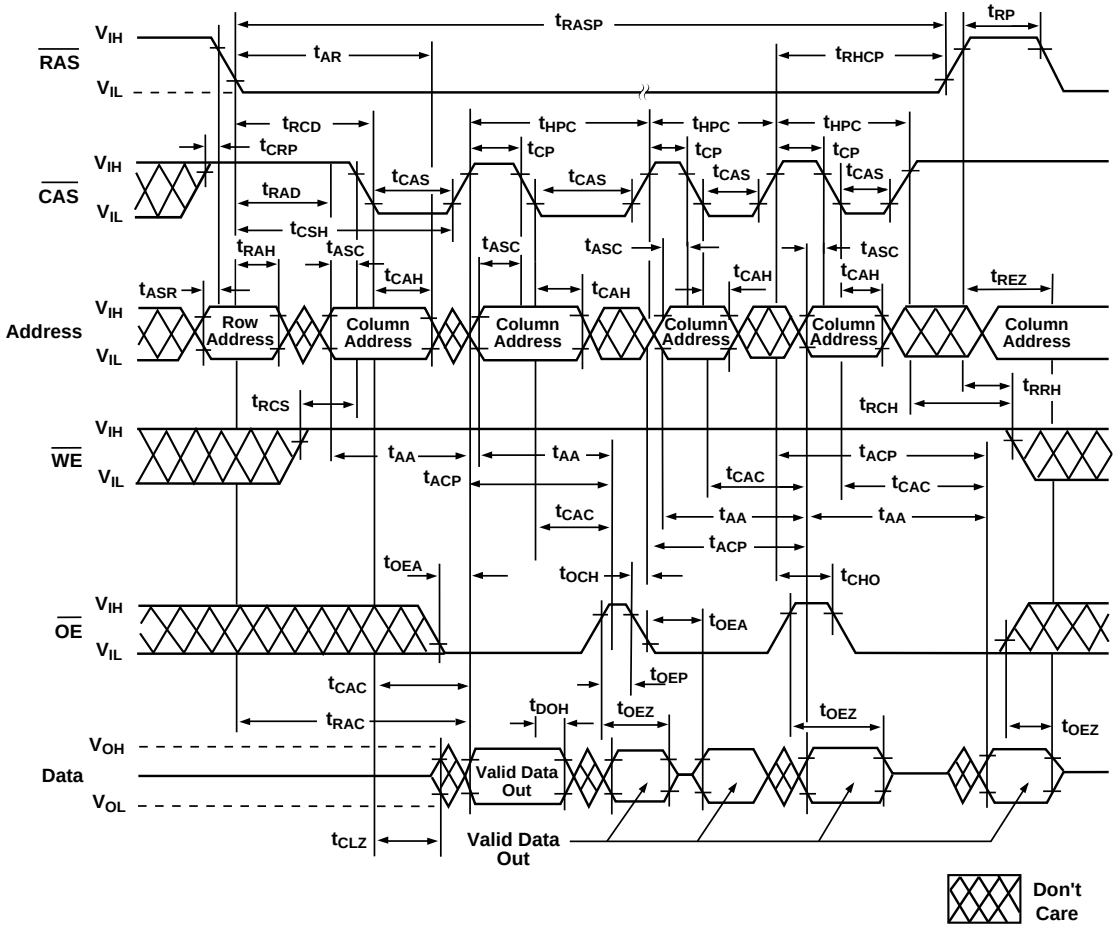
EDO-based Module Timing Waveforms (cont'd)

Write Cycle (Early Write)



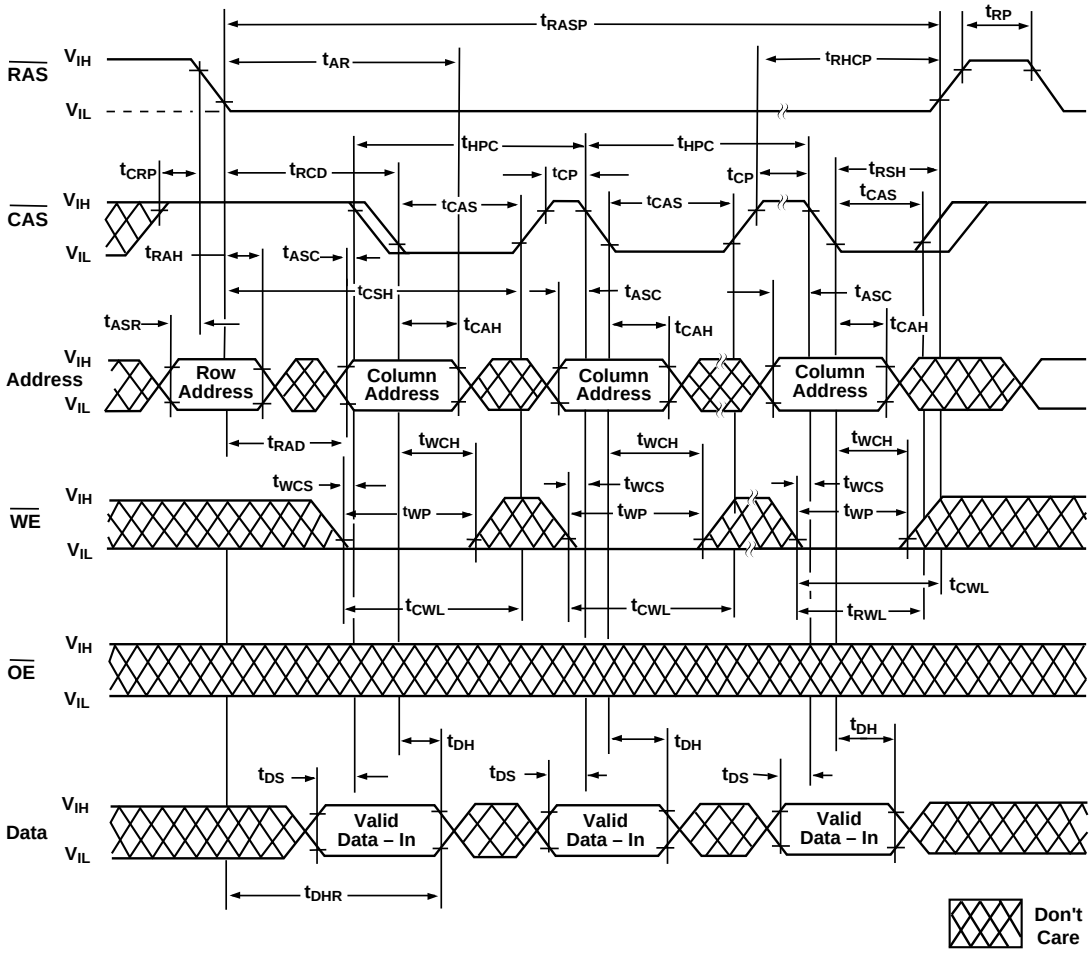
EDO-based Module Timing Waveforms (cont'd)

Hyper Page Read Cycle



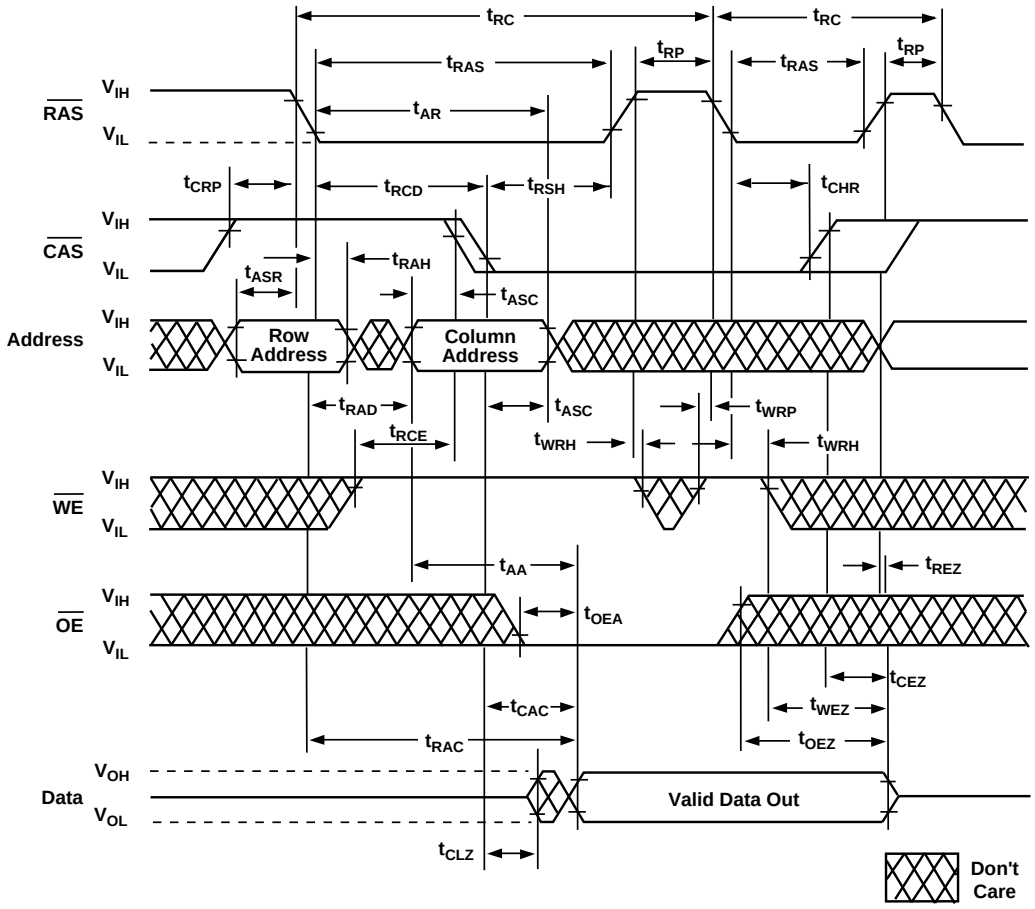
EDO-based Module Timing Waveforms (cont'd)

Hyper Page Write Cycle (Early Write)



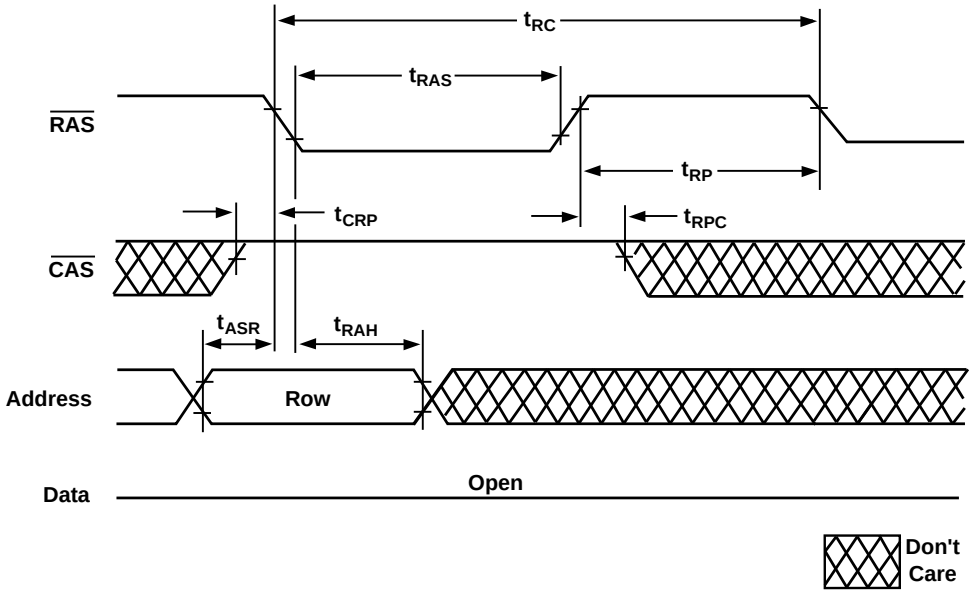
EDO-based Module Timing Waveforms (cont'd)

Hidden Refresh Cycle

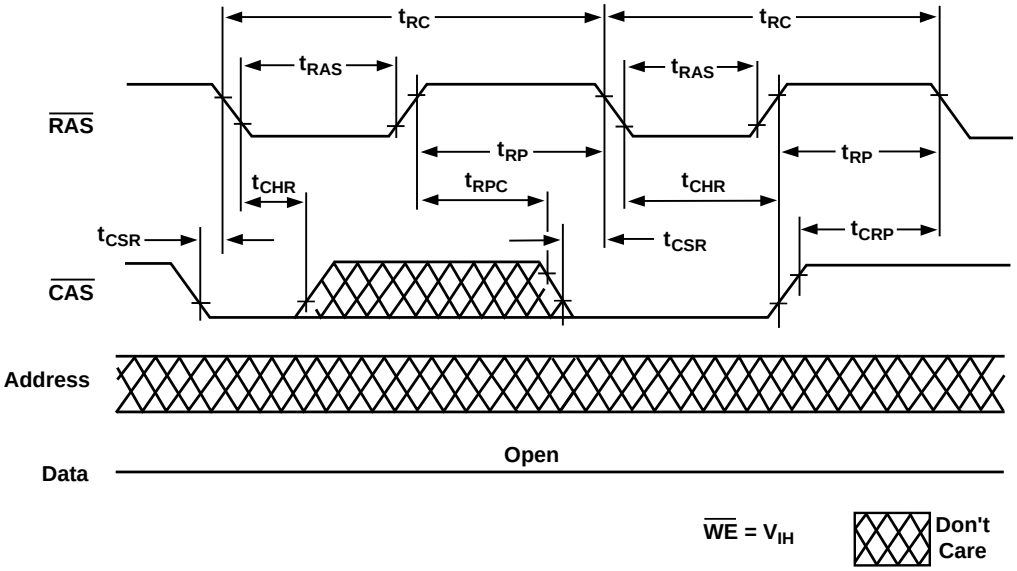


FPM & EDO-based Module Timing Waveforms (cont'd)

RAS# Only Refresh Cycle



CAS#-Before-RAS# Refresh Cycle



Ordering Information

SM	5	72	16	4	0	U	U	E	U	G	U
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)	(10)	(11)	(12)

(1) **SMART**
Modular Technologies

(2) **Product Category**
5 : DRAM SIMM / DIMM

(3) **Module Data Bus Width**
72 : x72

(4) **Module Address Depth**
16 : 16M

(5) **Device Data Width**
4 : x4

(6) **Special Device Feature**
0 : Standard

(7) **Voltage / Mode**
0 : 5.0V / Fast Page Mode
1 : 3.3V / Fast Page Mode
8 : 5.0V / Hyper Page Mode (EDO)
9 : 3.3V / Hyper Page Mode (EDO)

(8) **Refresh / Power**
4 : 4K Ref. / Standard Power
8 : 8K Ref. / Standard Power

(9) **Module Configuration**
E : ECC

(10) **Device Physicals**
4 : SOJ DRAMs (400mil)
6 : TSOP DRAMs (400mil)

(11) **Module Lead Finish**
G : Gold

(12) **Module Access Speed**
5 : 50ns
6 : 60ns
7 : 70ns

Note : “U” in the part number should be replaced by user specified option.

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