KMM372F1600AK/AS & KMM372F1680AK/AS Fast Page with EDO Mode

16Mx72 DRAM DIMM with ECC based on 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F160(8)0A is a 16M bit x 72 Dynamic RAM high density memory module. The Samsung KMM372F160(8)0A consists of eighteen CMOS 16Mx4bit DRAMs in SOJ/TSOP-II 400mil packages, and two 16 bits driver IC in 48pin TSSOP packages mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F160(8)0A is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFOMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-5	50ns	18ns	90ns	26ns
-6	60ns	20ns	110ns	30ns
-7	70ns	25ns	130ns	33ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
KMM372F1600AK	SOJ	4K	4K/64ms	
KMM372F1600AS	TSOP			
KMM372F1680AK	SOJ	8K	4K/64ms	8K/64ms
KMM372F1680AS	TSOP			

- Fast Page with EDO Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except $\overline{RAS}$ and DQ
- PCB : **Height(1250mil)**, double sided component

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PIN CONFIGURATIONS (Front Side / Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	RSVD	57	DQ22	85	Vss	113	RSVD	141	DQ58
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	*$\overline{RAS1}$	142	DQ59
3	DQ1	31	$\overline{OE0}$	59	Vdd	87	DQ37	115	RFU	143	Vdd
4	DQ2	32	Vss	60	DQ24	88	DQ38	116	Vss	144	DQ60
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU
6	Vdd	34	A2	62	RFU	90	Vdd	118	A3	146	RFU
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61
10	DQ7	38	A10	66	DQ26	94	DQ43	122	A11	150	DQ62
11	DQ8	39	A12	67	DQ27	95	DQ44	123	*A13	151	DQ63
12	Vss	40	Vdd	68	Vss	96	Vss	124	Vdd	152	Vss
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65
15	DQ11	43	Vss	71	DQ30	99	DQ47	127	Vss	155	DQ66
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67
17	DQ13	45	$\overline{RAS2}$	73	Vdd	101	DQ49	129	*$\overline{RAS3}$	157	Vdd
18	Vdd	46	$\overline{CAS4}$	74	DQ32	102	Vdd	130	*$\overline{CAS5}$	158	DQ68
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	RSVD	159	DQ69
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	$\overline{PDE}$	160	DQ70
21	DQ16	49	Vdd	77	DQ35	105	DQ52	133	Vdd	161	DQ71
22	DQ17	50	RSVD	78	Vss	106	DQ53	134	RSVD	162	Vss
23	Vss	51	RSVD	79	PD1	107	Vss	135	RSVD	163	PD2
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6
26	Vdd	54	Vss	82	PD7	110	Vdd	138	Vss	166	PD8
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1
28	$\overline{CAS0}$	56	DQ21	84	Vdd	112	*$\overline{CAS1}$	140	DQ57	168	Vdd

NOTE : A12 is used for only KMM372F1680AK/AS (8K ref.)

PIN NAMES

Pin Name	Function
A0, B0, A1 - A11	Address Input (4K ref.)
A0, B0, A1 - A12	Address Input (8K ref.)
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
Vdd	Power(+3.3V)
Vss	Ground
NC	No Connection
$\overline{PDE}$	Presence Detect Enable
PD1-8	Presence Detect
ID0-1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked "*" are not used in this module.

PD & ID Table

Pin	50NS	60NS	70NS
PD1	1	1	1
PD2	1	1	1
PD3	1	1	1
PD4	1	1	1
PD5	1	1	1
PD6	0	1	0
PD7	0	1	1
PD8	0	0	0
ID0	0	0	0
ID1	0	0	0

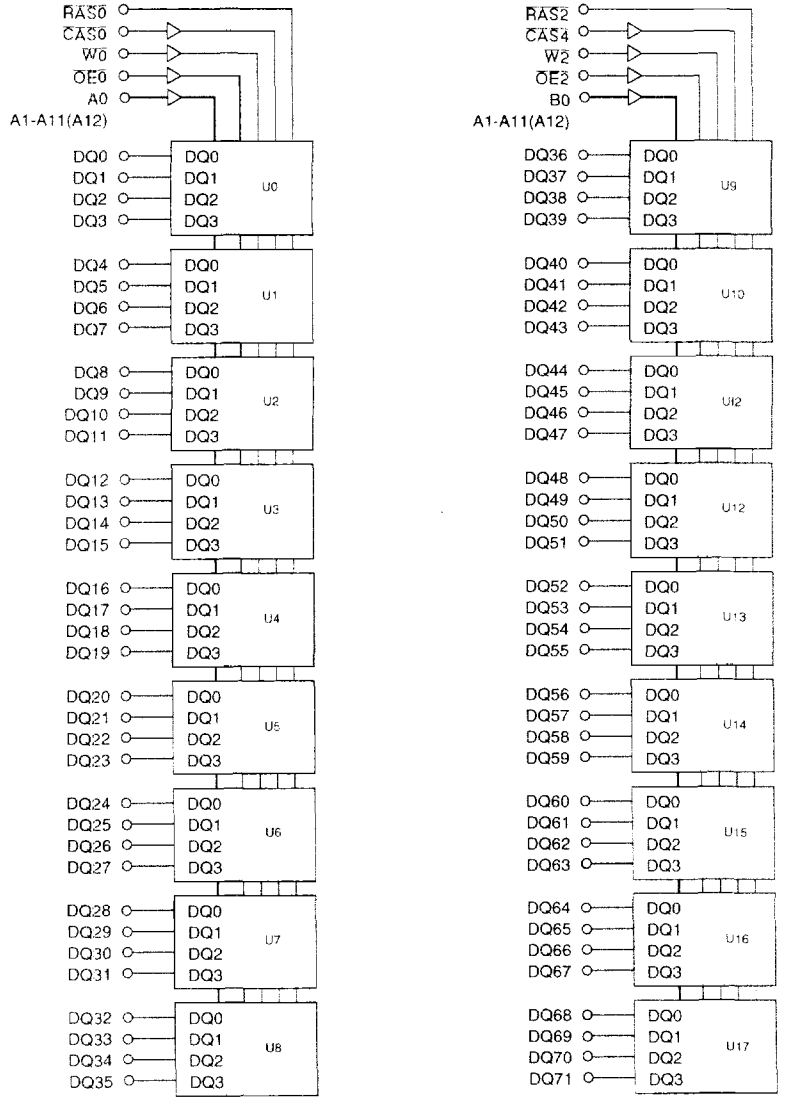
PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for Vss & 1 for N.C

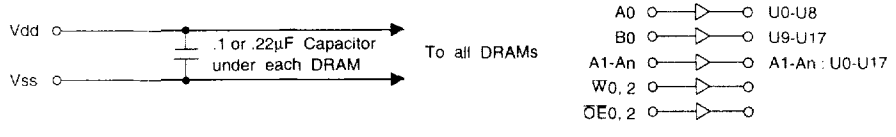
PD Note: PD & ID Terminals must each be pulled up through a resistor to Vdd at the next higher level assembly.
PDs will either be open (NC) or driven to Vss via on-board buffer circuits.

ID Note : IDs will either be open (NC) or connected directly to Vss without a buffer.

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372F1680AK/AS (8K ref.)



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to +4.6	V
Voltage on Vdd supply relative to Vss	Vdd	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +125	°C
Power Dissipation	Pd	18	W
Short Circuit Output Current	IOS	50	mA

* Permanent device camage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vdd	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vdd+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1: Vdd+1.3V/15ns(3.3V), Pulse width is measured at Vdd.
*2: -1.3V/15ns(3.3V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM372F1600AK/AS		KMM372F1680AK/AS		Unit
		Min	Max	Min	Max	
I_{CC1}	- 5	-	2700	-	1800	mA
	- 6	-	2520	-	1620	mA
	- 7	-	2340	-	1440	mA
I_{CC2}		-	100	-	100	mA
I_{CC3}	- 5	-	2700	-	1800	mA
	- 6	-	2520	-	1620	mA
	- 7	-	2340	-	1440	mA
I_{CC4}	- 5	-	2160	-	1980	mA
	- 6	-	1980	-	1800	mA
	- 7	-	1800	-	1620	mA
I_{CC5}		-	30	-	30	mA
I_{CC6}	- 5	-	2700	-	2700	mA
	- 6	-	2520	-	2520	mA
	- 7	-	2340	-	2340	mA
$I_{I(L)}$		-45	45	-45	45	μA
$I_{O(L)}$		-5	5	-5	5	μA
V_{OH}		2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)
I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)
I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$= VIH, $\overline{RAS}$ cycling @tRC =min.)
I_{CC4} : EDO Mode Current * ($\overline{RAS}$=VIL, $\overline{CAS}$ cycling : tHPC=min.)
I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vdd-0.2V)
I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC =min.)
$I_{I(L)}$: Input Leakage Current (Any input 0 ≤ V_{IN} ≤ Vdd+0.3V, all other pins not under test = 0 V.)
$I_{O(L)}$: Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vdd)
V_{OH} : Output High Voltage Level (I_{OH} = -2mA)
V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1},I_{CC3},I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=VIL. In I_{CC4}, address can be changed maximum once within one EDO mode cycle .

CAPACITANCE (Ta = 25°C, Vdd=3.3V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A12, B0]	CIN1	-	20	pF
Input capacitance [$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	CIN2	-	20	pF
Input capacitance [$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	73	pF
Input capacitance [$\overline{CAS0}$, $\overline{CAS4}$]	CIN4	-	20	pF
Input/Output capacitance [DQ0-71]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vdd=3.3V±0.3V. *See notes 1, 2.*)
Test condition : Vih/Vil=2.0V/0.8V, Voh/Vol=2.0V/0.8V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		ns	
Read-modify-write cycle time	tRWC	133		153		180		ns	
Access time from $\overline{RAS}$	tRAC		50		60		70	ns	3,4,10
Access time from $\overline{CAS}$	tCAC		18		20		25	ns	3,4,5,14
Access time from column address	tAA		30		35		40	ns	3,10,14
$\overline{CAS}$ to output in Low-Z	tCLZ	8		8		8		ns	3,14
$\overline{OE}$ to output in Low-Z	tOLZ	8		8		8		ns	3,14
Output buffer turn-off delay from $\overline{CAS}$	tCEZ	8	18	8	20	8	25	ns	6,11,12,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
$\overline{RAS}$ precharge time	tRP	30		40		50		ns	
$\overline{RAS}$ pulse width	tRAS	50	10K	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	18		20		25		ns	14
$\overline{CAS}$ hold time	tCSH	36		43		48		ns	14
$\overline{CAS}$ pulse width	tCAS	8	10K	10	10K	15	10K	ns	13
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	18	32	18	40	18	45	ns	4,14
$\overline{RAS}$ to column address delay time	tRAD	13	20	13	25	13	30	ns	10,14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	10		10		10		ns	14
Row address set-up time	tASR	5		5		5		ns	14
Row address hold time	tRAH	8		8		8		ns	14
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address to $\overline{RAS}$ lead time	tRAL	30		35		40		ns	14
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{CAS}$	tRCH	0		0		0		ns	8
Read command hold time referenced to $\overline{RAS}$	tRRH	-2		-2		-2		ns	8,14
Write command hold time	tWCH	10		10		15		ns	
Write command pulse width	tWP	10		10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	18		20		25		ns	14
Write command to $\overline{CAS}$ lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	-2		-2		-2		ns	9,14
Data hold time	tDH	15		15		20		ns	9,14
Refresh period (4K/8K Ref)	tREF		64		64		64	ms	
Write command set-up time	tWCS	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	tCWD	36		38		45		ns	7

AC CHARACTERISTICS (Continued)

STANDARD OPERATION	Symbol	-5		-6		-7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{W}$ delay time	tRWD	71		81		94		ns	7,14
Column address to $\overline{W}$ delay time	tAWD	48		53		60		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	tCPWD	53		60		70		ns	
$\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	14
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	tCHR	8		8		13		ns	14
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	3		3		3		ns	14
$\overline{CAS}$ precharge time($\overline{C}$-B-$\overline{R}$ counter test cycle)	tCPT	20		20		30		ns	
Access time from $\overline{CAS}$ precharge	tCPA		35		40		45	ns	3,14
Hyper Page cycle time	tHPC	26		30		33		ns	13
Hyper Page read-modify-write cycle time	tHPRWC	68		77		92		ns	13
$\overline{CAS}$ precharge time (Hyper Page cycle)	tCP	8		10		10		ns	
$\overline{RAS}$ pulse width (Hyper Page cycle)	tRASP	50	200K	60	200K	70	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	tRHCP	35		40		45		ns	14
$\overline{OE}$ access time	tOEA		18		20		25	ns	14
$\overline{OE}$ to data delay	tOED	18		18		25		ns	14
Out put buffer turn off delay from $\overline{OE}$	tOEZ	5	18	5	18	5	25	ns	6,11,14
$\overline{OE}$ command hold time	tOEH	13		15		20		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh)	tWRP	15		15		15		ns	14
$\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh)	tWRH	8		8		8		ns	14
Output data hold time	tDOH	10		10		10		ns	14
Output buffer turn off delay from $\overline{RAS}$	tREZ	3	13	3	15	3	20	ns	6,11,12
Output-buffer turn off delay from $\overline{W}$	tWEZ	3	18	3	20	3	25	ns	6,11,14
$\overline{W}$ to data delay	tWED	20		20		25		ns	14
$\overline{OE}$ to $\overline{CAS}$ hold time	tOCH	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	tCHO	5		5		5		ns	
$\overline{OE}$ precharge time	tOEP	5		5		5		ns	
$\overline{W}$ pulse width(Hyper Page Cycle)	tWPE	5		5		5		ns	
Present Detect Read Cycle									
$\overline{PDE}$ to Valid PD bit	tPD		10		10		10	ns	
$\overline{PDE}$ to PD bit Inactive	tPDOFF	2	7	2	7	2	7	ns	

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NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.

4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.

5. Assumes that tRCD ≥ tRCD(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.

7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameter.
   They are included in the data sheet as electrical characteristics only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
   If tCWD≥tCWD(min), tRWD≥tRWD(min) and tAWD≥tAWD(MIN), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminated.

8. Either tRCH or tRRH must be satisfied for a read cycle.

9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.

10. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

11. tCEZ(max), tREZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

13. tASC ≥ 6ns

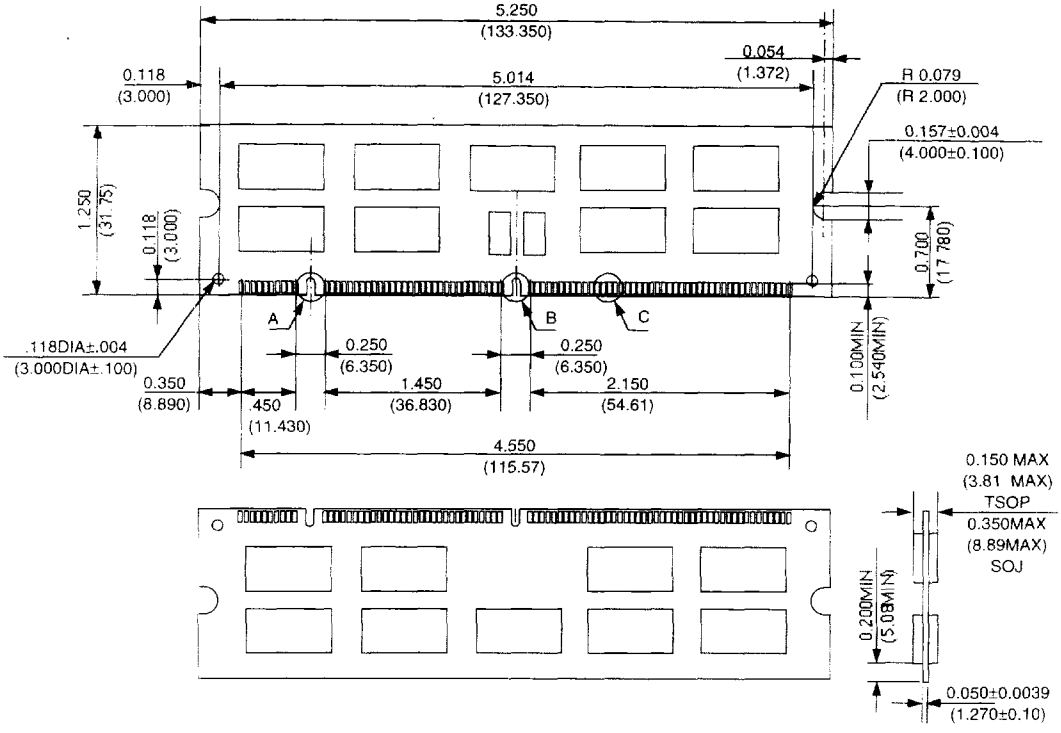
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

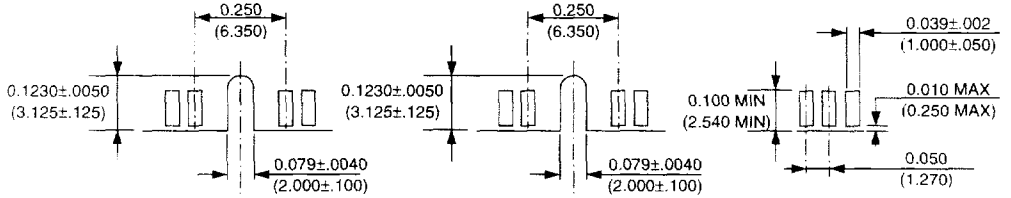
TIMING DIAGRAM

Please refer to attached timing chart (IV) !!!

PACKAGE DIMENSIONS

Units : Inches (millimeters)





Detail A Detail B Detail C

Tolerances : ±.005 (.13) unless otherwise specified

The used device is 16Mx4 DRAM with EDO mode, SOJ (400 mil) or TSOPII.(Forward) .
DRAM Part No. : KMM372F1600AK/AS - KM44V16104AK, KM44V16104AS.
KMM372F1680AK/AS - KM44V16004AK, KM44V16004AS.

Revision History
Rev 0.0 : Jan. '96