

# DALLAS

SEMICONDUCTOR

## DS1589/DS1593

### Serialized Real Time Clocks

#### FEATURES

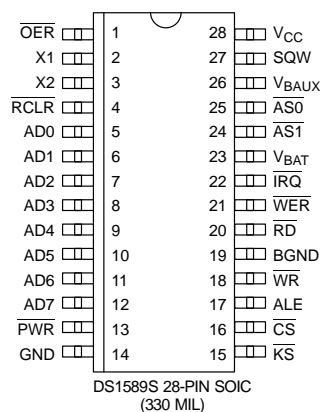
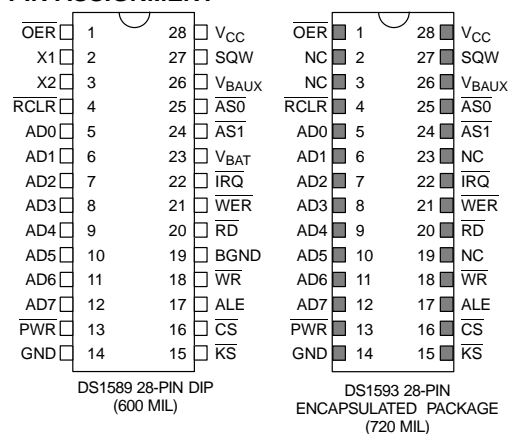
Incorporates industry standard DS1287 PC clock plus enhanced features:

- 64-bit Silicon serial number
- Power control circuitry supports system power on from date/time alarm or key closure
- 114 bytes user NVRAM
- 8K bytes additional NVRAM
- Auxiliary battery input
- RAM clear input
- Century register
- 32 kHz output for power management
- Compatible with existing BIOS for original DS1287 functions
- AD7–AD0 are open drain to allow interface to +3V logic
- Available as chip (DS1589) or stand-alone module (DS1593) with embedded lithium battery and crystal

#### PIN DESCRIPTION

OER	-	RAM output enable
X1	-	Crystal input
X2	-	Crystal output
RCLR	-	RAM clear input
AD0-AD7	-	Mux'ed address/data bus; open drain
PWR	-	Power on interrupt output; open drain
KS	-	Kickstart input
CS	-	RTC Chip select input
ALE	-	RTC address strobe
WR	-	RTC write data strobe
RD	-	RTC read data strobe
WER	-	RAM write data strobe
IRQ	-	Interrupt request output
AS1	-	RAM upper address strobe
AS0	-	RAM lower address strobe
SQW	-	Square wave output
V <sub>CC</sub>	-	+5V supply
GND	-	Ground
V <sub>BAT</sub>	-	Battery + supply
V <sub>BAUX</sub>	-	Auxiliary battery supply
BGND	-	Battery ground

#### PIN ASSIGNMENT



#### ORDERING INFORMATION

DS1589	RTC Chip; 28-pin DIP
DS1589S	RTC Chip; 28-pin SOIC
DS1593	RTC Module; 28-pin DIP

**DESCRIPTION**

The DS1589 and DS1593 are RAMified real time clocks (RTC's) designed as upward-compatible successors to the industry standard DS1287, DS1387, and DS1488 PC real time clocks. As such, these devices incorporate a number of enhanced features including a silicon serial number, power on/off control circuitry, 114 bytes of user NVSRAM, and 8K bytes of additional NVSRAM.

The DS1589 is a clock/calendar chip with the features described above. An external crystal and battery are the only components required to maintain time-of-day and memory status in the absence of power. The DS1593 incorporates the DS1589 chip, a 32.768 kHz

crystal, and a lithium battery in a complete, self-contained timekeeping module. The entire unit is fully tested at Dallas such that a minimum of 10 years of timekeeping and data retention in the absence of  $V_{CC}$  is guaranteed.

The DS1589 chip and DS1593 module are identical in function to the DS1585 and DS1587, respectively, with the exception that the AD7–AD0 data bus pins are open drain. This allows easy interface to +3V logic in mixed supply systems. The operational characteristics specific to the DS1589/DS1593 are described in this data sheet. All other operational details are discussed in the DS1585/DS1587 data sheet.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	−0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−40°C to +70°C
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Input Logic 1	$V_{IH}$	2.2		$V_{CC}+0.3$	V	1
Input Logic 0	$V_{IL}$	-0.3		+0.8	V	1
Battery Voltage	$V_{BAT}$	2.5		3.7	V	10
Auxiliary Battery Voltage	$V_{BAUX}$	2.5		3.7	V	10

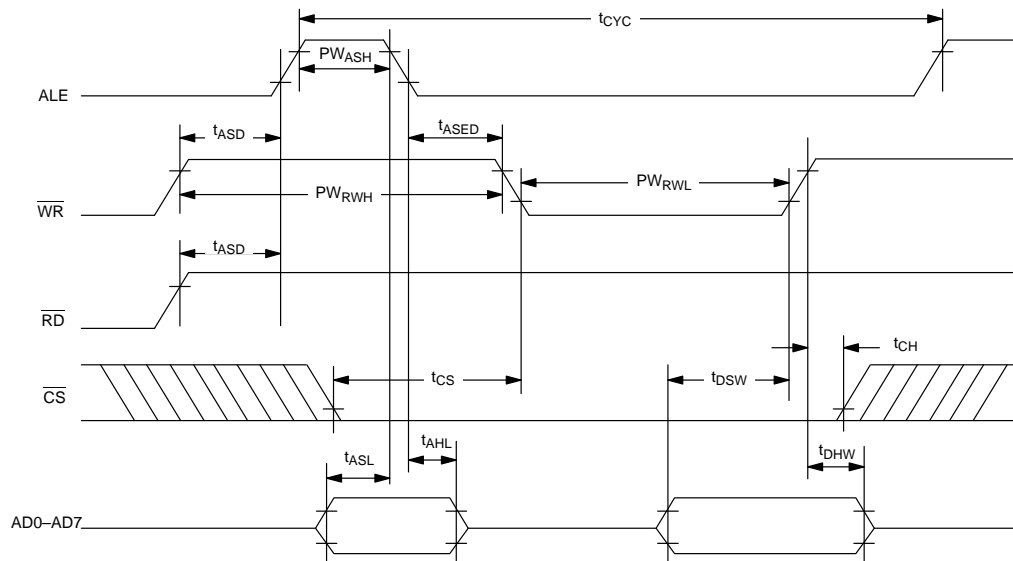
**DC ELECTRICAL CHARACTERISTICS**

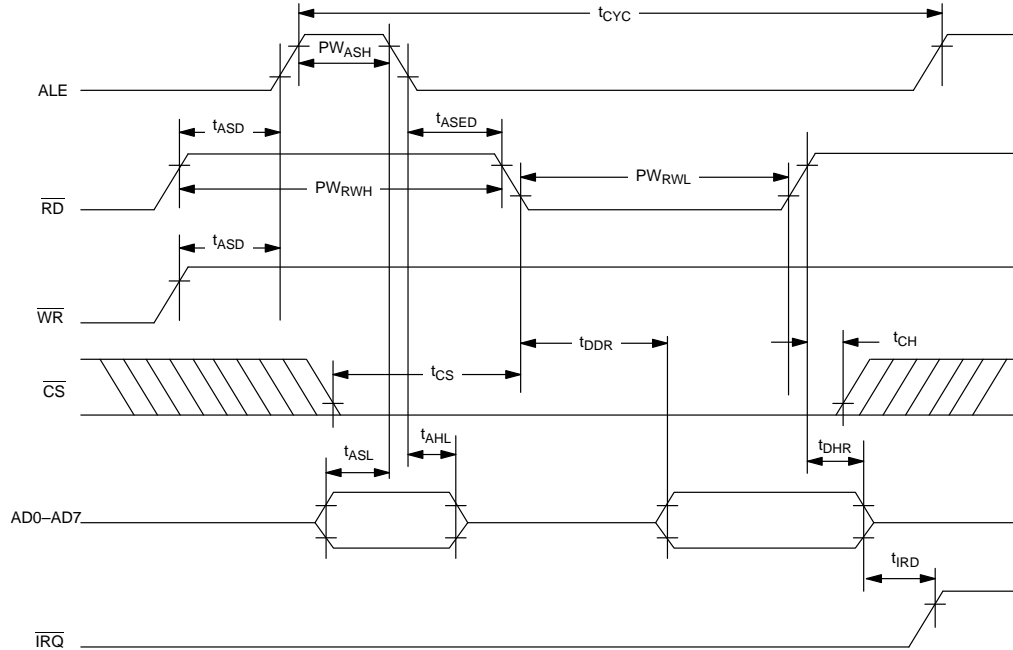
(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Current	$I_{CC1}$		35	50	mA	2
Standby Current $\overline{CS} = V_{CC} - 0.3V$	$I_{CC2}$		1	5.0	mA	6
Input Leakage	$I_{IL}$	-1.0		+1.0	$\mu A$	3
I/O Leakage	$I_{LO}$	-1.0		+1.0	$\mu A$	3, 4
Output @ 2.4V	$I_{OH}$	-1.0			mA	1, 4
Output @ 0.4V	$I_{OL}$			2.0	mA	1
Power Fail Trip Point	$V_{PF}$		4.25		V	1
PWR Output @ 0.4V	$I_{OLPWR}$			10.0	mA	1

**RTC AC TIMING CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 4.5V$  to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	$t_{CYC}$	335		DC	ns	5, 12
Pulse Width, $\overline{RD}/\overline{WR}$ Low	$PW_{RWL}$	155			ns	5, 12
Pulse Width, $\overline{RD}/\overline{WR}$ High	$PW_{RWH}$	150			ns	5, 12
Input Rise and Fall Time	$t_R, t_F$			30	ns	
Chip Select Setup Time Before $\overline{WR}$ , or $\overline{RD}$	$t_{CS}$	20			ns	
Chip Select Hold Time	$t_{CH}$	0			ns	
Read Data Hold Time	$t_{DHR}$	10		80	ns	
Write Data Hold Time	$t_{DHW}$	0			ns	
Muxed Address Valid Time to ALE Fall	$t_{ASL}$	30			ns	
Muxed Address Hold Time from ALE fall	$t_{AHL}$	10			ns	
$\overline{RD}$ or $\overline{WR}$ High Setup to ALE Rise	$t_{ASD}$	25			ns	
Pulse Width ALE High	$PW_{ASH}$	60			ns	5, 12
ALE Low Setup to $\overline{RD}$ or $\overline{WR}$ Fall	$t_{ASED}$	40			ns	
Output Data Delay Time from $\overline{RD}$	$t_{DDR}$	20		150	ns	5, 12
Data Setup Time	$t_{DSW}$	100			ns	
$\overline{IRQ}$ Release from $\overline{RD}$	$t_{IRD}$			2	$\mu s$	

**DS1589/DS1593 BUS TIMING FOR WRITE CYCLE TO RTC**

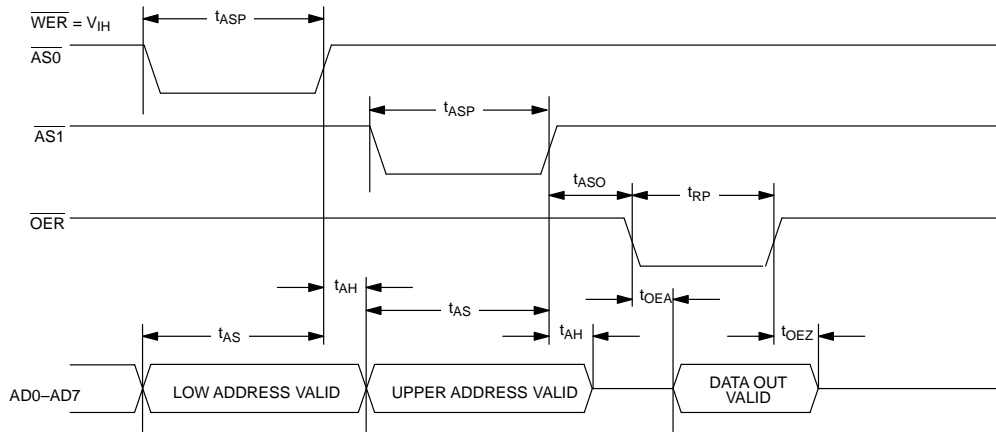
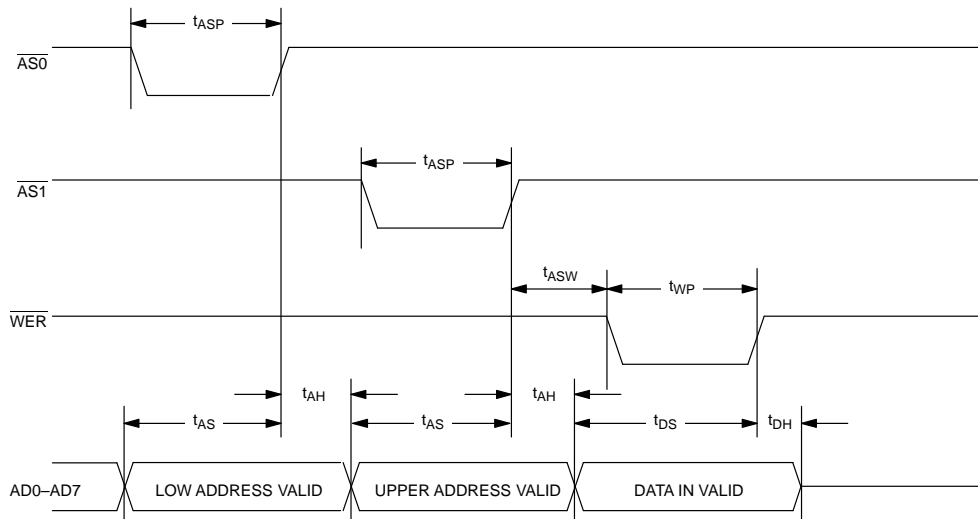
**DS1589/DS1593 BUS TIMING FOR READ CYCLE TO RTC****NOTE:**

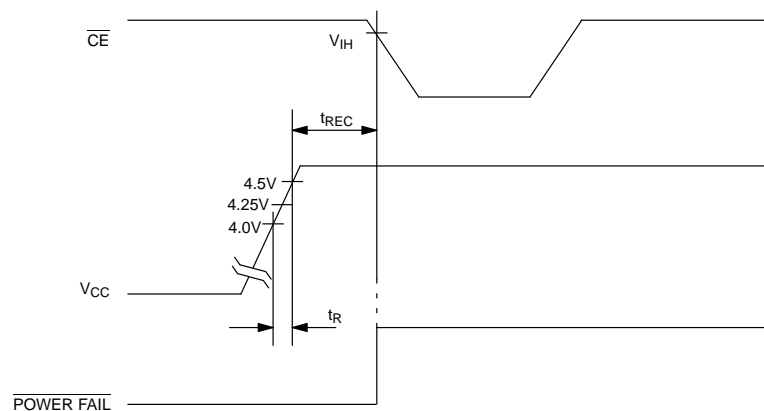
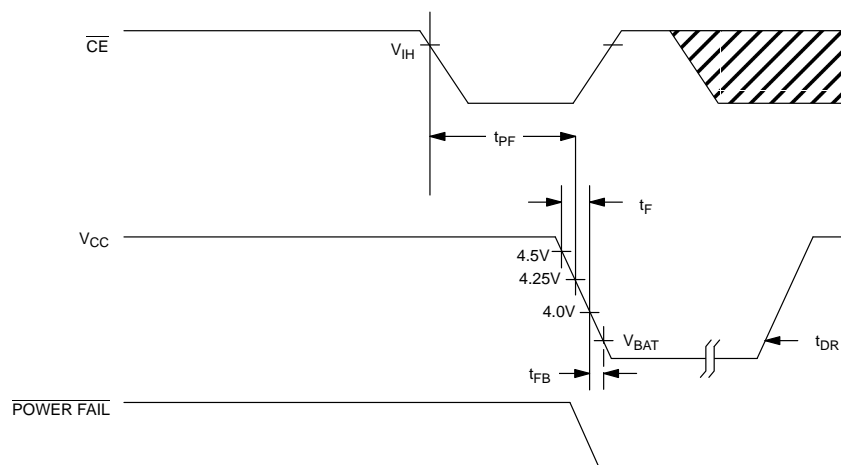
Input Levels = 0.8 volts and 2.2 volts.

Output Levels = 0.4 volts and 2.4 volts.

**8K X 8 AC TIMING CHARACTERISTICS**(0°C to 70°C;  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup Time	$t_{AS}$	50			ns	
Address Hold Time	$t_{AH}$	0			ns	
Data Setup Time	$t_{DS}$	75			ns	
Data Hold Time	$t_{DH}$	0			ns	
Output Enable Access Time	$t_{OEA}$			200	ns	8
Write Pulse Width	$t_{WP}$	125			ns	
$\overline{OER}$ to Output in High Z	$t_{OEZ}$			50	ns	
$\overline{OER}$ Pulse Width	$t_{RP}$	200			ns	
$\overline{AS0}$ , $\overline{AS1}$ Pulse Width	$t_{ASP}$	75			ns	
$\overline{AS0}$ , $\overline{AS1}$ High to $\overline{OER}$ Low	$t_{ASO}$	20			ns	
$\overline{AS0}$ , $\overline{AS1}$ High to $\overline{WER}$ Low	$t_{ASW}$	20			ns	

**BUS TIMING FOR READ CYCLE TO 8K X 8 NV SRAM****BUS TIMING FOR WRITE CYCLE TO 8K X 8 SRAM**

**POWER-UP CONDITION****POWER-DOWN CONDITION**

**POWER-UP POWER-DOWN TIMING**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{\text{CE}}$ High to Power Fail	t <sub>PF</sub>			0	ns	
Recovery at Power Up	t <sub>REC</sub>		150		ms	
V <sub>CC</sub> Slew Rate Power Down	t <sub>F</sub> 4.0 ≤ V <sub>CC</sub> ≤ 4.5V	300			μs	
V <sub>CC</sub> Slew Rate Power Down	t <sub>FB</sub> 3.0 ≤ V <sub>CC</sub> ≤ 4.0V	10			μs	
V <sub>CC</sub> Slew Rate Power Up	t <sub>R</sub> 4.5V ≥ V <sub>CC</sub> ≥ 4.0V	0			μs	
Expected Data Retention	t <sub>DR</sub>	10			years	9

**WARNING:**

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery back-up mode.

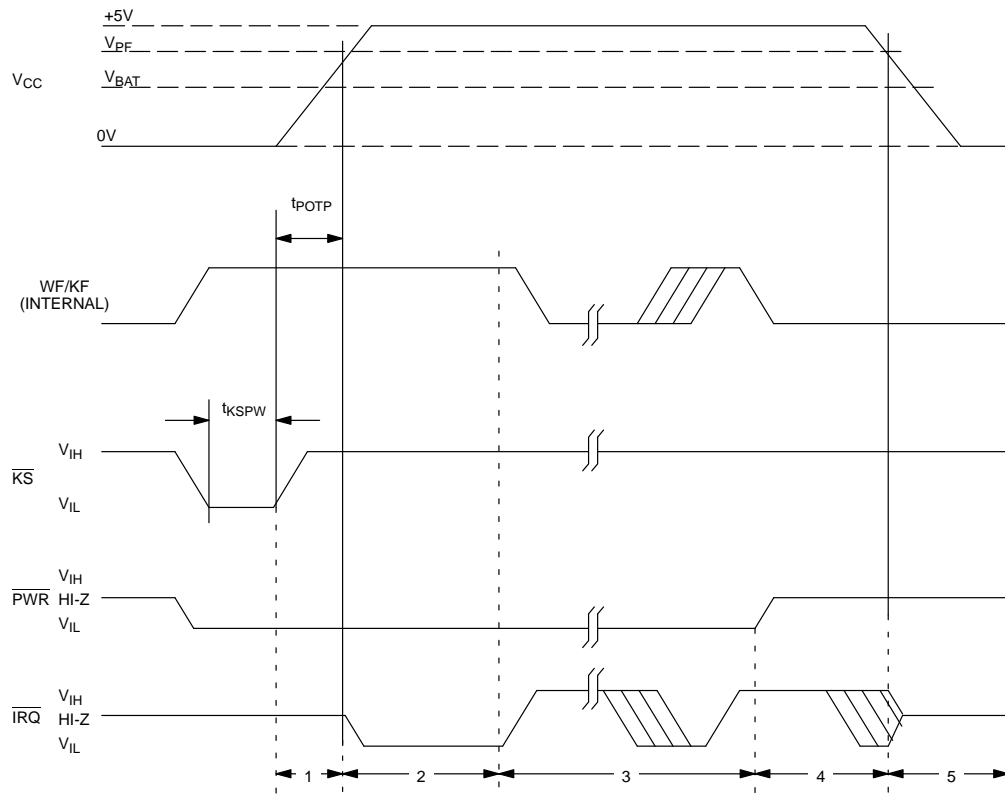
**CAPACITANCE**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>			12	pF	
Output Capacitance	C <sub>OUT</sub>			12	pF	

**WAKE UP/KICKSTART TIMING**(t<sub>A</sub> = 25°C)

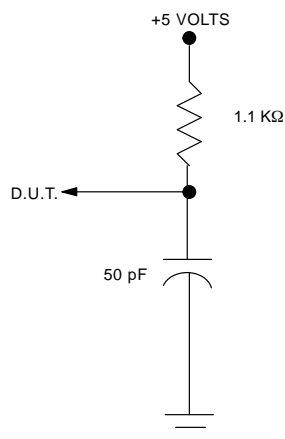
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Kickstart Input Pulse Width	t <sub>KSPW</sub>	2			μs	
Wake up/Kickstart Power On Timeout	t <sub>POTO</sub>	2			seconds	11



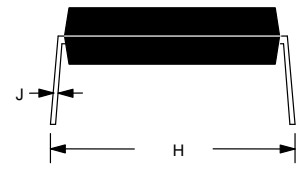
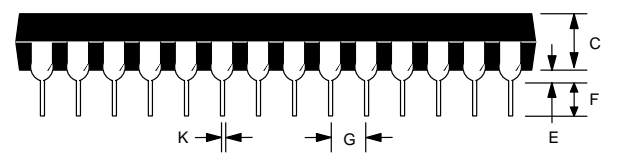
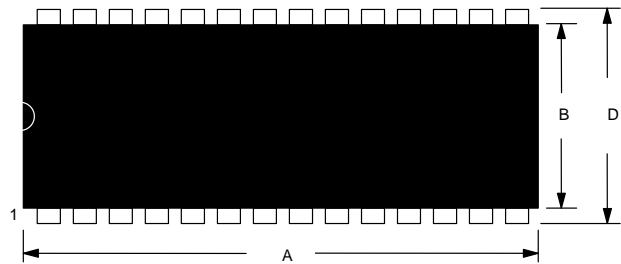
**WAKE UP/KICKSTART TIMING**

**NOTES:**

1. All voltages are referenced to ground.
2. All outputs are open.
3. Applies to the AD0-AD7 pins, and the SQW pin when each is in the high impedance state.
4. The  $\overline{\text{IRQ}}$  and AD0-AD7 pins are open drain.
5. Measured with a load as shown in Figure 5.
6. All other inputs at CMOS levels.
7. Transition current only applies while input is switched from one state to the other. Quiescent input current given by input leakage current specification.
8. Measured with a load as shown in Figure 5.
9. The real-time clock will keep time to an accuracy of  $\pm 1$  minute per month during data retention time for the period of  $t_{DR}$ .
10. Applies to DS1589 only.
11. Wake up/Kickstart timeout generated only when the oscillator is enabled and the countdown chain is not reset.
12. Measurement is dependent upon RC time constant of output load.

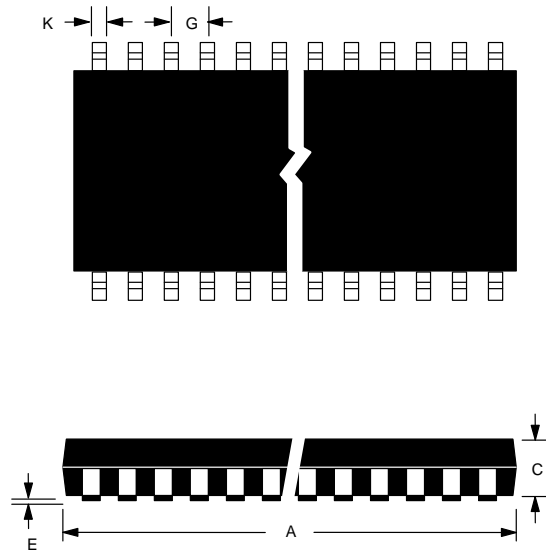
**OUTPUT LOAD Figure 5**

DS1589 28-PIN DIP

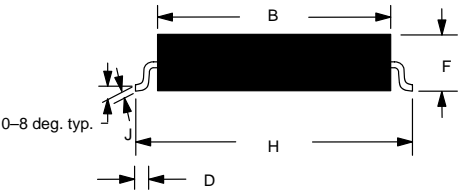


PKG	28-PIN	
	DIM	
A	IN.	MM
	MIN	MAX
B	IN.	MM
	MIN	MAX
C	IN.	MM
	MIN	MAX
D	IN.	MM
	MIN	MAX
E	IN.	MM
	MIN	MAX
F	IN.	MM
	MIN	MAX
G	IN.	MM
	MIN	MAX
H	IN.	MM
	MIN	MAX
J	IN.	MM
	MIN	MAX
K	IN.	MM
	MIN	MAX

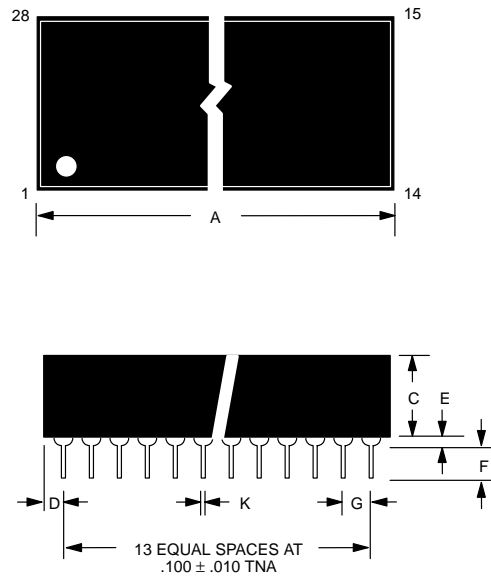
DS1589S 28-PIN SOIC



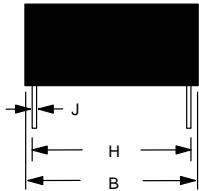
PKG	28-PIN	
DIM	MIN	MAX
A IN. MM	0.706 17.93	0.728 18.49
B IN. MM	0.338 8.58	0.350 8.89
C IN. MM	0.086 2.18	0.110 2.79
D IN. MM	0.020 0.58	0.050 1.27
E IN. MM	0.002 0.05	0.014 0.36
F IN. MM	0.090 2.29	0.124 3.15
G IN. MM	0.050 1.27	BSC
H IN. MM	0.460 11.68	
J IN. MM	0.006 0.15	0.013 0.33
K IN. MM	0.014 0.36	0.020 0.51



DS1593 28-PIN 740 MIL MODULE



PKG	28-PIN	
	DIM	
	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.350	0.375
MM	8.89	9.52
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.110	0.140
MM	2.79	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



NOTE: PINS 2, 3, 19 AND 23 ARE MISSING BY DESIGN.