Chapter 1
Introduction

The P55TV2 mainboard is a high performance system hardware based on Intel Pentium® processor and is equipped with four PCI slots, four standard ISA slots, Ultra I/O controller and dual port PCI-IDE connectors for the future expansion. The hardware dimension is 220mm x 260mm with a four-layer-design technology.

Specification

- Intel 82430VX PCIset chipset.
- Intel **Pentium**® Processor, Pentium® Processor with MMX™ technology, AMD K5/K6 and Cyrix M1/M2 operating at **90 ~ 266 MHz** with **321 ZIF socket 7** provides scalability to accept faster processors in the future.
- Supports up to 128 MegaBytes of DRAM (a minimum of 8 MB) on board (72 Pins SIMM x 4, 168 Pins DIMM x 2). BIOS will autometically detect and configure FP DRAM, EDO DRAM and SDRAM (Refer to Chapter 2-3, System Memory Configuration).
- Supports Onboard Pipelined Burst synchronous L2 **Write Back** Cache. The cache memory combination can be 256KB/512KB (32KB*32 and 64KB*32 SRAM, respectively).
- Supports four 16 bits ISA slots, four 32 bits PCI slots, and provides two independent high performance PCI IDE interfaces capable of supporting **PIO Mode 3 and Mode 4** devices. The **P55TV2** supports four PCI Bus Masters and a jumperless PCI INT# control scheme which reduces configuration confusion when plugging in PCI I/O controller card(s).
- Supports **AT API** (e.g., **CD-ROM**) devices on both IDE interfaces.
- Supports 1 floppy port, 1 parallel port (EPP,ECP port), 2 serial ports (16550 Fast UART compatible) and 2 USB ports.
- Supports a **PS/2** style mouse and standard AT style keyboard connectors.
- Supports Award Plug & Play BIOS. The BIOS is stored in Flash EPROM form. It provides better upgradability for the system.
- Supports CPU Hardware sleep and SMM (System Management Mode).
- **The P55TV2** utilizes a Lithium battery which provides environmental protection and longer battery life.

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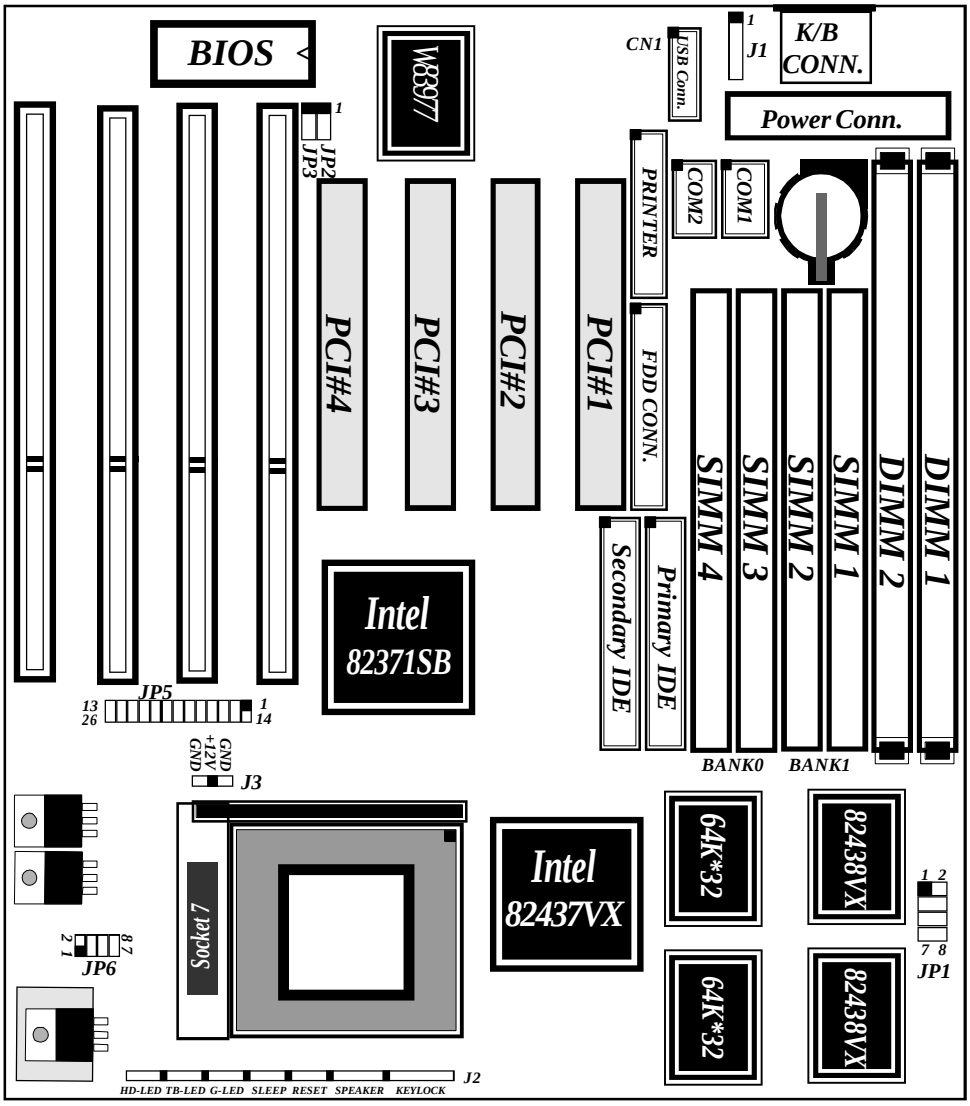
P55TV2 Layout



Note : ■ Means Pin 1

Figure 1-1

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Chapter 2
Hardware design

2-1 Overview

The P55TV2 is designed with Intel 82430VX PCIset chipset which is developed by INTEL Corporation to fully support Pentium® Processor PCI/ISA system. The Intel 82430VX PCIset chipset provides increased integration and improved performance designs. The chipset provides an integrated IDE controller with two high performance IDE interfaces for up to four IDE devices (hard devices, CD-ROM device, etc). The PnP Ultra I/O controller provides the standard PC I/O functions including: floppy interface, two 16 Byte FIFO serial ports and one EPP/ECP capable parallel port. The **P55TV2** layout is shown in the previous page for user's reference. **Care must be taken** when inserting memory modules, inserting CPU or even plugging PCI card into the associated slots to avoid damaging any circuits or sockets on board. A cooling fan is strongly recommended when installing P54C/P54CTB/P55C/K5/K6/6x86/6x86L processor due to possible overheat.

The P55TV2 supports a minimum of 8MB of System Memory and a maximum of 128MB while L2 Cache can be 256KB/512KB synchronous SRAM Onboard to increase system performance (Refer to **Page 2-10 Cache Memory Configuration** for the details).

The P55TV2 supports standard Fast Page, EDO (Extended Data Out or Hyper Page Mode) or synchronous DRAM.**The P55TV2** provides four 72-pin SIMM and two 168-pins DIMM sites for memory expansion. Each socket supports 1M x 32(4MB), 2M x 32(8MB), 4M x 32(16MB), and 8M x 32(32MB) single-sided or double-sided memory modules. The memory timing requires 70 ns Fast page devices or 60 ns EDO DRAM. **Memory parity generation and checking are not supported.** (DRAM Modules may be parity[x 36] or non-parity[x 32].

The P55TV2 supports **Onboard two PCI IDE** connectors, and BIOS detects IDE harddisk type automatically.

The P55TV2 supports Award Plug & Play BIOS for ISA and PCI cards. The BIOS is located in Flash EPROM which is a technology to easily revise/upgrade BIOS through software.

The P55TV2 has been designed with Baby AT form-factor. The mainboard layout is shown in Figure 1-1.

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2-2 Connectors and Jumpers

This section describes all of the connectors and jumpers built into the mainboard. Please refer to **Figure 1-1** (page 1-2) for the location of each connector and jumper. The following figures shows connector and jumper setting. means connecting to pins 1&2 and means connecting to pins 2&3. means setting jumpers with two pins open, and means setting jumpers with two pins close.

J2

KeyLock - Keyboard lock switch & Power LED connector.
1.Power LED(+)
2.N/C
3.GND
4.Keylock
5.GND

Speaker - connect to the system's speaker for beeping
7. Speaker
8. N/C
9. GND
10. VCC

Reset - Closed to restart system

Sleep/Resume switch : Closed to enter sleep mode
(A keystrobe or mouse movement will instantly "wake up".)

Power Saving LED indicator - LED ON when system is in any saving mode

Turbo LED indicator - LED ON when higher speed is selected

Harddisk LED indicator - LED ON when Onboard PCI IDE Harddisks activites

J3

The Power Supply (+12V) of the CPU Cooling FAN
1.GND
2.+12V
3.GND

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J1

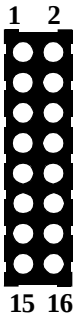
PS/2 MOUSE CONNECTOR

1 . Data (Red Wire)
2 . Clock (Blue Wire)
3 . GND (Green)
4 . NC
5 . VCC (Yellow)

J4

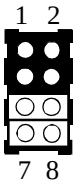
IrDA/ASK IR CONNECTOR

1 . VCC
2 . NC
3 . IRRX
4 . GND
5 . IRTX

CN1 

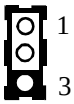
USB CONNECTOR

Reserved for USB port Adapter
(refer to APPENDIX B:I/O Connectors)

JP1 

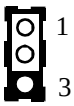
DIMM Working Voltage Selection

1-2, 3-4 : 5V
5-6, 7-8 : 3.3V (Default)
(Refer to 2-4 : Memory Configuration for the detail)

JP2 

EPROM BIOS Selection

1-2 : 5V Flash ROM (Default)
2-3 : 12V Flash ROM

JP3 

BIOS Flash Mode Selection

1-2 : Normal operation (Default)
2-3 : BootBlock Flash

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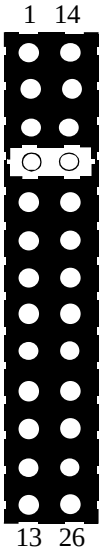
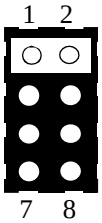
JP5 : CPU Clock Rate Selection (Single Jumper)



CPU / JP5	Pentium PentiumMMX AMD K5 / K6	Bus Freqency x Multiplier	Cyrix 6x86(L) / 6x86MX IBM 6x86(L) / 6x86MX
1-14	90MHz	60MHz x 1.5	
2-15	100MHz	66MHz x 1.5	
3-16	120MHz	60MHz x 2	6x86/L-PR150
4-17	133MHz	66MHz x 2	6x86/L/MX-PR166
5-18	150MHz	60MHz x 2.5	6x86MX-PR166
6-19	166MHz	66MHz x 2.5	6x86MX-PR200
7-20	188MHz	75MHz x 2.5	* 6x86MX-PR233
8-21	200MHz	66MHz x 3	* 6x86MX-PR233
9-22	225MHz	75MHz x 3	* 6x86MX-PR266
10-23	233MHz	66MHz x 3.5	* 6x86MX-PR266
11-24	* 266MHz	66MHz x 4	
12-25	110MHz	55MHz x 2	6x86/L-PR133
13-26	150MHz	75MHz x 2	6x86/L/MX-PR200

* ***These jumper settings are reserved for the future CPU versions. when the future CPUversions are ready and suitable for this mainboard, these jumper settings will be correctly updated.***

JP6 : CPU Vcore voltage selection : For Pentium MMX Processor, AMD K6 and Cyrix 6x86L/MX



1-2 : 2.8V for Pentium MMX Processor and Cyrix 6x86L
3-4 : 2.9V for AMD K6-PR2-166/200 and Cyrix 6x86MX
5-6 : 3.2V for AMD K6-PR2-233/266
7-8 : 3.5V for Pentium, AMD K5 and Cyrix 6x86

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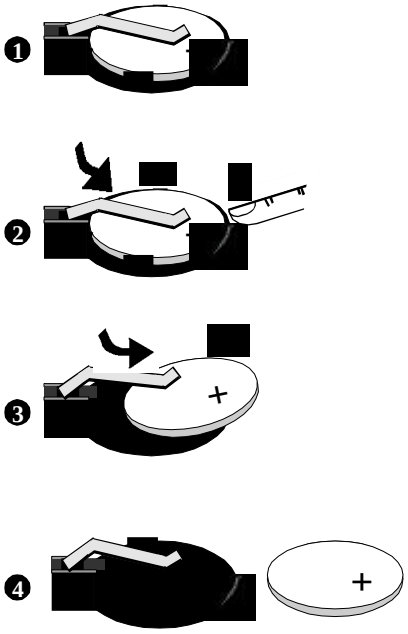
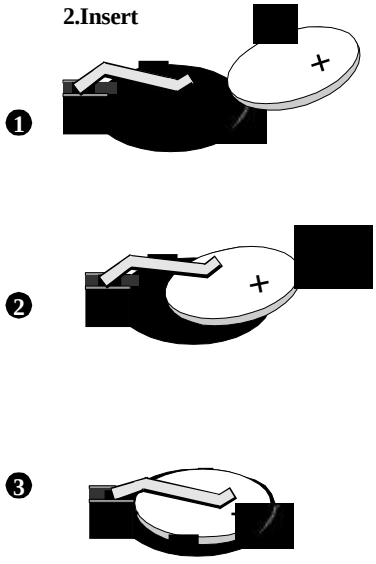
2-3 Real Time Clock Battery Replacement

The battery can be replaced with an equivalent coin lithium battery such as Sanyo / Panasonic CR2032. Please follow the following steps to replace the battery.

1.Remove



2.Insert



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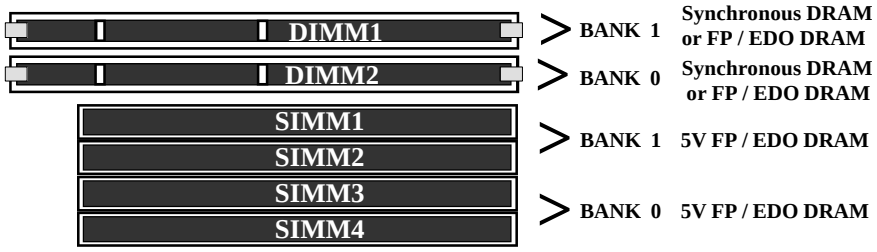
2-4 System Memory Configuration

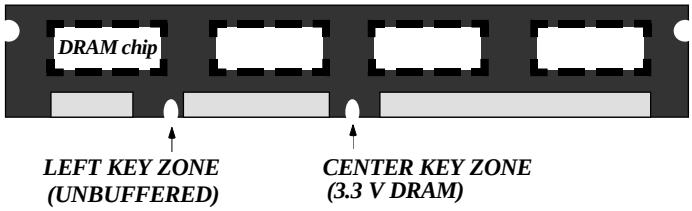
The **P55TV2** supports different types of settings for the system memory. The memory configuration does not need jumper or hardware setting. The following tables provide all possible memory combinations.



SIMM3,4 (BANK 0)	SIMM1,2 (BANK 1)	DIMM2 (BANK 0)	DIMM1 (BANK1)	STATUS
Installed	None	None	None	OK
None	Installed	None	None	OK
None	None	Installed	None	OK
None	None	None	Installed	OK
Installed	Installed	None	None	OK
None	Installed	Installed	None	OK
Installed	None	None	Installed	OK
None	None	Installed	Installed	OK
Installed	None	Installed	None	Not allowed
None	Installed	None	Installed	Not allowed
Installed	Installed	Installed	None	Not allowed
Installed	Installed	Installed	Installed	Not allowed

NOTE: 1.The P55TV2 supports both Fast Page DRAM and EDO DRAM SIMMs,but they cannot be used in the same memory bank.

2.The ***KEY ZOOM*** of the DIMM socket is ***3.3V/Unbuffered***



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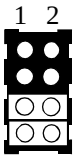
The **P55TV2** supports two 168-pin DIMM module sockets to extpand system memory size.You can install (3.3V/Unbuffered) Fast Page, EDO or Synchronous DRAM. Besides, to support 5V FP and EDO DRAM with DIMM socket, ***the P55TV2 provides JP1 to allow user using 3.3V/Unbuffered DIMM module with 5V FP and EDO DRAM chips***. The setting of the JP1 as follow:

JP1



DIMM Working Voltage Selection
1-2, 3-4 : For 5V FP and EDO DRAM
5-6, 7-8 : For 3.3V FP, EDO and Synchronous DRAM

When you plug a DIMM module into a 168-pin dual readout socket, you must make sure that the key zoom of the DIMM module is 3.3V/Unbuffered and supports Intel Pentium® Processor System.

Memory Configuration Table 1

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
4M x 2 (8 MB)	Empty	Empty	Empty	8MB
4M x 2 (8 MB)	4M x 2 (8 MB)	Empty	Empty	16MB
4M x 2 (8 MB)	8M x 2 (16 MB)	Empty	Empty	24MB
4M x 2 (8 MB)	16M x 2 (32 MB)	Empty	Empty	40MB
4M x 2 (8 MB)	32M x 2 (64 MB)	Empty	Empty	72MB
8M x 2 (16 MB)	Empty	Empty	Empty	16MB
8M x 2 (16 MB)	4M x 2 (8 MB)	Empty	Empty	24MB
8M x 2 (16 MB)	8M x 2 (16 MB)	Empty	Empty	32MB
8M x 2 (16 MB)	16M x 2 (32 MB)	Empty	Empty	48MB
8M x 2 (16 MB)	32M x 2 (64 MB)	Empty	Empty	80MB
16M x 2 (32 MB)	Empty	Empty	Empty	32MB
16M x 2 (32 MB)	4M x 2 (8 MB)	Empty	Empty	40MB
16M x 2 (32 MB)	8M x 2 (16 MB)	Empty	Empty	48MB
16M x 2 (32 MB)	16M x 2 (32 MB)	Empty	Empty	64MB
16M x 2 (32 MB)	32M x 2 (64 MB)	Empty	Empty	96MB
32M x 2 (64 MB)	Empty	Empty	Empty	64MB
32M x 2 (64 MB)	4M x 2 (8 MB)	Empty	Empty	72MB
32M x 2 (64 MB)	8M x 2 (16 MB)	Empty	Empty	80MB
32M x 2 (64 MB)	16M x 2 (32 MB)	Empty	Empty	96MB
32M x 2 (64 MB)	32M x 2 (64 MB)	Empty	Empty	128MB

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Memory Configuration Table 2

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
Empty	Empty	8MB	Empty	8MB
Empty	Empty	8MB	8MB	16MB
Empty	Empty	8MB	16MB	24MB
Empty	Empty	8MB	32MB	40MB
Empty	Empty	8MB	64MB	72MB
Empty	Empty	16MB	Empty	16MB
Empty	Empty	16MB	8MB	24MB
Empty	Empty	16MB	16MB	32MB
Empty	Empty	16MB	32MB	48MB
Empty	Empty	16MB	64MB	80MB
Empty	Empty	32MB	Empty	32MB
Empty	Empty	32MB	8MB	40MB
Empty	Empty	32MB	16MB	48MB
Empty	Empty	32MB	32MB	64MB
Empty	Empty	32MB	64MB	96MB
Empty	Empty	64MB	Empty	64MB
Empty	Empty	64MB	8MB	72MB
Empty	Empty	64MB	16MB	80MB
Empty	Empty	64MB	32MB	96MB
Empty	Empty	64MB	64MB	128MB

Memory Configuration Table 3

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
Empty	Empty	8MB	Empty	8MB
Empty	4M x 2 (8 MB)	8MB	Empty	16MB
Empty	8M x 2 (16 MB)	8MB	Empty	24MB
Empty	16M x 2 (32 MB)	8MB	Empty	40MB
Empty	32M x 2 (64 MB)	8MB	Empty	72MB
Empty	Empty	16MB	Empty	16MB
Empty	4M x 2 (8 MB)	16MB	Empty	24MB
Empty	8M x 2 (16 MB)	16MB	Empty	32MB
Empty	16M x 2 (32 MB)	16MB	Empty	48MB
Empty	32M x 2 (64 MB)	16MB	Empty	80MB

Table 3(CONT.)

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Memory Configuration Table 3 (CONT.)

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
Empty	Empty	32MB	Empty	32MB
Empty	4M x 2 (8 MB)	32MB	Empty	40MB
Empty	8M x 2 (16 MB)	32MB	Empty	48MB
Empty	16M x 2 (32 MB)	32MB	Empty	64MB
Empty	32M x 2 (64 MB)	32MB	Empty	96MB
Empty	Empty	64MB	Empty	64MB
Empty	4M x 2 (8 MB)	64MB	Empty	72MB
Empty	8M x 2 (16 MB)	64MB	Empty	80MB
Empty	16M x 2 (32 MB)	64MB	Empty	96MB
Empty	32M x 2 (64 MB)	64MB	Empty	128MB

Memory Configuration Table 4

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
Empty	Empty	Empty	8MB	8MB
4M x 2 (8 MB)	Empty	Empty	8MB	16MB
8M x 2 (16 MB)	Empty	Empty	8MB	24MB
16M x 2 (32 MB)	Empty	Empty	8MB	40MB
32M x 2 (64 MB)	Empty	Empty	8MB	72MB
Empty	Empty	Empty	16MB	16MB
4M x 2 (8 MB)	Empty	Empty	16MB	24MB
8M x 2 (16 MB)	Empty	Empty	16MB	32MB
16M x 2 (32 MB)	Empty	Empty	16MB	48MB
32M x 2 (64 MB)	Empty	Empty	16MB	80MB
Empty	Empty	Empty	32MB	32MB
4M x 2 (8 MB)	Empty	Empty	32MB	40MB
8M x 2 (16 MB)	Empty	Empty	32MB	48MB
16M x 2 (32 MB)	Empty	Empty	32MB	64MB
32M x 2 (64 MB)	Empty	Empty	32MB	96MB
Empty	Empty	Empty	64MB	64MB
4M x 2 (8 MB)	Empty	Empty	64MB	72MB
8M x 2 (16 MB)	Empty	Empty	64MB	80MB
16M x 2 (32 MB)	Empty	Empty	64MB	96MB
32M x 2 (64 MB)	Empty	Empty	64MB	128MB

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Memory Configuration Table 5

SIMM3,4(Bank0)	SIMM1,2(Bank1)	DIMM2(Bank0)	DIMM1(Bank1)	TOTAL
4M x 2 (8 MB)	4M x 2 (8 MB)	8MB	8MB	32MB
4M x 2 (8 MB)	4M x 2 (8 MB)	8MB	32MB	56MB
4M x 2 (8 MB)	4M x 2 (8 MB)	32MB	32MB	72MB
16M x 2 (32 MB)	16M x 2 (32 MB)	8MB	8MB	80MB
16M x 2 (32 MB)	16M x 2 (32 MB)	8MB	32MB	104MB
16M x 2 (32 MB)	16M x 2 (32 MB)	32MB	32MB	128MB

Note : 1, Assume all DRAM and SDRAM in Table 5 are **single-side.**

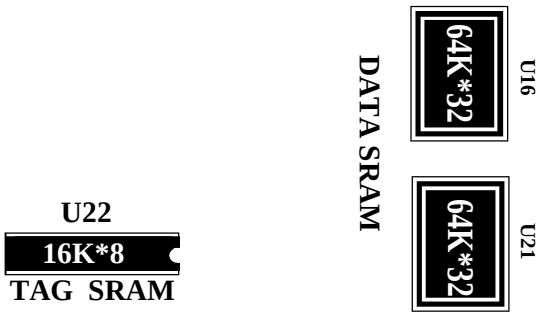
2, The P55TV2 Supports and extends many memory configurations on its 4 SIMM and 2 DIMM sites. The memory size of any configuration can be combined flexibly. The above tables only list the basic memory configurations for your reference. Many configurations are not listed, you may use other configurations not listed on the above. BIOS will detect your memory configuration automatically.

3, The 70ns Fast Page Mode or 60ns EDO DRAM is necessary.

4, **Usually, the DIMM2 and SIMM3&4 occupy the same memory block, Bank 0. They cannot be installed at the same time. Likewise, the DIMM1 and SIMM1&2 occupy the same memory block, Bank1. They cannot be installed at the same time either. However with a special design to expand memory, the P55TV2 allows you to upgrade single-side DRAM at DIMM2 (Bank0) and DIMM1 (Bank1), if you use single-side DRAM at the SIMM3&4 and SIMM1&2.**
Regarding single-side or double-side DRAM/SDRAM, please contact your DRAM/ SDRAM suppliers for the details,

2-5 Cache Memory Configuration

The second level (L2) cache is installed in the mainboard to increase the system performance. The **P55TV2** supports 512KB cache (piplined burst SRAM).



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2-6 Integrated PCI Bridge

The **P55TV2** utilizes **Intel's 430VX PCIset** chipset to support Intel Pentium® Processor PCI/ISA system. The Intel 82430VX PCIset chipset consists of one 82437VX system controller (TVC), two 82438VX Data Path (TDP) devices, and one 82371SB PCI ISA/IDE Accelerator (PIIX3) bridge chip. It provides an interface which translates CPU cycle into PCI bus cycle and PCI burst read/write capability. In addition, it provides high performance PCI arbiter or supports four PCI Masters, Rotating Priority Mechanism, and Hidden Arbitration Scheme Minimizes Arbitration Overhead. The 82371SB(PIIX3) supports PCI Specification Revision 2.1 Compliant and contains a Universal Serial Bus interface with both host and hub control functions. The P55TV2 reserves USB connector to provide two USB ports for serial transfer at 12 or 1.5 Mbit/sec. This will supports legacy keyboard and mouse software with USB-Base Keyboard and mouse.

There are four interrupts in each PCI slot : INTA#, INTB#, INTC#, and INTD#, since the **P55TV2** adapts the PCI auto-configuration with the system BIOS Setup utility. When the system is turned on after adding a PCI add-in card, the BIOS automatically configure interrupts, DMA channels, I/O space, and other paramaters. You do not have to configure jumpers or worry about potential resource conflicts. Because PCI cards use the same interrupt resource as ISA cards, you must specify the interrupts used by ISA add-in cards in the BIOS Setup utility.

If a "Legacy card" (such as paddle card and cable) is plugged into the ISA slot the following modifications in the **ROM SETUP UTILITY** become necessary. First, enter **PCI CONFIGURATION SETUP** utility from **ROM SETUP UTILITY** main menu to set the "**PCI IDE IRQ MAP TO** : **ISA**".

Second, enter **CHIPSET FEATURES SETUP UTILITY** from **ROM SETUP UTILITY** main menu and set the "**Onboard Primary PCI IDE: Disabled** and **Onboard Secondary PCI IDE: Disabled**." When you plugg the PCI/ISA IDE card into the system, You should **Disabled Onboard Primary and Secondary PCI IDE** from **CHIPSET FEATURES SETUP UTILITY** too.

you can set the system interrupt request (IRQ) on some "Legacy cardswhich have no paddle card and cable" (refer to user's manual of the card) to a proper system IRQ level (In general, the card's Primary is assigned to INTA and Secondary is assigned to INTB). If the card is plugged into slot 1(marked PCI#1), you cannot use second slot (marked PCI#2) because the Secondary INT signal takes INTB from the slot (Refer to Page 3-12 for circuit diagram). The user then enters **PCI CONFIGURATION SETUP** utility from **ROM SETUP UTILITY** main menu and sets the "**PCI IDE IRQ MAP TO** : **PCI-Slot 1**" (depend on the slot # where the Legacy card is plugged).

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Chapter 3
AWARD BIOS Setup

Award's ROM BIOS provides a built-in Setup program which allows user to modify the basic system configuration and hardware parameters. The modified data will be stored in a battery-backed CMOS RAM so data will be retained even when the power is turned off. In general, the information saved in the CMOS RAM stay unchanged unless there is a configuration change in the system, such as a hard drive replacement or a new device installment.

It is possible for the CMOS battery to fail. This will cause data lose in CMOS only.If this does happen you will need to reconfigure your configuration parameters.

To enter Setup Propgram

Power on the computer and press <**Del**> key immediately . This will bring you into BIOS **CMOS SETUP UTILITY**.

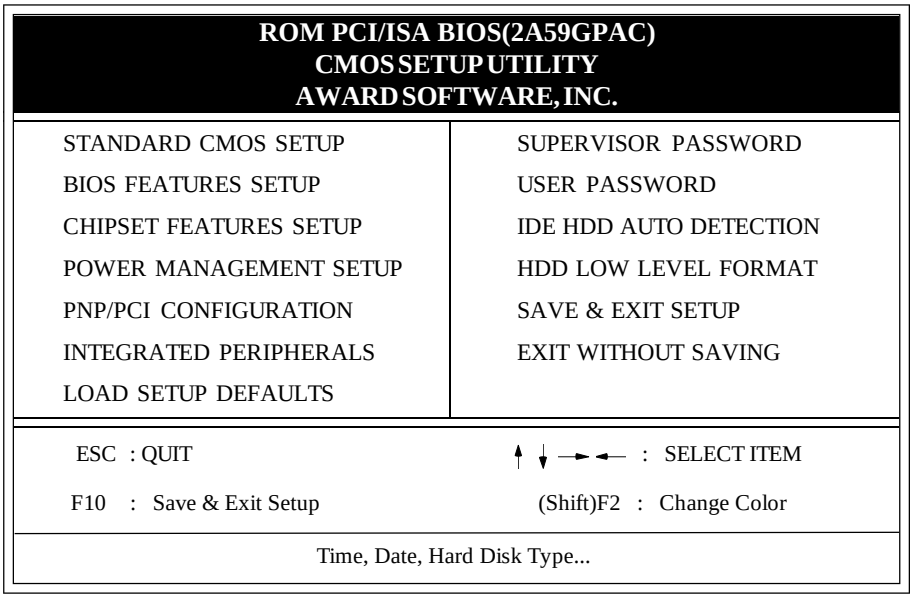

Figure 3-1 CMOS SETUP UTILITY

The menu displays all the major selection items. Select the item you need to reconfigure. The selection is made by moving cursor (press any direction key) to the item and press the 'Enter' key. An on-line help message is displayed at the bottom of the screen as the cursor is moving to various items which provides a better understanding of each function. When a selection is made, the menu of selected item will appear so the user can modify associated configuration parameters.

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3-1 STANDARD CMOS SETUP

Choose "**STANDARD CMOS SETUP**" in the **CMOS SETUP UTILITY** Menu (Fig.3-1). The **STANDARD CMOS SETUP** allows user to configure system setting such as the current date and time, type of hard disk drive installed, floppy drive type, and display type. Memory size is auto-detected by the BIOS and displayed for your reference. When a field is highlighted (use direction keys to move cursor and <Enter> key to select), the entry in the field will be changed by pressing <PgDn> or <PgUp> keys or user can enter new data directly from the keyboard.

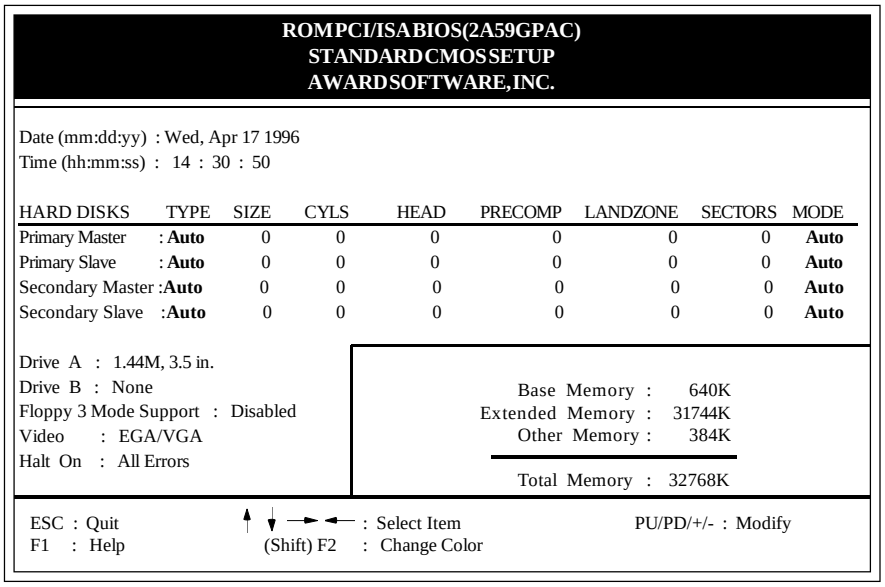

Figure 3-2 STANDARD CMOS SETUP

NOTE: If hard disk Primary Master/Slave and Secondary Master/Slave use Auto, then the hard disk size and model will be auto-detected.

NOTE: The "**Halt On :**" field is to determine when to halt the system by the BIOS if an error occurrs.

3-2 BIOS FEATURES SETUP

Selecting the "**BIOS FEATURES SETUP**" option in the **CMOS SETUP UTILITY** menu allows user to change system related parameters in the displayed menu. This menu shows all of the manufacturer's default values of the P55TV2. Again, user can move the cursor by pressing direction keys and <PgDn> or <PgUp> keys to modify the parameters. Pressing [F1] key to display help message of the selected item.

This setup program also provides 2 convenient ways to load the default parameter data from BIOS [F6] or CMOS [F7] area if the shown data is corrupted. This provides the system a capability to recover from any possible error.

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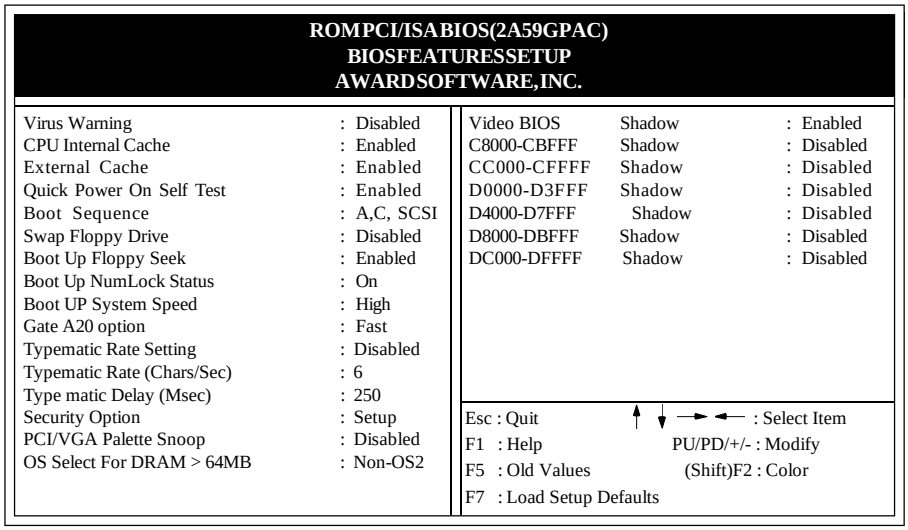

Figure 3-3 BIOS FEATURES SETUP

Note: The **Security Option** contians "**setup**" and "**system**". The "**setup**" indicates that the password setting is for CMOS only while the "**system**" indicates the password setting is for both CMOS and system boot up.

- **Virus Warning:** This category flashes on the screen. During and after the system boots up, any attempts to write to the boot sector or partition table of the hard disk drive will halt the system and an error message will appear. You should then run an anti-virus program to locate the virus. Keep in mind that this feature protects only the boot sector, not the entire hard drive. Default value is Disabled

  ***Enabled* :** Activate automatically when the system boots up causing a warning message to appear when any attempts to access the boot sector or the hard disk partition table.

  ***Disabled*:** No warning message to appear when any attempts to access the boot sector or the hard disk partition table.

- **CPU Internal Cache / External Cache:** These two categories speed up memory access. However, it depends on CPU/chipset design. The default value is Enabled. If your CPU is without Internal Cache then the item "CPU Internal Cache" will not show.

  ***Enabled*:** Enable cache.

  ***Disable* :** Disable cache.

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- **Quick Power On Self Test:** This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.
  Enabled **:** Enable quick POST.
  Disabled**:** Normal POST.

- **Boot Sequence:** This category determines which drive is searched for first for the O/S(Operating System). Default value is A,C.
  A,C **:** System will first search for the floppy disk drive then the hard disk drive.
  C,A **:** System will first search for the hard disk drive then the floppy disk drive.
  CDROM,C,A: System will first search for the CDROM drive (If the CDROM has a bootable CD title.) and second search for the hard disk drive then the flopp disk drive.
  C,CDROM,A: System will first search for the hard disk driver and second search for the CDROM drive (If the CDROM has a bootable CD title.) then the floppy disk drive.

- **Swap Floppy Drive:** This will swap your physical drive letters A&B if you are using two floppy disks. Default value is Disabled.
  Enabled **:** Floppy A & B will be swapped under the O/S.
  Disabled**:** Floppy A & B will be not swapped.

- **Boot Up Floppy Seek:** During POST,BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. Only 360K type is 40 tracks while 760K, 1.2M and 1.44M are all 80 tracks. The default value is Enabled.
  Enabled **:** BIOS searches for the floppy disk drive to determine if it is 40 or 80 tracks. Note that BIOS cannot tell from 720K, 1.2M or 1.44M drive type as they are all 80 tracks.
  Disabled**:** BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

- **Boot Up NumLock Status:** The default value is On.
  On **:** Keypad is number keys.
  Off **:** Keypad is arrow keys.

- **Boot UP System Speed**: Select the default system speed. The system will run at the selected speed after the system boots.
  High: Set the speed to high.
  Low : Set the speed to low.

- **Gate A20 Option:** This refers to the way the system addresses memory above 1MB (extended memory). The default value is Fast.
  Normal **:** The A20 signal is controlled by keyboard controller or chipset hardware.
  Fast **:** The A20 signal is controlled by Port 92 or chipset specific method.

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- **Typematic Rate Setting:** This determines the typematic rate.
  Enabled **:** Enable typematic rate and typematic delay programming.
  Disabled**:** Disable typematic rate and typematic delay programming. The system BIOS will use default value of these 2 items and the default is controlled by keyboard.

- **Typematic Rate(Chars/Sec):**

6 : 6 characters per second.	**8 : 8 characters per second.**
10: 10 characters per second.	**12: 12 characters per second.**
15: 15 characters per second.	**20: 20 characters per second.**
24: 24 characters per second.	**30: 30 characters per second.**

- **Typematic Delay(Msec):** When holding a key, the time between the first and second character displayed is typematic delay.
  250 : 250msec.
  500 : 500 msec.
  750 : 750 msec.
  1000: 1000 msec.

- **Security Option:** This category allows you to limit access to the system and Setup, or just to Setup. The default value is Setup.
  System**:** The system will not boot and access to Setup if the correct password is not entered at the prompt.
  Setup **:** The system will boot, but the access to Setup will be denied if the correct password is not entered at the prompt.

- **PCI/VGA Palette Snoop:** This filed controls the ability of a primary PCI VGA controller to share a common palette (when a snoop write cycles) with an ISA video card. The default value is Disabled.
  Enabled: If an ISA card connects to a PCI VGA card via the VESA connector and the ISA card connects to VGA monitor and that ISA card uses the RAMDAC of PCI card, the PCI/VGA Palette Snoop is enabled.
  Disabled: Disable the VGA card Palette snoop function.

- **Video BIOS Shadow:** It determines whether video BIOS will be copied to RAM, however, it is optional from chipset design. Video Shadow will increase the video speed.
  Enabled **:** Video shadow is enabled.
  Disabled**:** Video shadow is disabled.

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- **C8000 - CBFFF Shadow :**
  CC000 - CFFFF Shadow:
  D0000 - D3FFF Shadow:
  D4000 - D7FFF Shadow:
  D8000 - DBFFF Shadow:
  DC000 - DFFFF Shadow:

  These categories determine whether other expansion card optional ROM will be copied to RAM by 16K byte or 32K byte perunit and the size depends on chipset. If you install other expansion cards with ROMs on them, you will need know which addresses the ROMs used to shadow themselves specifically.
  ***Enabled* :** Optional shadow is enabled.
  ***Disabled*:** Optional shadow is disabled.

3-3 CHIPSET FEATURES SETUP

Choose the "**CHIPSET FEATURES SETUP**" in the **CMOS SETUP UTILITY** menu to display the following menu.

ROM PCI/ISA BIOS (2A59GPAC)
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	Peer Concurrency	: Enabled
DRAM Timing	: 60 ns	Chipset NA# Asserted	: Enabled
		Passive Release	: Enabled
DRAM RAS# Precharge Time	: 3	Delayed Transaction	: Disabled
DRAM R/W Leadoff Timing	: 6		
Fast RAS to CAS Delay	: 3		
DAM Read Burst (EDO/FP)	: x222/x333		
DRAM Write Burst Timing	: x222		
Fast MA to RAS# Delay CLK	: 1		
Fast EDO Path Select	: Disabled		
Refresh RAS# Assertion	: 4 Clks		
ISA Bus Clock	: PCICLK/4		
Pipline Cache Timing	: Fastest		
System BIOS Cacheable	: Disabled		
Video BIOS Cacheable	: Enabled		
8 Bit I/O Recovery Time	: 1		
16 Bit I/O Recovery Time	: 1		
Memory Hole At 15M-16M	: Disabled		

Esc : Quit ↑ ↓ →← : Select Item
F1 : Help PU/PD/+/- : Modify
F5 : Old Values (Shift)F2 : Color
F7 : Load Setup Defaults

Figure 3-4 CHIPSET FEATURES SETUP

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- **Auto Configuration:** This Category allows you to set the DRAM timing. The default value is Enabled. When disabled this field, you can select the different DRAM timings supported by chipsets.

  Note: When you insert slower memory modules in the system and set a faster timing, maybe, the system will hang up.

- **DRAM Timing:** The default value is 60ns.
  60ns **:** 2 (faster) Burst Wait State, for 60~70ns Fast Page Mode/EDO DRAM.
  70ns **:** 3 (slower) Burst Wait State, for 70ns Fast Page Mode/EDO DRAM.

- **Video BIOS Cacheable:** The default value is Enabled.
  Enabled **:** Enable the Video BIOS Cacheable to speed up the VGA Performance.
  Disabled**:** Disable the Video BIOS Cacheable function.

- **8/16 Bit I/O Recovery Time:** The default value is 1.
  8 Bit I/O Recovery Time**:** This field defines the recovery time from 1 to 8 for 8-bit I/O.
  16 Bit I/O Recovery Time**:** To define the recovery time from 1 to 4 for 16-bit I/O.
- **Memory Hole at 15M-16M:** The default value is Disabled.
  Disabled**:** Normal Setting.
  Enabled : enable the main memory (15~16MB) remap to ISA BUS. This feature reserves 15MB to 16MB memory address space to ISA expansion card that specifically requires this setting.

- **Peer Concurrency:** The default value is Enabled.
- **Chipset NA# Asserted:** The default value is Enabled.
- **Passive Release:** The default value is Enabled.
- **Delay Transaction:** The default value is Disabled.

3-4 POWER MANAGEMENT SETUP

Choose the "**POWER MANAGEMENT SETUP**" in the **CMOS SETUP UTILITY** to display the following screen. This menu allows user to modify the power management parameters and IRQ signals. In general, these parameters should not be changed unless it is absolutely necessary.

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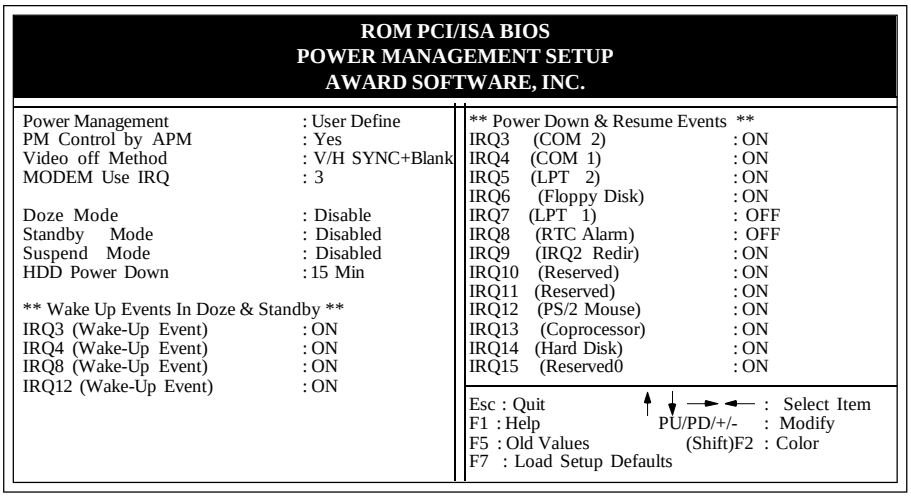

Figure 3-5 POWER MANAGEMENT SETUP

Again, user can move the cursor by pressing direction keys to the field that needs to be modified and press <PgDn> or <PgUp> to alter item selection. You can only change the content of **Doze Mode**, **Standby Mode**, and **Suspend Mode** when the **Power Management** is set to **User Define**'.

Note: When the computer enters the suspend mode (setting the suspend mode valid range from 1 minute up to 1 hour) activated by the BIOS Power Management, you need to RUN a program POWER.EXE under DOS root, or need to add DEVICE=C:\DOS\POWER.EXE in your CONFIG.SYS. This will keep the system time updating normally when the system wake up from the suspend mode. The supend mode for Windows® 95 or windows 3.1x must have windows APM feature installed. Choose "Advanced Power Management" item from "system device". The "system device" field was from "system" icon in the "control panel."

3-4-1 The Description of the Power Management

A. Power Management mode selection :

Disabled : The system operates in NORMAL conditions (Non-GREEN) and the Power Management function is disabled.

Max. saving: This mode will maximize the power saving capability.

Min. saving: This mode will minimize the power saving capability.

User Define: Allows user to define time-out parameters to control the power saving mode. Refer to item B shown below.

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B. Time-out parameters :

HDD Standby
HDD Standby timer can be set from 1 to 15 minute(s).

System Doze
The "System Doze" mode timer starts to count when there is no "PM events" occurred. The valid time-out setting is from 1 minute up to 1 hour.

System Standby
The "Standby" mode timer starts to count when "System Doze" mode timer timed out and no "PM events" occurred. Valid range is from 1 minute up to 1 hour.

System Suspend
This function works only when the Pentium® Procssor is installed. The timer starts to count when "System Standby" mode timer is timed out and no "PM Events" occurred. Valid range is from 1 minute up to 1 hour.

3-4-2 Description of the Green Functions

The P55TV2 supports HDD Power Down, Doze and standby power saving functions when Intel Pentium® Processor is installed. In addition, the suspend function is supported when the J2's sleep (refer to Figure1-1) is closed to enter the green function. The detailed descriptions of these functions are provided in the next page.

HDD Power Down
When system stop reading or writing HDD, the timer starts to count. The system will cut off the HDD power when timer runs out of time. The system will not resume operation until either a read from or a wirte to HDD command is executed again.

Doze Mode
The system hardware will drop down CPU clock from nomal working speed when Doze mode time-out occurs

Standby Mode
When the system standby mode timer times-out, it will enter the standby mode and retain CPU at slow working speed. The screen will be blanked out.

Suspend Mode
When the system suspend timer times-out, the system will enter the suspend mode and the chipset will stop CPU clock immediately. The power consumption in Suspend Mode is lower than in standby mode. The screen is also blanked out.

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PM Events:
AWARD BIOS defines 15 PM Events in the power management mode (Doze, standby & suspend). The user can initialize any PM Events to be "Enable" or "Disable". When the system detects all of the enabled events, do not have any activity. It will start the system Doze timer first if the "Power Management" is not "Disabled". Once the system Doze timer is timed out, it will process doze power saving procedure by starting the system standby timer. When the standby timer run out and all of the "Enabled" events remains silent, the system will enter the standby mode. By now, the system will not only process the standby power saving procedures but also start the system suspend timer. When the suspend timer times out, all of the CPU clock will stop by dropping system clock down to zero and remains this way until any one of the "Enabled" event occurrs.

3-5 PnP/PCI CONFIGURATION

The PnP/PCI configuration program is for the user to modify the PCI/ISA IRQ signals when various PCI/ISA cards are inserted in the PCI or ISA slots.

WARNING : Conflicting IRQs may cause the system to not find cutain devices

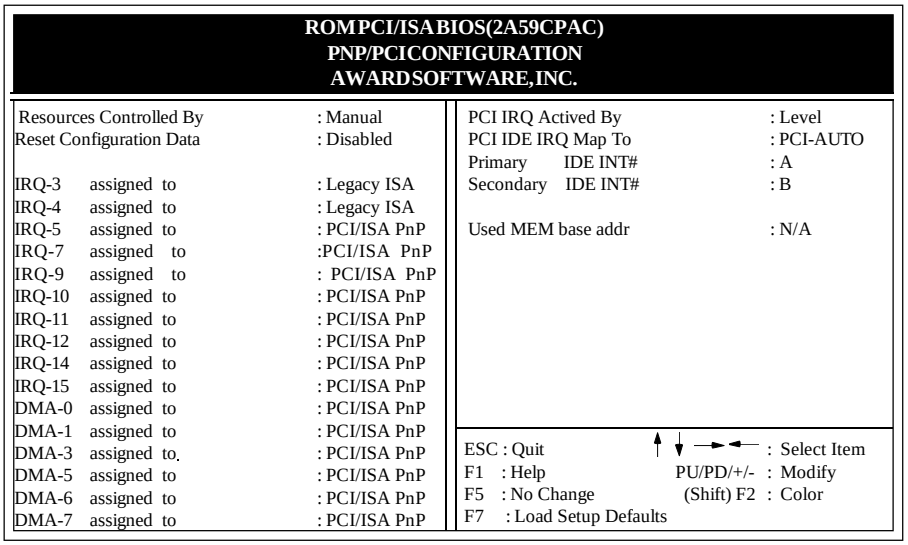

Figure 3-6 PCI CONFIGURATION SETUP

- **Resource Controlled By:** The default value is Manual.
  Manual: The PNP Card's resource will be controlled manually. You can set which IRQ-X and DMA-X are assigned to PCI/ISA PNP or Legacy ISA Cards.
  Auto: If your ISA card and PCI card are all PNP cards, BIOS will assign the inter rupt resource automatically.

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- **Reset Configuration Data:** The default value is Disabled.
  Disabled: Normal Setting.
  Enabled : If you had plugged some Legacuy cards in the system and they were recorded into ESCD(Extended System Configuration Data), you can set this field to Enabled to clear ESCD.

- **PCI IDE IRQ Map To:** The default value is PCI-AUTO

  When you have true PCI card(s) plugged into the system, you will not need to change any thing here in the **SETUP** program. However, if you do not know whether you have true PCI card or not, please refer to your PCI card user's manual for the details.

  When you have a Legacy card (describbed in section 2-6) to be plugged into the system,a proper setting is extremely important or it may cause the system hang. The diagram shown below tells you how the Rotating Priority Mechanism is designed.

- **Used MEM base addr and Used MEM Length : The default value is N/A.**

  The Used MEM base addr (CB00, CC00, D000, D400, D800, DC00)and Used MEM Length (8K, 16K, 32K, 64K)were to support some specific ISA Legacy cards with requested memory space below 1M address. Now with these two functions, users can define where the used memory address is located and its length of the legacy area that is wsed by the legacy device to avoid the memory space confilict. For example, if users select "D000" for "Used MEM base addr" and "16K" for "Used MEM Length," that means the address region D0000H-D3FFFH is occupied by ISA legacy cards, and thus BIOS will not assign this region for PnP/ISA and PCI cards.

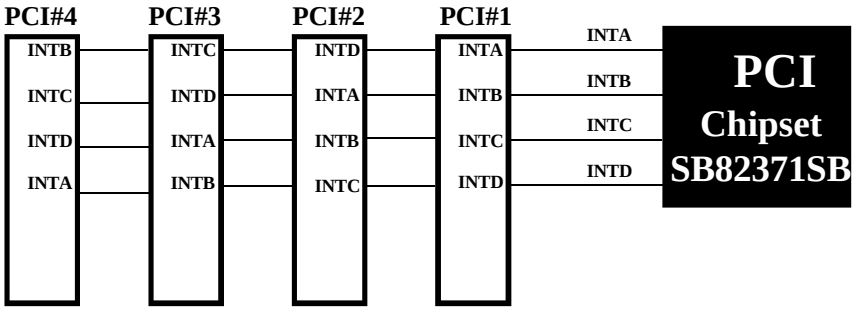

Figure 3-7 The Combination of PCI INT# lines

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3-6 INTEGRATED PERIPHERALS

ROM PCI/ISA BIOS(2A59GPAC)
INTEGRATED PERIPHERALS
WARD SOFTWARE, INC.

IDE HDD Block Mode	: Enabled	Onboard IR Controller	: Disabled
IDE Primary Master PIO	: Auto		
IDE Primary Slave PIO	: Auto		
IDE Secondary Master PIO	: Auto		
IDE Secondary Slave PIO	: Auto		
Onboard Primary PCI IDE	: Enabled		
Onboard Secondary PCI IDE	: Enabled		
PCI Slot IDE 2nd Channel	: Enabled		
USB Controller	: Disabled		
KBC input clock	: Auto		
Onboard FDC Controller	: Enabled		
Onboard Serial Port 1	: Auto		
Onboard Serial Port 2	: Auto		
Onboard Parallel Port	: 378/IRQ7	ESC : Quit	↑ ↓ → ← : Select Item
Parallel Port Mode	: ECP+EPP	F1 : Help	PU/PD/+/- : Modify
ECP Mode Use DMA	: 3	F5 : No Change	(Shift) F2 : Color
Parallel Port EPP Type	: EPP1.9	F7 : Load Setup Defaults	

Note: If you do not use the Onboard IDE connector, then use On-card (PCI or ISA card) IDE connector. You will set Onboard Primary PCI IDE: Disabled and Onboard Secondary PCI IDE: Disabled from CHIPSET FEATURES SETUP UTILITY.
The Onboard PCI IDE cable should be equal to or less than 18 inches (45 cm.).

- **IDE HDD Block Mode:** The default value is Enabled.
  Enabled **:** Enable IDE HDD Block Mode to provide higher HDD transfer rate.
  Disabled**:** Disable IDE HDD Block Mode.

- **PCI Slot IDE 2nd Channel:** The default value is Enabled.
  Enabled **:** Enable secondary IDE port and BIOS will assign IRQ15 for this port.
  Disabled **:** Disable secondary IDE port and IRQ15 is available for other device.

- **Onboard Primary PCI IDE:** The default value is Enabled.
  Enabled **:** Enable Onboard IDE primary port.
  Disabled **:** Disable Onboard IDE primary port, when using On-card (PCI or ISA card) IDE connector.

- **Onboard Secondary PCI IDE:** The default value is Enabled.
  Enabled **:** Enable Onboard IDE secondary port.
  Disabled **:** Disable Onboard IDE secondary port when usingOn-card (PCI or ISA card) IDE connector.

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- **IDE Primary Master PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Primary Master PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Primary Slave PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Primary Slave PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Secondary Master PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Secondary Master PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Secondary Slave PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Secondary Slave PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **Onboard FDC Controller:** The default value is Enabled.
  Enabled **:** Enable the Onboard SMC CHIP's floppy drive interface controller.
  Disabled **:** Disable the Onboard SMC CHIP's floppy drive interface controller. when using On-card ISA FDC's controller.

- **Onboard UART 1:** This field allows the user to sellect the serial port. The default value is 3F8H/IRQ4.
  COM1**:** Enable Onboard Serial port 1 and address is 3F8H/IRQ4.
  COM2**:** Enable Onboard Serial port 1 and address is 2F8H/IRQ3.
  COM3**:** Enable Onboard Serial port 1 and address is 3E8H/IRQ4.
  COM4**:** Enable Onboard Serial port 1 and address is 2E8H/IRQ3.
  Disabled**:** Disable Onboard SMC CHIP's Serial port 1.

- **Onboard UART 2:** This field allows the user to sellect the serial port. The default value is 2F8H/IRQ3.
  COM1**:** Enable Onboard Serial port 2 and address is 3F8H/IRQ4.
  COM2**:** Enable Onboard Serial port 2 and address is 2F8H/IRQ3.
  COM3**:** Enable Onboard Serial port 2 and address is 3E8H/IRQ4.
  COM4**:** Enable Onboard Serial port 2 and address is 2E8H/IRQ3.
  Disabled**:** Disable Onboard SMC CHIP's Serial port 2.

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- **Onboard UART 2 Mode:** The default value is standard. This field allows the User to select the COM2 port that can support a serial Infrared Interface.
  Standard: Support a Serial Infrared Interface IrDA.
  HPSIR: Support a HP Serial Infrared Interface format.
  ASKIR: Support a Sharp Serial Infrared Interface format.

- **Onboard Parallel port:** This field allows the user to sellect the LPT port. The default value is 378H/IRQ7.
  378H **:** Enable Onboard LPT port and address is 378H and IRQ7
  278H **:** Enable Onboard LPT port and address is 278H and IRQ5.
  3BCH **:** Enable Onboard LPT port and address is 3BCH and IRQ7.
  Disabled **:** Disable Onboard SMC CHIP's LPT port.

  NOTE**: Parallel Port address is 378H/3BCH that selects the rounting of IRQ7 for LPT1. Parallel Port address is 278H that selects the rounting of IRQ5 for LPT1.**

- **Parallel port Mode:** This field allows the user to sellect the parallel port mode. The default value is ECP+EPP.
  Normal **:** Standard mode. IBM PC/AT Compatible bidirectional parallel port.
  EPP **:** Enhanced Parallel Port mode.
  ECP **:** Extended Capabilities Port mode.
  EPP+ECP **:** ECP Mode & EPP Mode.

  ECP Mode USE DMA: This field allows the user to sellect DMA1 or DMA3 for the ECP mode. The default value is DMA3.
  DMA1 **:** The filed selects the rounting of DMA1 for the ECP mode.
  DMA3 **:** The filed selects the rounting of DMA3 for the ECP mode.

3-7 LOAD SETUP DEFAULTS

The "**LOAD SETUP DEFAULTS**" function loads the system default data directly from ROM and initializes the associated hardware properly. This function will be necessary only when the system CMOS data is corrupted.

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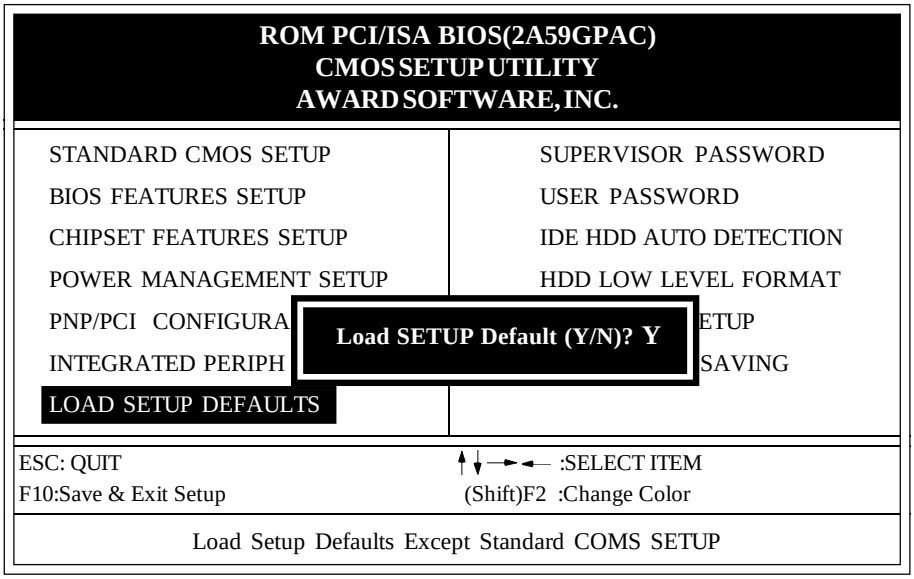

Figure 3-8 LOAD SETUP DEFAULT

3-8 CHANGE SUPERVISOR or USER PASSWORD

To change the password, choose the '**SUPERVISOR PASSWORD or USER PASSWORD** " option from the **CMOS SETUP UTILITY** menu and press [Enter].

NOTE : Either "**Setup**" or "**System**" must be selected in the '**Security Option**" of the **BIOS FEATURES SETUP** menu (Refer to Figure 3-3 for the details).

1. If CMOS is corrupted or the option is not used, a default password stored in the ROM will be used. The screen will display the following message:

   Enter Password:

   Press the [Enter] key to continue after proper password is given.

2. If CMOS is corrupted or the option was used earlier and the user wish to change default password, the **SETUP UTILITY** will display a message and ask for a confirmation.

   Confirm Password:

3. After pressing the [Enter] key (ROM password if the option was not used) or current password (user-defined password), the user can change the password and store new one in CMOS RAM. A maximum of 8 characters can be entered.

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3-9 IDE HDD AUTO DETECTION

The "IDE HDD AUTO DETECTION" utility is a very useful tool especially when you do not know which kind of hard disk type you are using. You can use this utility to detect the correct disk type installed in the system automatically. **But now** you can set **HARD DISK TYPE** to **Auto** in the **STANDARD CMOS SETUP**. You do not need the "IDE HDD AUTO DETECTION" utility. The BIOS will Auto-detect the hard disk size and model on display during POST.

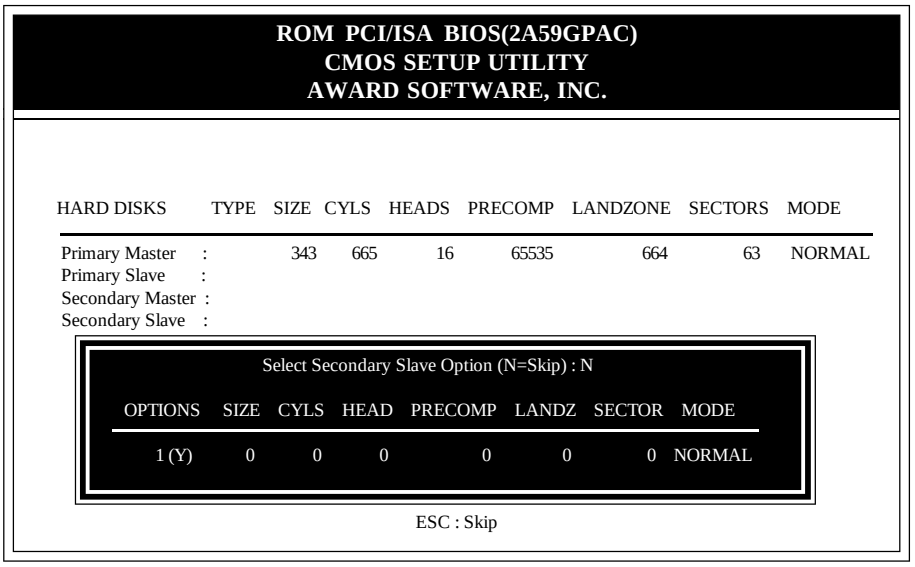

Figure 3-9 IDE HDD AUTO DETECTION

NOTE: HDD Modes

The Award BIOS supports 3 HDD modes : NORMAL, LBA & LARGE

NORMAL mode.

Generic access mode in which neither the BIOS nor the IDE controller will make any transformations during accessing.

The maximum numbers of cylinders, heads & sectors for NORMAL mode are 1024, 16 & 63.

no. Cyclinder	(1024)
x no. Head	(16)
x no. Sector	(63)
x no. per sector	(512)
528 Megabytes	

If user sets his HDD to NORMAL mode, the maximum accessible HDD size will be 528 Megabytes even though its physical size may be greater than that!

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LBA (Logical Block Addressing) mode: A new HDD accessing method to overcome the 528 Megabyte bottleneck.
The number of cylinders, heads & sectors shown in setup may not be the number physically contained in the HDD.

During HDD accessing, the IDE controller will transform the logical address described by sector, head & cylinder into its own physical address inside the HDD.

The maximum HDD size supported by LBA mode is 8.4 Gigabytes which is obtained by the following formula:

no. Cyclinder	(1024)
x no. Head	(255)
x no. Sector	(63)
x bytes per secttor	(512)
8.4 Gigabytes	

LARGE mode: Extended HDD access mode supported by Award Software.

Some IDE HDDs contain more than 1024 cylinder without LBA support (in some cases, user does not want LBA). The Award BIOS provides another alternative to support these kinds of LARGE mode:

CYLS.	HEADS	SECTOR	MODE
1120	16	59	NORMAL
560	32	59	LARGE

BIOS tricks DOS (or other OS) that the number of cylinders is less than 1024 by dividing it by 2. At the same time, the number of heads is nultiplied by 2. A reverse transformation process will be made inside INT 12h in order to access the right HDD address!

Maximum HDD size:

no. Cyclinder	(1024)
x no. Head	(32)
x no. Sector	(63)
x bytes per sector	(512)
1 Gigabytes	

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Note:

To support LBA or LARGE mode of HDDs, there must be some softwares involved. All the software is located in the Award HDD Service Routine (1NT 13h). It may fail to access a HDD with LBA (LARGE) mode selected if you are running under an Operating System which replaces the whole 1NT 13h. UNIX operating systems do not support either LBA or LARGE and must utilize the Standard mode. UNIX can support drives larger than 528MB.

3-10 HDD LOW LEVEL FORMAT

Interleave

Select the interleave number of the hard disk drive that you wish to perform a low level format on. You may select from 1 to 8. Check the documentation that came with the drive for the correct interleave number, or select 0 for automatic detection.

Auto scan bad track

This allows the utility to scan first then format by each track.

Start

Press<Y>to start low level format.

3-11 SAVE & EXIT SETUP

The "**SAVE & EXIT SETUP**" option will bring you back to boot up procedure with all changes you just recorded in the CMOS RAM.

3-12 EXIT WITHOUT SAVING

The "**EXIT WITHOUT SAVING**" option will bring you back to normal boot up procedure without saving any data into CMOS RAM. All old data in the CMOS will not be destroyed.

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Chapter 4
Technical Information

4-1 I/O & MEMORY MAP

MEMORY MAP

Address Range	Size	Description
[00000-7FFFF]	512K	Conventional memory
[80000-9FBFF]	127K	Extended Conventional memory
[9FC00-9FFFF]	1K	Extended BIOS data area if PS/2 mouse is installed
[A0000-C7FFF]	160K	Available for Hi DOS memory
[C8000-DFFFF]	96K	Available for Hi DOS memory and adapter ROMs
[E0000-EEFFF]	60K	Available for UMB
[EF000-EFFFF]	4K	Video service routine for Monochrome & CGA adaptor
[F0000-F7FFF]	32K	BIOS CMOS setup utility
[F8000-FCFFF]	20K	BIOS runtime service routine (2)
[FD000-FDFFF]	4K	Plug and Play ESCD data area
[FE000-FFFFF]	8K	BIOS runtime service routine (1)

I/O MAP

[000-01F]	DMA controller.(Master)
[020-021]	INTERRUPT CONTROLLER.(Master)
[022-023]	CHIPSET control registers. I/O ports.
[040-05F]	TIMER control registers.
[060-06F]	KEYBOARD interface controller.(8042)
[070-07F]	RTC ports & CMOS I/O ports.
[080-09F]	DMA register.
[0A0-0BF]	INTERRUPT controller.(Slave)
[0C0-0DF]	DMA controller.(Slave)
[0F0-0FF]	MATH COPROCESSOR.
[1F0-1F8]	HARD DISK controller.
[278-27F]	PARALLEL port 2.
[2B0-2DF]	GRAPHICS adapter controller.
[2F8-2FF]	SERIAL port 2.
[360-36F]	NETWORK ports.
[378-37F]	PARALLEL port 1.
[3B0-3BF]	MONOCHROME & PARALLEL port adapter.
[3C0-3CF]	EGA adapter.
[3D0-3DF]	CGA adapter.
[3F0-3F7]	FLOPPY DISK controller.
[3F8-3FF]	SERIAL port 1.

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4-2 TIME & DMA CHANNELS MAP

TIME MAP:	TIMER Channel 0	System timer interrupt.
	TIMER Channel 1	DRAM REFRESH request.
	TIMER Channel 2	SPEAKER tone generator.
DMA CHANNELS :	DMA Channel 0	Available.
	DMA Channel 1	Onboard ECP (Option).
	DMA Channel 2	FLOPPY DISK (SMC CHIP).
	DMA Channel 3	Onboard ECP (default).
	DMA Channel 4	Cascade for DMA controller 1.
	DMA Channel 5	Available.
	DMA Channel 6	Available.
	DMA Channel 7	Available.

4-3 INTERRUPT MAP

NMI : Parity check error.

IRQ (H/W) :	0	System TIMER interrupt from TIMER 0.
	1	KEYBOARD output buffer full.
	2	Cascade for IRQ 8-15.
	3	SERIAL port 2.
	4	SERIAL port 1.
	5	PARALLEL port 2.
	6	FLOPPY DISK (SMC CHIP).
	7	PARALLEL port 1.
	8	RTC clock.
	9	Available.
	10	Available.
	11	Available.
	12	PS/2 Mouse.
	13	MATH coprocessor.
	14	Onboard HARD DISK(IDE1) channel.
	15	Onboard HARD DISK(IDE2) channel.

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4-4 RTC & CMOS RAM MAP

RTC & CMOS :	00	Seconds.
	01	Second alarm.
	02	Minutes.
	03	Minutes alarm.
	04	Hours.
	05	Hours alarm.
	06	Day of week.
	07	Day of month.
	08	Month.
	09	Year.
	0A	Status register A.
	0B	Status register B.
	0C	Status register C.
	0D	Status register D.
	0E	Diagnostic status byte.
	0F	Shutdown byte.
	10	FLOPPY DISK drive type byte.
	11	Reserve.
	12	HARD DISK type byte.
	13	Reserve.
	14	Equipment type.
	15	Base memory low byte.
	16	Base memory high byte.
	17	Extension memory low byte.
	18	Extension memory high byte.
	19-2d	
	2E-2F	
	30	Reserved for ectension memory low bytw.
	31	Reserved for extension memory high byte.
	32	DATE CENTURY byte.
	33	INFORMATION FLAG.
	35-3F	Reserve.
	40-7F	Reserved for CHIPSET SETTING DATA.

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APPENDIX A: POST CODES

ISA POST codes are typically output to port address 80h.

POST(hex)	DESCRIPTION
01-02	Reserved.
C0	Turn off OEM specific cache, shadow.
03	1.Initialize EISA registers (EISA BIOS only). 2.Initialize all the standard devices with default values Standard devices includes. -DMA controller (8237). -Programmable Interrupt Controller (8259). -Programmable Interval Timer (8254). -RTC chip.
04	Reserved
05	1.Keyboard Controller Self-Test. 2.Enable Keyboard Interface.
06	Reserved.
07	Verifies CMOS's basic R/W functionality.
C1	Auto-detection of onboard DRAM & Cache.
C5	Copy the BIOS from ROM into E0000-FFFFF shadow RAM so that POST will go faster.
08	Test the first 256K DRAM.
09	OEM specific cache initialization. (if needed)
0A	1.Initialize the first 32 interrupt vectors with corresponding Interrupt handlers Initialize INT no from 33-120 with Dummy (Suprious) Interrupt Handler. 2.Issue CPUID instruction to identify CPU type. 3.Early Power Management initialization. (OEM specific)
0B	1.Verify the RTC time is valid or not. 2.Detect bad battery. 3.Read CMOS data into BIOS stack area. 4.PnP initializations including. (PnP BIOS only) -Assign CSN to PnP ISA card. -Create resource map from ESCD. 5.Assign IO & Memory for PCI devices. (PCI BIOS only)

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POST(hex)	DESCRIPTION
0C	Initialization of the BIOS Data Area. (40:ON - 40:FF)
0D	1.Program some of the Chipset's value according to Setup. (Early Setup Value Program) 2.Measure CPU speed for display & decide the system clock speed. 3.Video initialization including Monochromc, CGA, EGA/VGA. If no display device found, the speaker will beep.
0E	1.Test video RAM. (If Monochromc display device found) 2.Show messages including. -Award Logo, Copyright string, BIOS Data code & Part No. -OEM specific sign on messages. -Energy Star Logo. (Green BIOS ONLY) -CPU brand, type & speed. -Test system BIOS checksum. (Non-Compress Version only)
0F	DMA channel 0 test.
10	DMA channel 1 test.
11	DMA page registers test.
12-13	Reserved.
14	Test 8254 Timer 0 Counter 2.
15	Test 8259 interrupt mask bits for channel 1.
16	Test 8259 interrupt mask bits for channel 2.
17	Reserved.
19	Test 8259 functionality.
1A-1D	Reserved.
1E	If EISA NVM checksum is good, exccute EISA initialization. (EISA BIOS only)
1F-29	Reserved.
30	Detect Base Memory & Extended Memory Size.
31	1.Test Base Memory from 256K to 640K. 2.Test Extended Memory from 1M to the top of memory.

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POST(hex)	DESCRIPTION
32	1.Display the Award Plug & Play BIOS Extension message. (PnP BIOS only) 2.Program all onboard super I/O chips (if any) including COM ports, LPT ports, FDD port ... according to setup value.
33-3B	Reserved.
3C	Set flag to allow users to enter CMOS Setup Utility.
3D	1.Initialize Keyboard. 2.Install PS2 mouse.
3E	Try to turn on Level 2 cache. Note : Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in POST 61h.
3F-40	Reserved.
BF	1.Program the rest of the Chipset's value according to Setup. (Later Setup Value Program) 2.If auto-configuration is enabled, programmed the chipset with pre-defined Values.
41	Initialize floppy disk drive controller.
42	Initialize Hard drive controller.
43	If it is a PnP BIOS, initialize serial & parallel ports.
44	Reserved.
45	Initialize math coprocessor.
46-4D	Reserved.
4E	If there is any error detected (such as video, kb...), show all the error messages on the screen & wait for user to press <F1> key.
4F	1.If password is needed, ask for password. 2.Clear the Energy Star Logo. (Green BIOS only)
50	Write all CMOS values currently in the BIOS stack area back into the CMOS.
51	Reserved.

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POST(hex)	DESCRIPTION
52	1.Initialize all ISA ROMs. 2.Later PCI initializations. (PCI BIOS only) -assign IRQ to PCI devices. -initialize all PCI ROMs. 3.PnP Initialzations. (PnP BIOS only) -assign IO, Memory, IRQ & DMA to PnP ISA devices. -initialize all PnP ISA ROMs. 4.Program shadows RAM according to Setup settings. 5.Program parity according to Setup setting. 6.Power Management Initialization. -Enable/Disable global PM. -APM interface initialization.
53	1.If it is NOT a PnP BIOS, initialize serial & paralled ports. 2.Initialize time value in BIOS data area by translate the RTC time value into a timer tick value.
60	Setup Virus Protection. (Boot Sector Protection) functionality according to Setup setting.
61	1.Try to turn on Level 2 cache. Note : if L2 cache is already turned on in POST 3D, this part will be skipped. 2.Set the boot up speed according to Setup setting. 3.Last chance for Chipset initialization. 4.Last chance for Power Management initialization. (Green BIOS only) 5.Show the system configuration table.
62	1.Setup daylight saving according to Setup value. 2.Program the NUM Lock, typematic rate & typematic speed according to Setup setting.
63	1.If there is any changes in the hardware configuration, update the ESCD information. (PnP BIOS only) 2.Clear memory that have been used. 3.Boot system via INT 19H.
FF	System Booting. This means that the BIOS already pass the control right to the operating system.

Unexpected Errors:

POST(hex)	DESCRIPTION
B0	If interrupt occurs in protected mode.
B1	Unclaimed NMI occurs.

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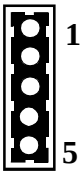
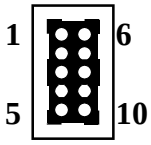
APPENDIX B: I/O CONNECTORS

J1 : PS/2 MOUSE CONNECTOR:



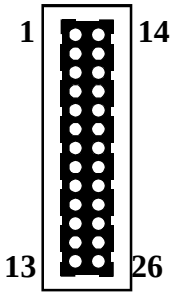
Pin	Signal Name
1	Data (Red Wire)
2	Clock (Blue Wire)
3	GND (Green Wire)
4	NC
5	VCC (Yellow Wire)

CN3/COM1,CN4/COM2 : Serial Ports Connector



Signal Name	Pin	Pin	Signal Name
DCD	1	6	DSR
SIN	2	7	RTS
SOUT	3	8	CTS
DTR	4	9	RI
GND	5		

CN5 : Parallel Port Connector



Signal Name	Pin	Pin	Signal Name
STROBE-	1	14	AUTO FEED-
Data Bit 0	2	15	ERROR-
Data Bit 1	3	16	INIT-
Data Bit 2	4	17	SLCT IN-
Data Bit 3	5	18	Ground
Data Bit 4	6	19	Ground
Data Bit 5	7	20	Ground
Data Bit 6	8	21	Ground
Data Bit 7	9	22	Ground
ACJ-	10	23	Ground
BUSY	11	24	Ground
PE	12	25	Ground
SLCT	13		

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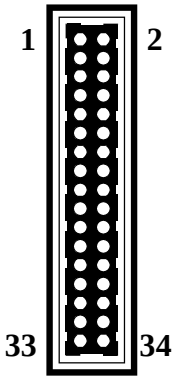
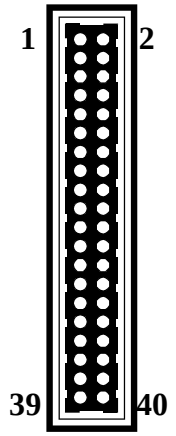
CN6 : Floppy Disk Connector



Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Ground	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data
Ground	23	24	Write Gate
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	SIDE 1 SELECT-
Ground	33	34	Diskette

CN7/CN8 : Primary, Secondray IDE Connector



Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	32	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

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CN1: USB Connector:

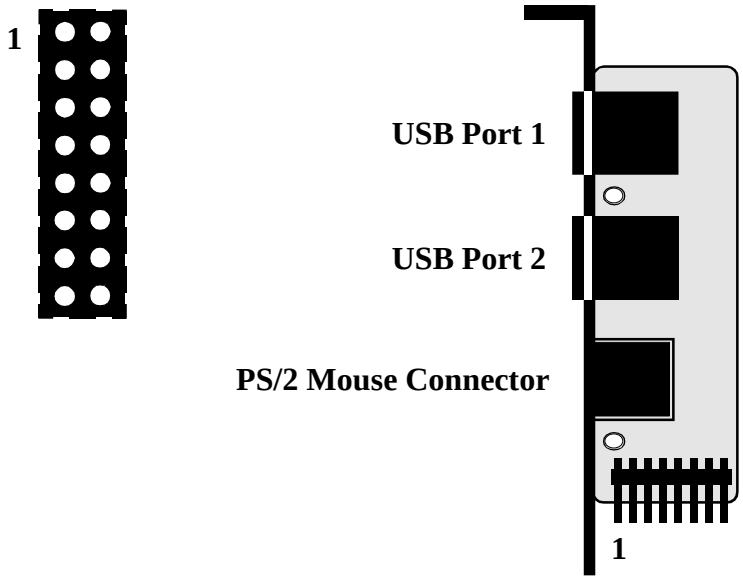

Figure 4-1 USB Port Adapter

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