# 16M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

## DESCRIPTION

This is a family of 16,777,216 x 4 bit Fast Page Mode CMOS DRAMs. Fast Page Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time(-5, -6, or -7), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh and Hidden refresh capabilities. Further- more, Self-refresh operation is available in L- version. This 16Mx4 Fast Page mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability.



## FEATURES

- Part Identification
  - KM44V16000A/A-L(3.3V, 8K Ref.)
  - KM44V16100A/A-L(3.3V, 4K Ref.)

- Active Power Dissipation

Unit : mW

| Speed | 8K | 4K |
|---|---|---|
| -5 | 360 | 540 |
| -6 | 324 | 504 |
| -7 | 288 | 468 |

- Refresh cycles

| Part NO. | Refresh cycle | Refresh time | |
|---|---|---|---|
| | | Normal | L-ver |
| KM44V16000A* | 8K | 64ms | 128ms |
| KM44V16100A | 4K | | |

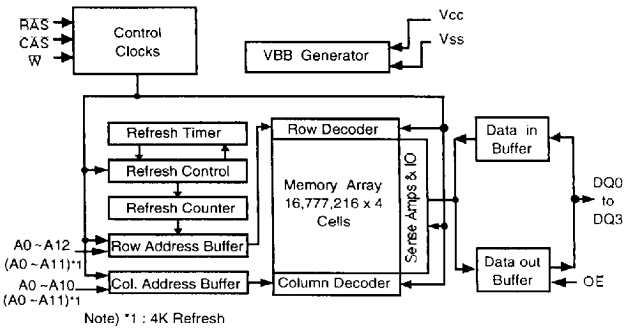
* Access mode & $\overline{RAS}$ only refresh mode
: 8K cycle/64ms
$\overline{CAS}$-before-$\overline{RAS}$ & Hidden refresh mode
: 4K cycle/64ms

- Performance range:

| Speed | tRAC | tCAC | tRC | tPC |
|---|---|---|---|---|
| -5 | 50ns | 13ns | 90ns | 35ns |
| -6 | 60ns | 15ns | 110ns | 40ns |
| -7 | 70ns | 20ns | 130ns | 45ns |

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$ only and Hidden refresh capability
- Self-refresh capability(L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

## FUNCTIONAL BLOCK DIAGRAM




Note) *1 : 4K Refresh

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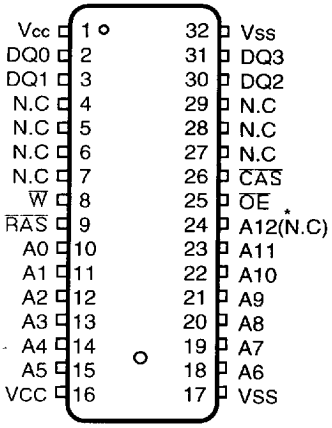
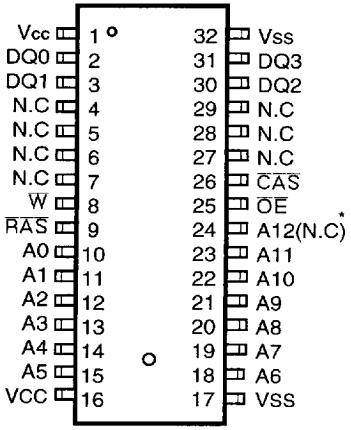
## PIN CONFIGURATION (Top Views)

• KM44V160(1)00AK




(K: 400mil SOJ)

• KM44V160(1)00AS




(S: 400mil TSOP(II))

* ( N.C) : N.C for 4K Refresh product

| Pin Name | Pin Function |
|---|---|
| A0 - A12 | Address Inputs(8K Product) |
| A0 - A11 | Address Inputs(4K Product) |
| DQ0 -3 | Data In/Out |
| Vss | Ground |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{W}$ | Read/Write Input |
| $\overline{OE}$ | Data Outputs Enable |
| Vcc | Power(+3.3V) |
| N.C | No Connection |



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## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$,$V_{OUT}$ | -0.5 to +4.6 | V |
| Voltage on $V_{CC}$ supply relative to Vss | $V_{CC}$ | -0.5 to +4.6 | V |
| Storage Temperature | Tstg | -55 to +150 | °C |
| Power Dissipation | $P_D$ | 1 | W |
| Short Circuit Output Current | $I_{OS}$ | 50 | mA |

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS}$, $T_A$= 0 to 70 °C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage | $V_{IH}$ | 2.0 | - | Vcc+0.3*1 | V |
| Input Low Voltage | $V_{IL}$ | -0.3*2 | - | 0.8 | V |

*1 : Vcc+1.3V at pulse width ≤ 15ns which is measured at Vcc
*2 : -1.3V at pulse width ≤ 15ns which is measured at Vss

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Input Leakage Current (Any input 0≤$V_{IN}$≤Vcc+0.3V, all other pins not under test=0 volt.) | $I_{I(L)}$ | - 5 | 5 | μA |
| Output Leakage Current (Data out is disabled, 0V≤$V_{OUT}$≤Vcc) | $I_{O(L)}$ | - 5 | 5 | μA |
| Output High Voltage Level($I_{OH}$=-2mA) | $V_{OH}$ | 2.4 | - | V |
| Output Low Voltage Level($I_{OL}$=2mA) | $V_{OL}$ | - | 0.4 | V |

**DC AND OPERATING CHARACTERISTICS** (Continued.)

| Symbol | Power | Speed | Max | | Units |
|---|---|---|---|---|---|
| | | | KM44V16000A | KM44V16100A | |
| $I_{CC1}$ | Don't care | -5<br>-6<br>-7 | 100<br>90<br>80 | 150<br>140<br>130 | mA<br>mA<br>mA |
| $I_{CC2}$ | Normal<br>L | Don't care | 1<br>1 | 1<br>1 | mA<br>mA |
| $I_{CC3}$ | Don't care | -5<br>-6<br>-7 | 100<br>90<br>80 | 150<br>140<br>130 | mA<br>mA<br>mA |
| $I_{CC4}$ | Don't care | -5<br>-6<br>-7 | 70<br>60<br>55 | 80<br>70<br>65 | mA<br>mA<br>mA |
| $I_{CC5}$ | Normal<br>L | Don't care | 500<br>300 | 500<br>300 | µA<br>µA |
| $I_{CC6}$ | Don't care | -5<br>-6<br>-7 | 150<br>140<br>130 | 150<br>140<br>130 | mA<br>mA<br>mA |
| $I_{CC7}$ | L | Don't care | 550 | 550 | µA |
| $I_{CCS}$ | L | Don't care | 450 | 450 | µA |

$I_{CC1}$* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

$I_{CC2}$ : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$V_{IH}$ )

$I_{CC3}$* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=$V_{IH}$, $\overline{RAS}$ cycling @tRC=min.)

$I_{CC4}$* : Fast Page Mode Current ($\overline{RAS}$=$V_{IL}$, $\overline{CAS}$, Address cycling @tPC=min.)

$I_{CC5}$ : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$V_{CC}$-0.2V)

$I_{CC6}$* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)

$I_{CC7}$ : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage($V_{IH}$)=Vcc-0.2V, Input low voltage($V_{IL}$)=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V

$\overline{W}$, $\overline{OE}$ = VIH, Address = Don't care, DQ = Open, $T_{RC}$= 31.25µs

$T_{RAS}$=$T_{RAS}$min~300 ns

$I_{CCS}$ : Self Refresh Current

$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11) = Vcc-0.2V or 0.2V, DQ0 ~ DQ3= Vcc-0.2V, 0.2V or Open

* NOTE : $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In $I_{CC1}$, $I_{CC3}$, and $I_{CC6}$, address can be changed maximum once while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed maximum once within one fast page mode cycle time tPC.

**CAPACITANCE**($T_A$=25°C, Vcc= 3.3V, f=1MHz)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance [A0 - A12] | $C_{IN1}$ | - | 5 | pF |
| Input capacitance [$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$] | $C_{IN2}$ | - | 7 | pF |
| Output Capacitance [DQ0 - DQ3] | $C_{DQ}$ | - | 7 | pF |

**AC CHARACTERISTICS** (0°C≤$T_A$≤70°C, See note 2)
Test condition : Vcc=3.3V±0.3V, $V_{ih}$/$V_{il}$=2.0/0.8V, $V_{oh}$/$V_{ol}$ =2.0/0.8V

| Parameter | Symbol | -5 | | -6 | | -7 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 90 | | 110 | | 130 | | ns | |
| Read-modify-write cycle time | tRWC | 133 | | 153 | | 180 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 50 | | 60 | | 70 | ns | 3,4,10 |
| Access time from $\overline{CAS}$ | tCAC | | 13 | | 15 | | 20 | ns | 3,4,5 |
| Access time from column address | tAA | | 25 | | 30 | | 35 | ns | 3,10 |
| $\overline{CAS}$ to output in Low-Z | tCLZ | 0 | | 0 | | 0 | | ns | 3 |
| Output buffer turn-off delay | tOFF | 0 | 13 | 0 | 13 | 0 | 15 | ns | 6 |
| Transition time (rise and fall) | tT | 3 | 50 | 3 | 50 | 3 | 50 | ns | 2 |
| $\overline{RAS}$ precharge time | tRP | 30 | | 40 | | 50 | | ns | |
| $\overline{RAS}$ pulse width | tRAS | 50 | 10K | 60 | 10K | 70 | 10K | ns | |
| $\overline{RAS}$ hold time | tRSH | 13 | | 15 | | 20 | | ns | |
| $\overline{CAS}$ hold time | tCSH | 50 | | 60 | | 70 | | ns | |
| $\overline{CAS}$ pulse width | tCAS | 13 | 10K | 15 | 10K | 20 | 10K | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | tRCD | 20 | 37 | 20 | 45 | 20 | 50 | ns | 4 |
| $\overline{RAS}$ to column address delay time | tRAD | 15 | 25 | 15 | 30 | 15 | 35 | ns | 10 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | tCRP | 5 | | 5 | | 5 | | ns | |
| Row address set-up time | tASR | 0 | | 0 | | 0 | | ns | |
| Row address hold time | tRAH | 10 | | 10 | | 10 | | ns | |
| Column address set-up time | tASC | 0 | | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 10 | | 10 | | 15 | | ns | |
| Column address to $\overline{RAS}$ lead time | tRAL | 25 | | 30 | | 35 | | ns | |
| Read command set-up time | tRCS | 0 | | 0 | | 0 | | ns | |
| Read command hold time referenced to $\overline{CAS}$ | tRCH | 0 | | 0 | | 0 | | ns | 8 |
| Read command hold time referenced to $\overline{RAS}$ | tRRH | 0 | | 0 | | 0 | | ns | 8 |
| Write command hold time | tWCH | 10 | | 10 | | 15 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | 15 | | ns | |
| Write command to $\overline{RAS}$ lead time | tRWL | 15 | | 15 | | 20 | | ns | |
| Write command to $\overline{CAS}$ lead time | tCWL | 13 | | 15 | | 20 | | ns | |

## AC CHARACTERISTICS (Continued)

| Parameter | Symbol | -5 | | -6 | | -7 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Data set-up time | tDS | 0 | | 0 | | 0 | | ns | 9 |
| Data hold time | tDH | 10 | | 10 | | 15 | | ns | 9 |
| Refresh period(4K, Normal) | tREF | | 64 | | 64 | | 64 | ms | |
| Refresh period(8K, Normal) | tREF | | 64 | | 64 | | 64 | ms | |
| Refresh period(L-ver) | tREF | | 128 | | 128 | | 128 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | 0 | | ns | 7 |
| $\overline{CAS}$ to $\overline{W}$ delay time | tCWD | 36 | | 38 | | 45 | | ns | 7 |
| $\overline{RAS}$ to $\overline{W}$ delay time | tRWD | 73 | | 83 | | 95 | | ns | 7 |
| Column address to $\overline{W}$ delay time | tAWD | 48 | | 53 | | 60 | | ns | 7 |
| $\overline{CAS}$ precharge to $\overline{W}$ delay time | tCPWD | 53 | | 60 | | 70 | | ns | |
| $\overline{CAS}$ set-up time ($\overline{CAS}$-before-$\overline{RAS}$ refresh) | tCSR | 10 | | 10 | | 10 | | ns | |
| $\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh) | tCHR | 10 | | 10 | | 15 | | ns | 14 |
| $\overline{RAS}$ to $\overline{CAS}$ precharge time | tRPC | 5 | | 5 | | 5 | | ns | |
| $\overline{CAS}$ precharge time($\overline{CBR}$ counter test cycle) | tCPT | 20 | | 20 | | 30 | | ns | |
| Access time from $\overline{CAS}$ precharge | tCPA | | 30 | | 35 | | 40 | ns | 3 |
| Fast Page mode cycle time | tPC | 35 | | 40 | | 45 | | ns | |
| Fast Page mode read-modify-write cycle time | tPRWC | 76 | | 85 | | 100 | | ns | |
| $\overline{CAS}$ precharge time (Fast page cycle) | tCP | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ pulse width (Fast page cycle) | tRASP | 50 | 200K | 60 | 200K | 70 | 200K | ns | |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | tRHCP | 30 | | 35 | | 40 | | ns | |
| $\overline{OE}$ access time | tOEA | | 13 | | 15 | | 20 | ns | |
| $\overline{OE}$ to data delay | tOED | 13 | | 13 | | 15 | | ns | |
| Out put buffer turn off delay time from $\overline{OE}$ | tOEZ | 0 | 13 | 0 | 13 | 0 | 15 | ns | 6 |
| $\overline{OE}$ command hold time | tOEH | 13 | | 15 | | 20 | | ns | |
| Write command set-up time(Test mode in) | tWTS | 10 | | 10 | | 10 | | ns | 11 |
| Write command hold time(Test mode in) | tWTH | 15 | | 15 | | 15 | | ns | 11 |
| $\overline{W}$ to $\overline{RAS}$ precharge time($\overline{C}$-B-$\overline{R}$ refresh) | tWRP | 10 | | 10 | | 10 | | ns | |
| $\overline{W}$ to $\overline{RAS}$ hold time($\overline{C}$-B-$\overline{R}$ refresh) | tWRH | 10 | | 10 | | 10 | | ns | |
| $\overline{RAS}$ pulse width($\overline{C}$-B-$\overline{R}$ self refresh) | tRASS | 100 | | 100 | | 100 | | us | 13 |
| $\overline{RAS}$ precharge time ($\overline{C}$-B-$\overline{R}$ self refresh) | tRPS | 90 | | 110 | | 130 | | ns | 13 |
| $\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ self refresh) | tCHS | -50 | | -50 | | -50 | | ns | 13 |

## TEST MODE CYCLE

(Note. 11)

| Parameter | Symbol | -5 | | -6 | | -7 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 95 | | 115 | | 135 | | ns | |
| Read-modify-write cycle time | tRWC | 138 | | 160 | | 190 | | ns | |
| Access time from $\overline{RAS}$ | tRAC | | 55 | | 65 | | 75 | ns | 3,4,10,12 |
| Access time from $\overline{CAS}$ | tCAC | | 18 | | 20 | | 25 | ns | 3,4,5,12 |
| Access time from column address | tAA | | 30 | | 35 | | 40 | ns | 3,10,12 |
| $\overline{RAS}$ pulse width | tRAS | 55 | 10K | 65 | 10K | 75 | 10K | ns | |
| $\overline{CAS}$ pulse width | tCAS | 18 | 10K | 20 | 10K | 25 | 10K | ns | |
| $\overline{RAS}$ hold time | tRSH | 18 | | 20 | | 25 | | ns | |
| $\overline{CAS}$ hold time | tCSH | 55 | | 65 | | 75 | | ns | |
| Column address to $\overline{RAS}$ lead time | tRAL | 30 | | 35 | | 40 | | ns | |
| $\overline{CAS}$ to $\overline{W}$ delay time | tCWD | 41 | | 43 | | 50 | | ns | 7 |
| $\overline{RAS}$ to $\overline{W}$ delay time | tRWD | 78 | | 88 | | 100 | | ns | 7 |
| Column address to $\overline{W}$ delay time | tAWD | 53 | | 58 | | 65 | | ns | 7 |
| Fast Page mode cycle time | tPC | 40 | | 45 | | 50 | | ns | |
| Fast page mode read-modify-write cycle time | tPRWC | 81 | | 90 | | 105 | | ns | |
| $\overline{RAS}$ pulse width (Fast page cycle) | tRASP | 55 | 200K | 65 | 200K | 75 | 200K | ns | |
| Access time form $\overline{CAS}$ precharge | tCPA | | 35 | | 40 | | 45 | ns | 3 |
| $\overline{OE}$ access time | tOEA | | 18 | | 20 | | 25 | ns | |
| $\overline{OE}$ to data delay | tOED | 18 | | 18 | | 20 | | ns | |
| $\overline{OE}$ command hold time | tOEH | 18 | | 20 | | 25 | | ns | |

## NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}$(min) and $V_{IL}$(max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$(min) and $V_{IL}$(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD≥ tRCD(max).
6. tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to $V_{oh}$ or $V_{ol}$.
7. tWCS, tRWD, tCWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If tWCS≥tWCS(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tCWD≥ tCWD(min), tRWD≥tRWD(min) and tAWD≥ tAWD(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-modify-write cycles.
10. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. For all of the refresh mode except the distributed $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096(8192) cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
14. It can get less $\overline{CAS}$-before-$\overline{RAS}$ current loss if tCHR≥tRAS or $\overline{CAS}$≤0.2V at $\overline{CAS}$-before-$\overline{RAS}$ refresh mode.