INTEGRATED CIRCUIT

TOSHIBA

TECHNICAL DATA

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT
TC5117400 CSJ / CST - 40
TC5117400 CSJ / CST - 50
TC5117400 CSJ / CST - 60
SILICON GATE CMOS

TENTATIVE DATA

4,194,304 WORD ×4 BIT FAST PAGE DYNAMIC RAM

DESCRIPTION

The TC5117400CSJ/CST is fast page dynamic RAM organized 4,194,304 words by 4 bits. The TC5117400CSJ/CST utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5117400CSJ/CST to be packaged in 26/24 pin plastic SOJ (300mil), 26/24 pin plastic TSOP (300mil). The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

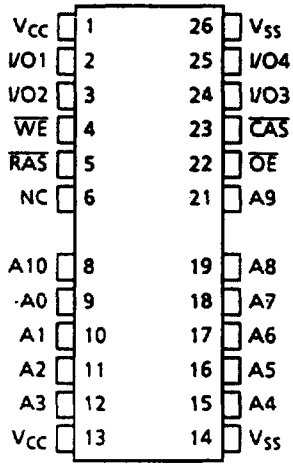
- 4,194,304 word by 4 bit organization
- Fast access time and cycle time

		TC5117400CSJ/CST		
		-40	-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	40ns	50ns	60ns
t_{AA}	Column Address Access Time	20ns	25ns	30ns
t_{CAC}	$\overline{CAS}$ Access Time	11ns	13ns	15ns
t_{RC}	Cycle Time	75ns	90ns	110ns
t_{PC}	Fast Page Mode Cycle Time	30ns	35ns	40ns

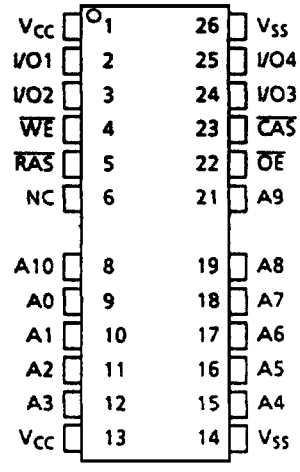
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  825mW MAX. Operating
  (TC5117400CSJ/CST-40)
  715mW MAX. Operating
  (TC5117400CSJ/CST-50)
  605mW MAX. Operating
  (TC5117400CSJ/CST-60)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 2048 refresh cycles/32ms
- Package TC5117400CSJ : SOJ26-P-300C
  TC5117400CST : TSOP26-P-300D

PIN CONNECTION (TOP VIEW)

Plastic SOJ



Plastic TSOP



PIN NAMES

A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground

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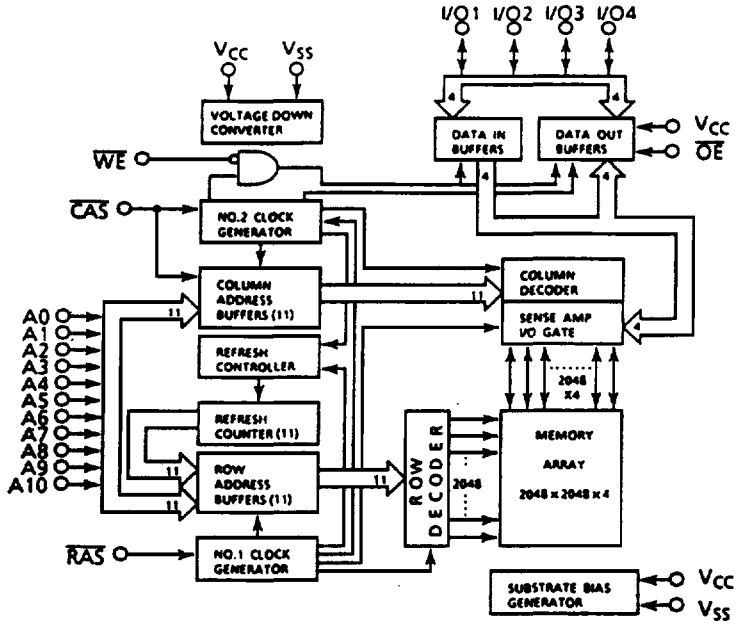
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V	1
Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V	1
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	$-55 \sim 150$	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	900	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	$V_{CC}+0.5$*	V	2
V_{IL}	Input Low Voltage	-0.5**	-	0.8	V	2

* $V_{CC}+2.0V$ at pulse width ≤ 20ns (pulse width is measured at V_{CC})

** $-2.0V$ at pulse width ≤ 20ns (pulse width is measured at V_{SS})

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC5117400CSJ/CST-40	–	150	mA	3, 4
		TC5117400CSJ/CST-50	–	130		5
		TC5117400CSJ/CST-60	–	110		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC5117400CSJ/CST-40	–	150	mA	3, 5
		TC5117400CSJ/CST-50	–	130		
		TC5117400CSJ/CST-60	–	110		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC5117400CSJ/CST-40	–	90	mA	3, 4
		TC5117400CSJ/CST-50	–	80		5
		TC5117400CSJ/CST-60	–	70		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC5117400CSJ/CST-40	–	150	mA	3, 5
		TC5117400CSJ/CST-50	–	130		
		TC5117400CSJ/CST-60	–	110		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq Vcc$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq Vcc$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5117400CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	75	–	90	–	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	107	–	126	–	150	–	ns	
t_{PC}	Fast Page Mode Cycle Time	30	–	35	–	40	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	62	–	71	–	80	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	40	–	50	–	60	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	11	–	13	–	15	ns	9,14
t_{AA}	Access Time from Column Address	–	20	–	25	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	25	–	30	–	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	11	0	13	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	25	–	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	40	10,000	50	10,000	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	40	200,000	50	200,000	60	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	6	–	8	–	10	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	25	–	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	40	–	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	11	10,000	13	10,000	15	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	16	29	18	37	20	45	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	20	13	25	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	6	–	8	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	6	–	8	–	10	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC5117400CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	6	–	8	–	10	–	ns	
t_{WP}	Write Command Pulse Width	6	–	8	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	6	–	8	–	10	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	6	–	8	–	10	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	6	–	8	–	10	–	ns	12
t_{REF}	Refresh Period	–	32	–	32	–	32	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	–	36	–	40	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	61	–	73	–	85	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	41	–	48	–	55	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	46	–	53	–	60	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	20	–	20	–	20	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	6	–	8	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	11	–	13	–	15	ns	
t_{OED}	$\overline{OE}$ to Data Delay	11	–	13	–	15	–	ns	
t_{OLZ}	$\overline{OE}$ to output in Low-Z	0	–	0	–	0	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	11	0	13	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	6	–	8	–	10	–	ns	
t_{ODS}	Output Disable Set-up Time	0	–	0	–	0	–	ns	
t_{WTS}	Write Commamd Set-Up Time (Test Mode In)	5	–	5	–	5	–	ns	
t_{WTH}	Write Commamd Hold Time (Test Mode In)	6	–	8	–	10	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	6	–	8	–	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS IN THE TEST MODE

SYMBOL	PARAMETER	TC5117400CSJ/CST						UNIT	NOTE
		-40		-50		-60			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	80	–	95	–	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	35	–	40	–	45	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	45	–	55	–	65	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	16	–	18	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	25	–	30	–	35	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	30	–	35	–	40	ns	9
t_{RAS}	$\overline{RAS}$ Pulse Width	45	10,000	55	10,000	65	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	45	200,000	55	200,000	65	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	11	–	13	–	15	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	45	–	55	–	65	–	ns	
t_{RHCP}	$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	30	–	35	–	40	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	16	10,000	18	10,000	20	10,000	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	–	30	–	35	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

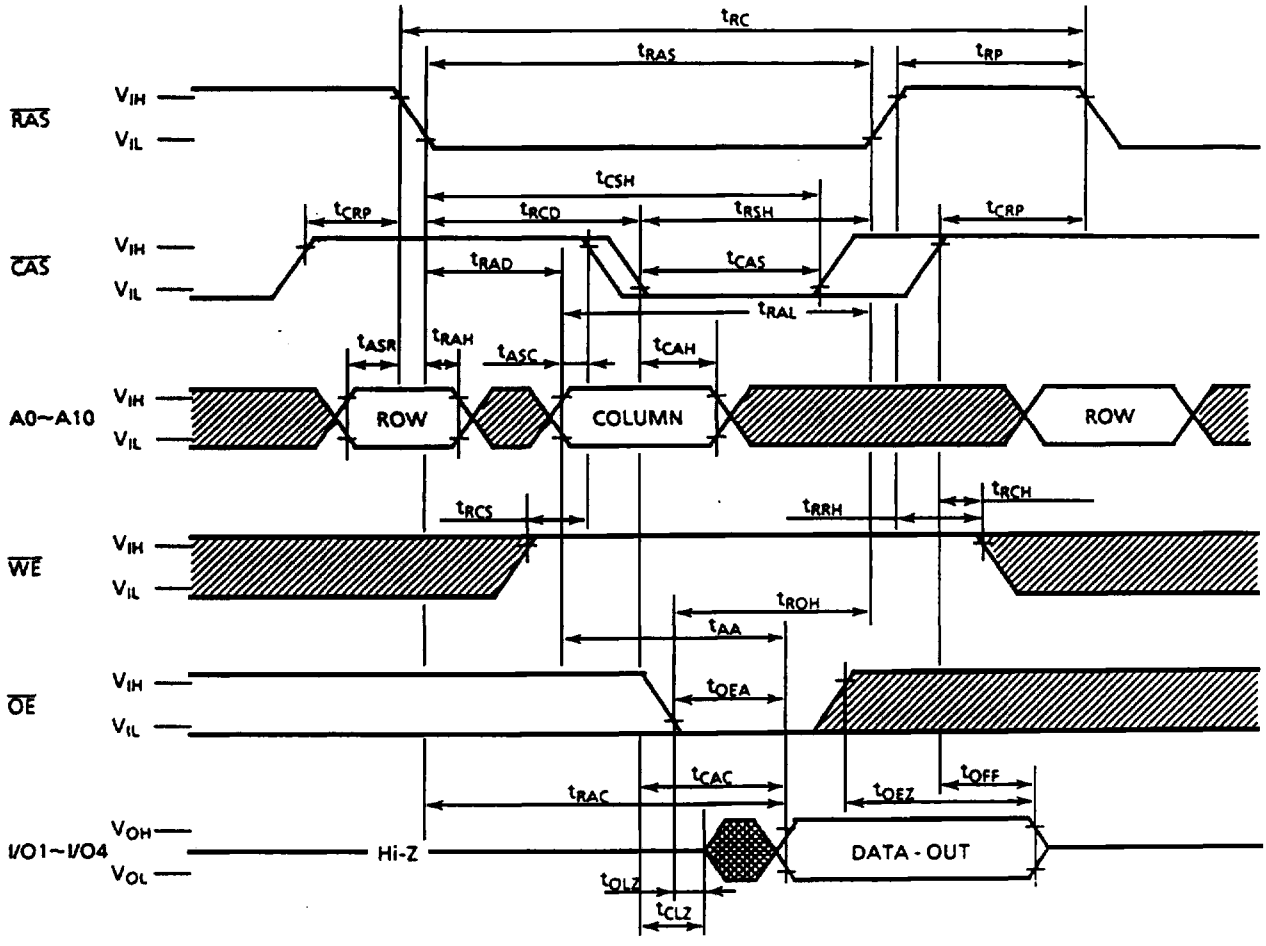
SYMBOL	PARAMETER	MIN.	MAX.	N
C_{I1}	Input Capacitance (A0~A10)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once or less while $\overline{RAS}=V_{IL}$. In case of Icc4, it can be changed once or less during a fast page mode cycle (tPC).
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING DIAGRAMS

READ CYCLE

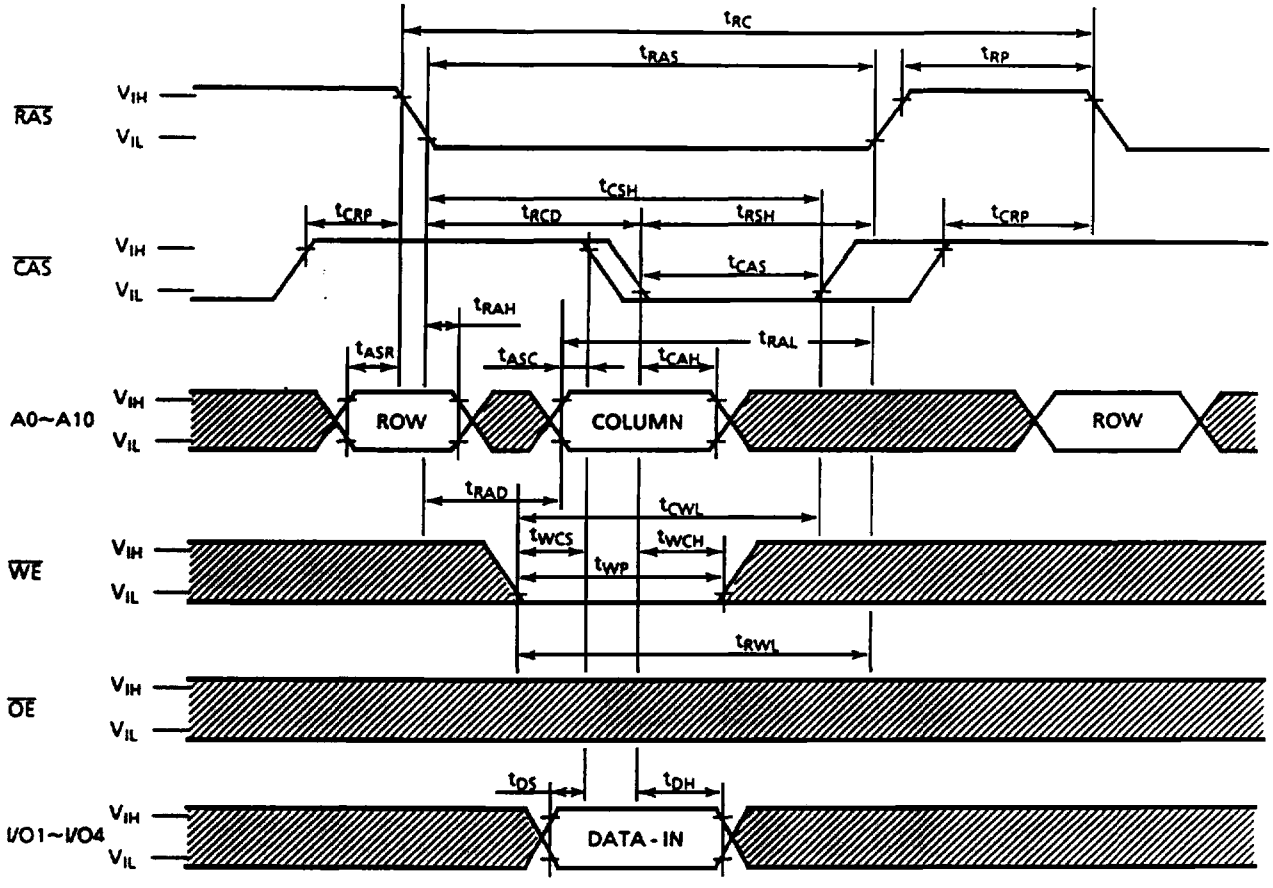


Note : D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

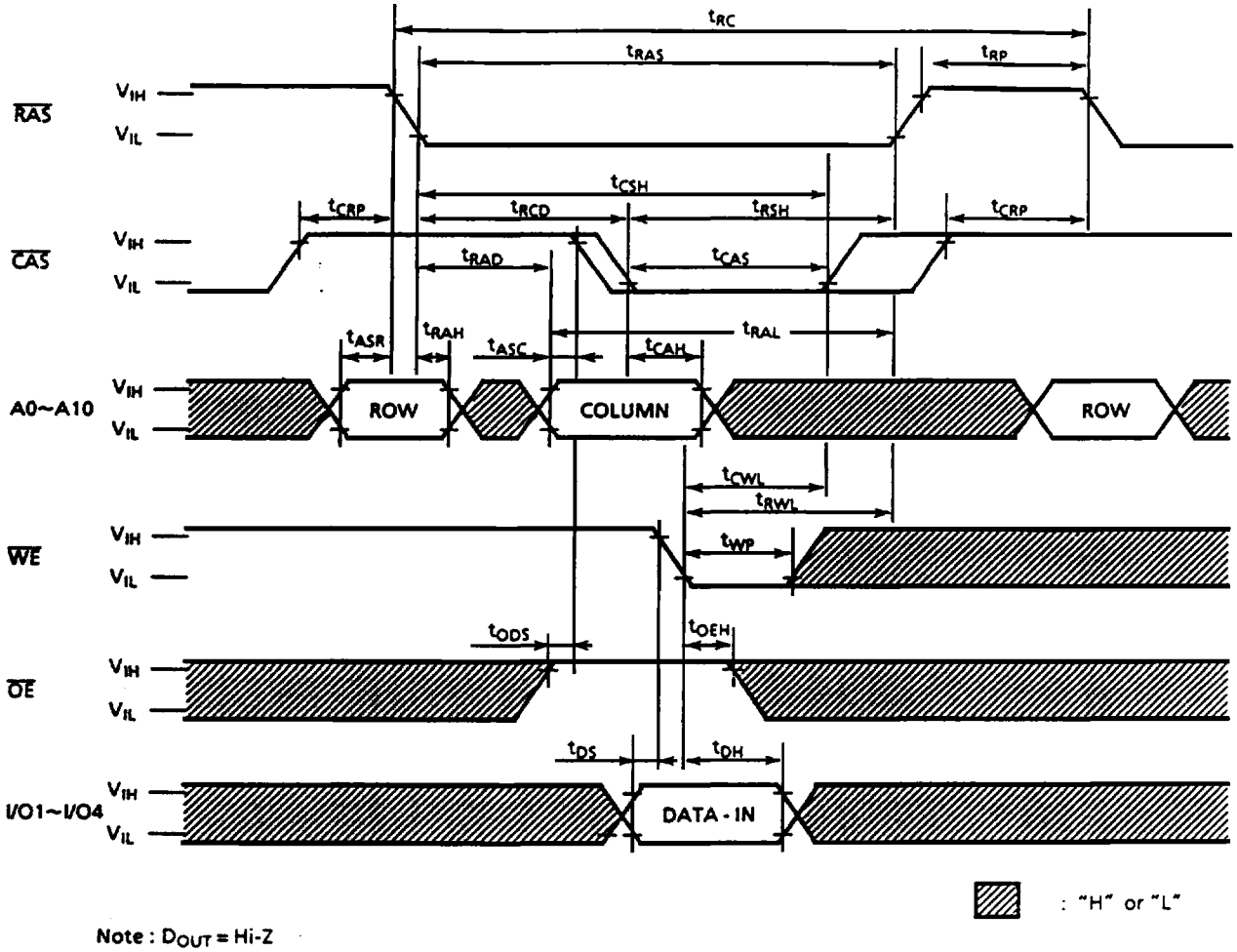
WRITE CYCLE (EARLY WRITE)



: "H" or "L"

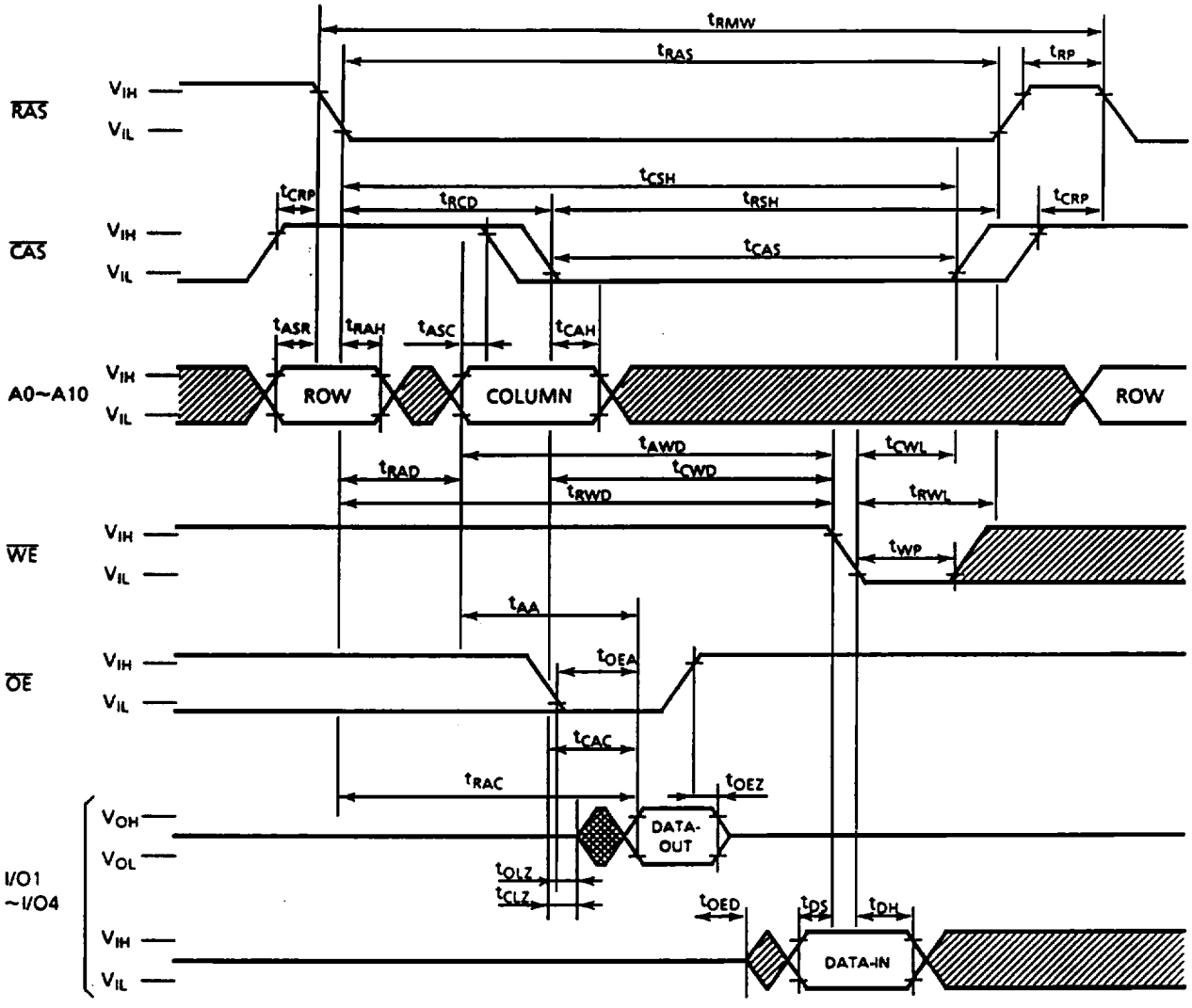
Note : D_{OUT} = Hi-Z

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note : D_{OUT} = Hi-Z

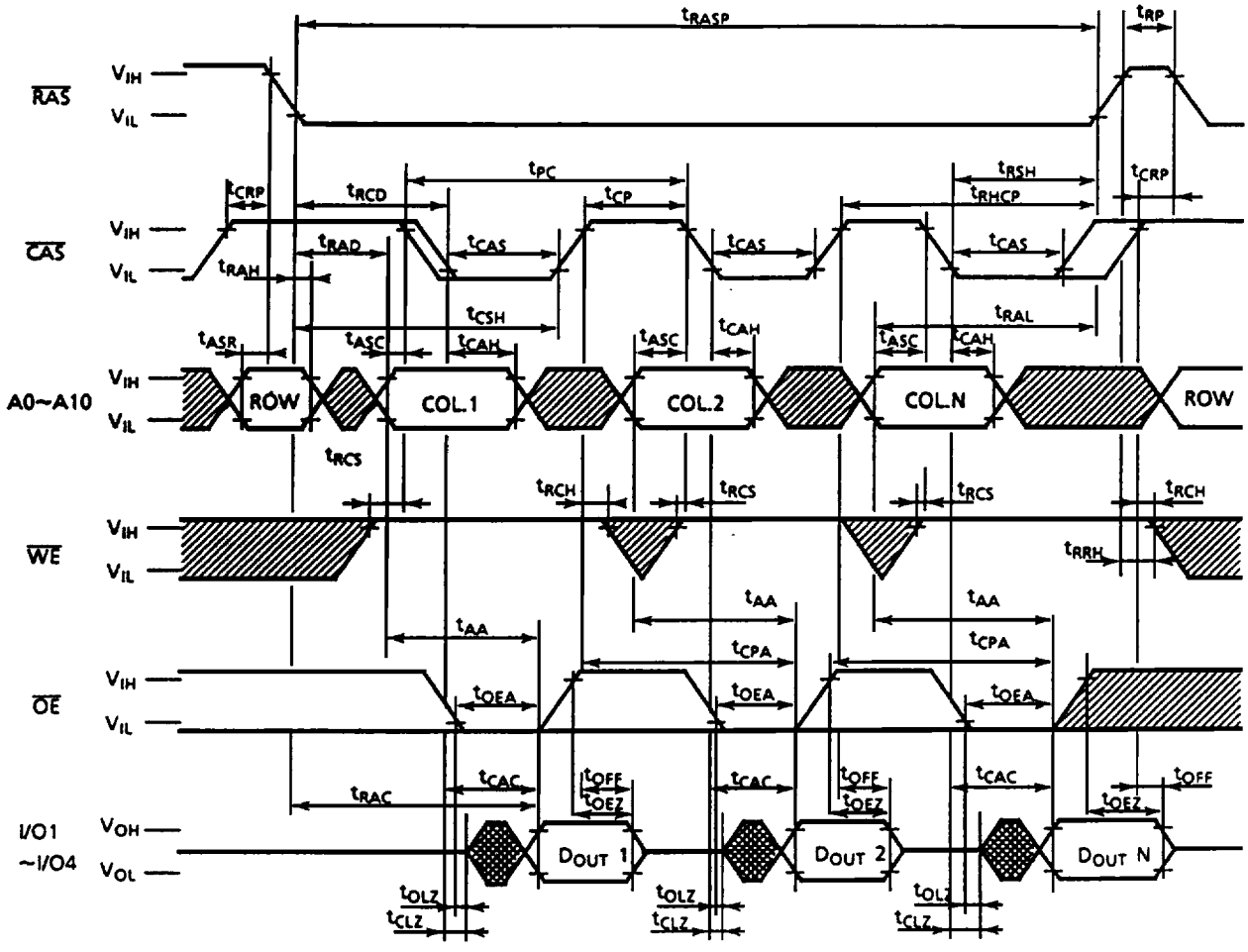
READ-MODIFY-WRITE CYCLE



: "H" or "L"

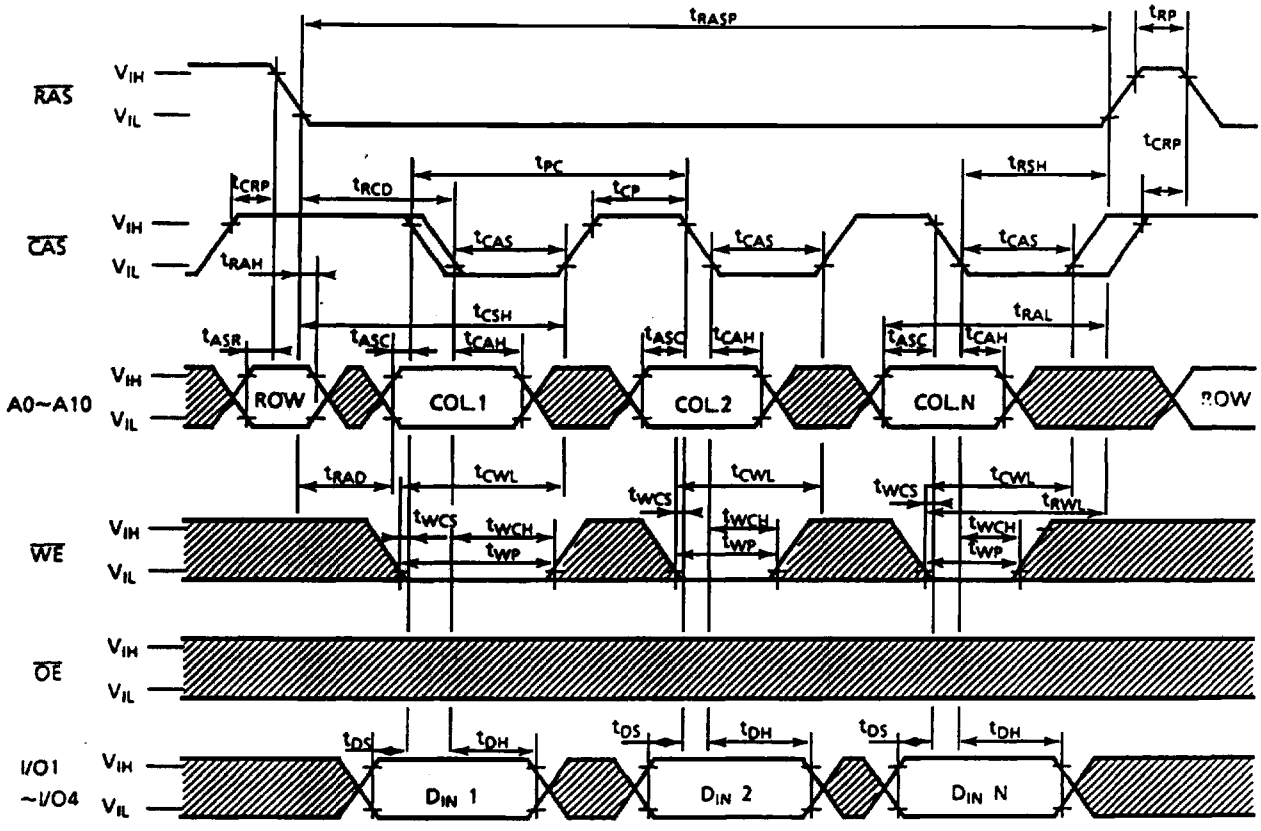
: Invalid Data

FAST PAGE MODE READ CYCLE



Note : D_{IN} = Hi-Z

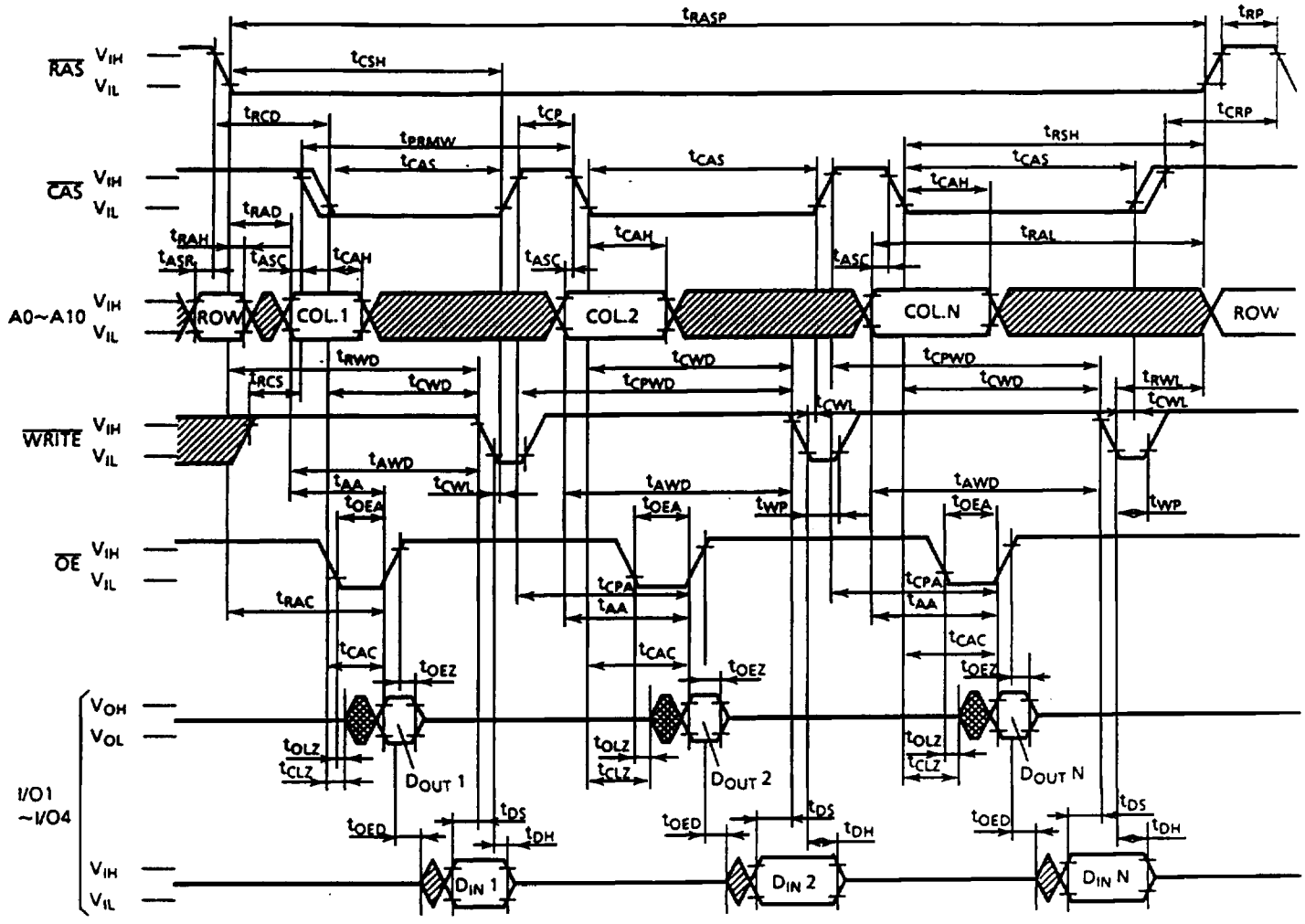
FAST APGE MODE WRITE CYCLE (EARLY WRITE)



Note : D_{OUT} = Hi-Z

▨ : "H" or "L"

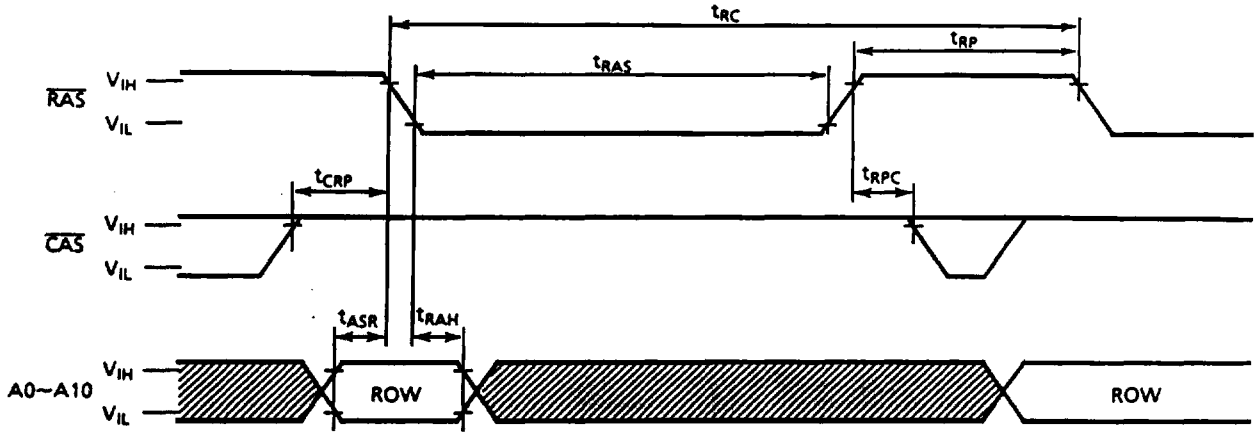
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



: "H" or "L"

: Invalid Data

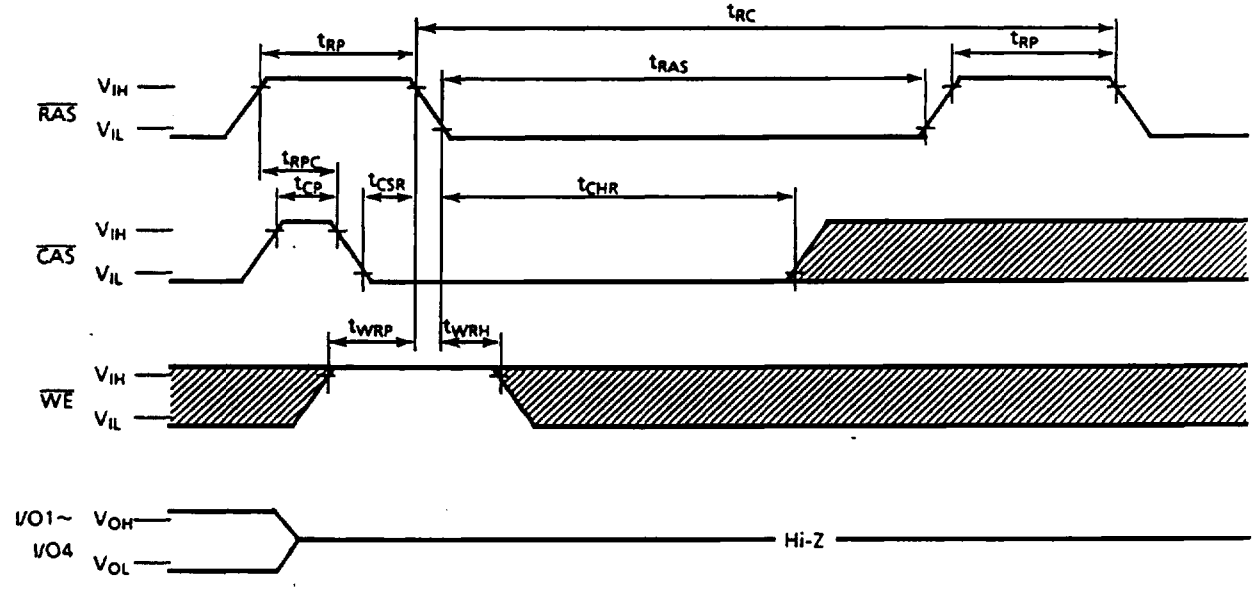
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{WE}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

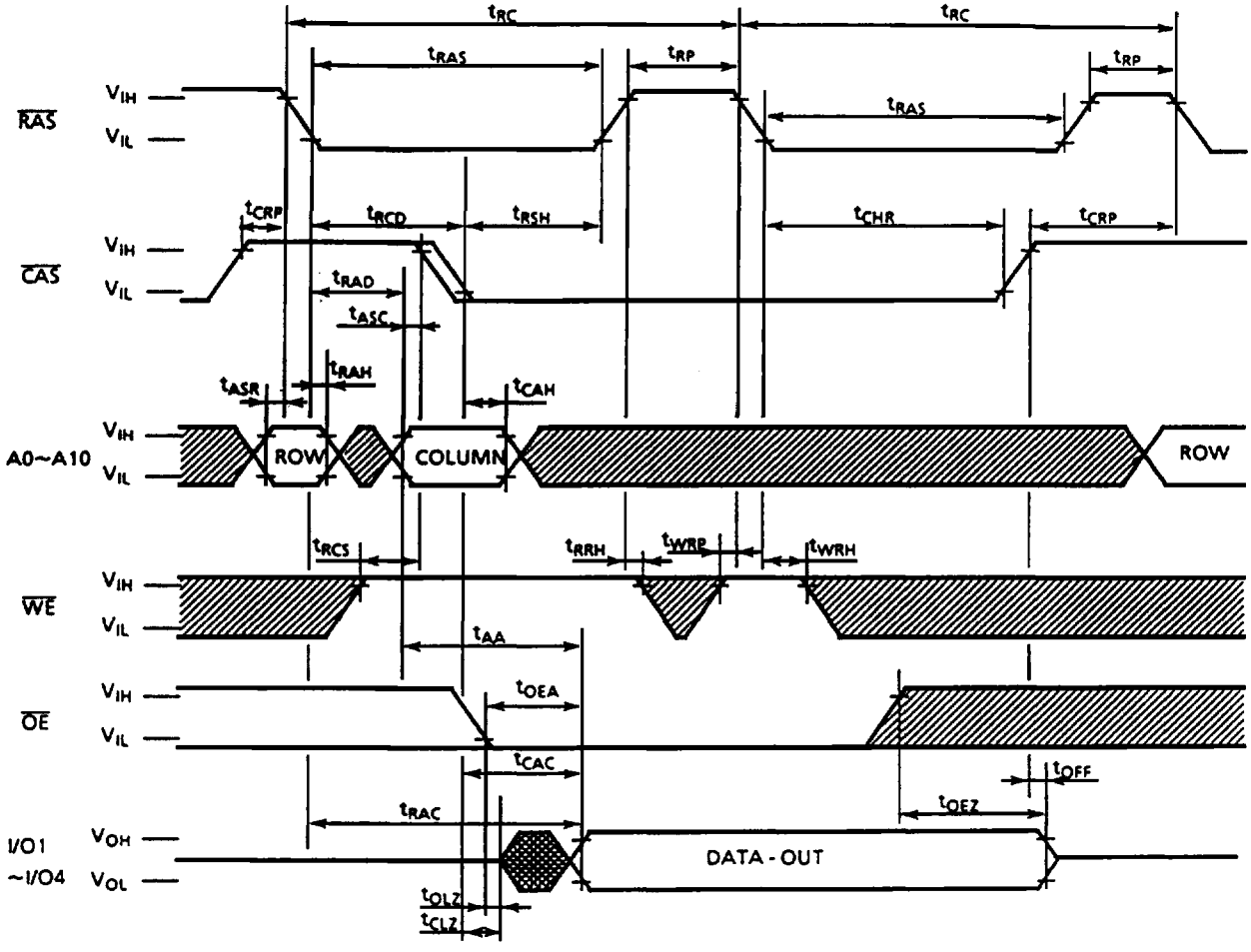
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{OE}$, A0~A10 = "H" or "L"

▨ : "H" or "L"

HIDDEN REFRESH CYCLE (READ)

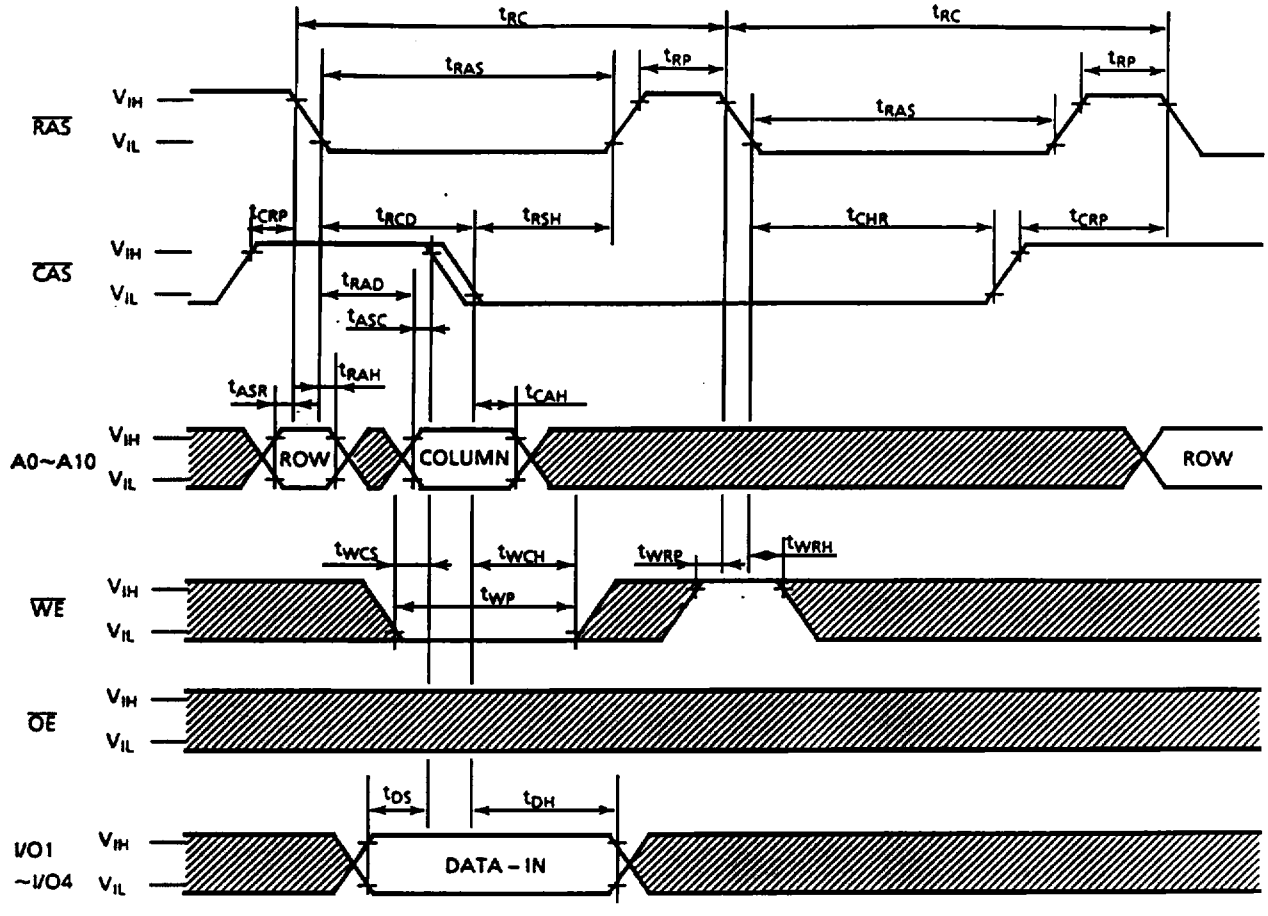


Note : D_{IN} = Hi-Z

▨ : "H" or "L"

▩ : Invalid Data

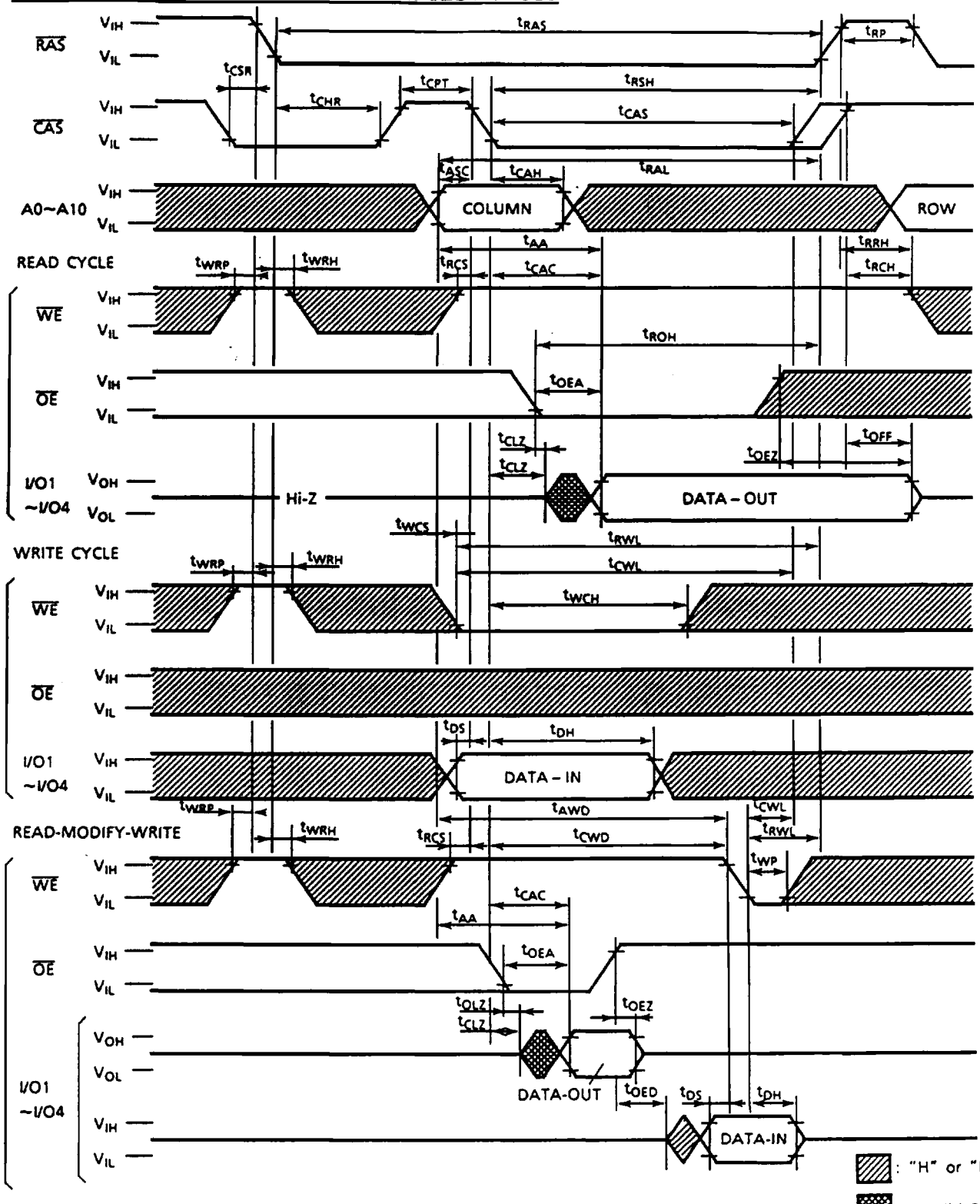
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = Hi-Z

▨ : "H" or "L"

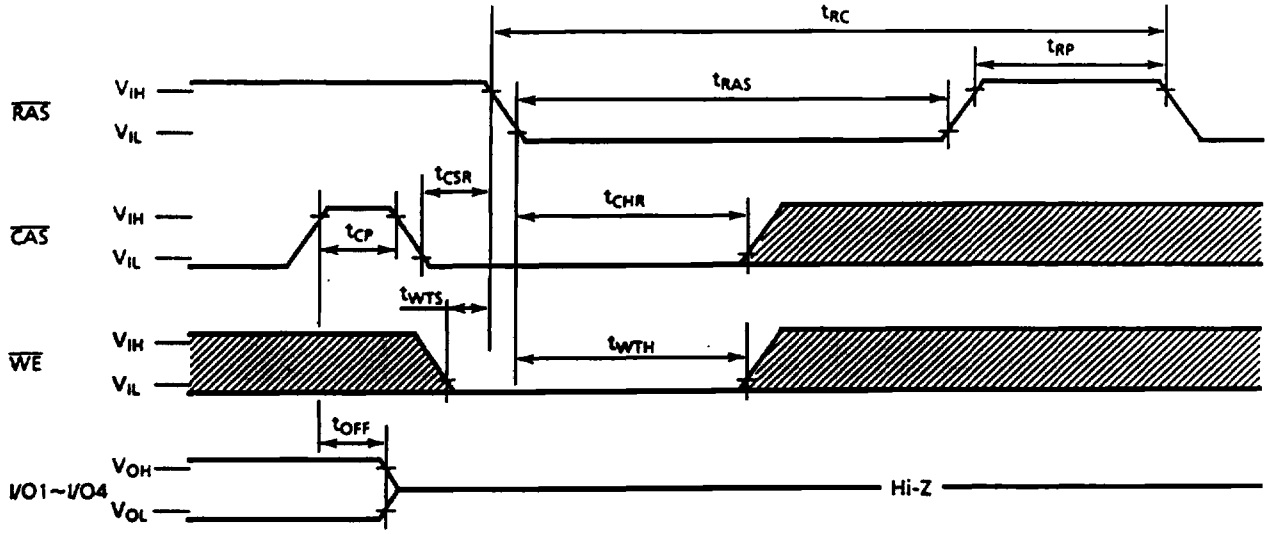
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



: "H" or "L"

: Invalid Da

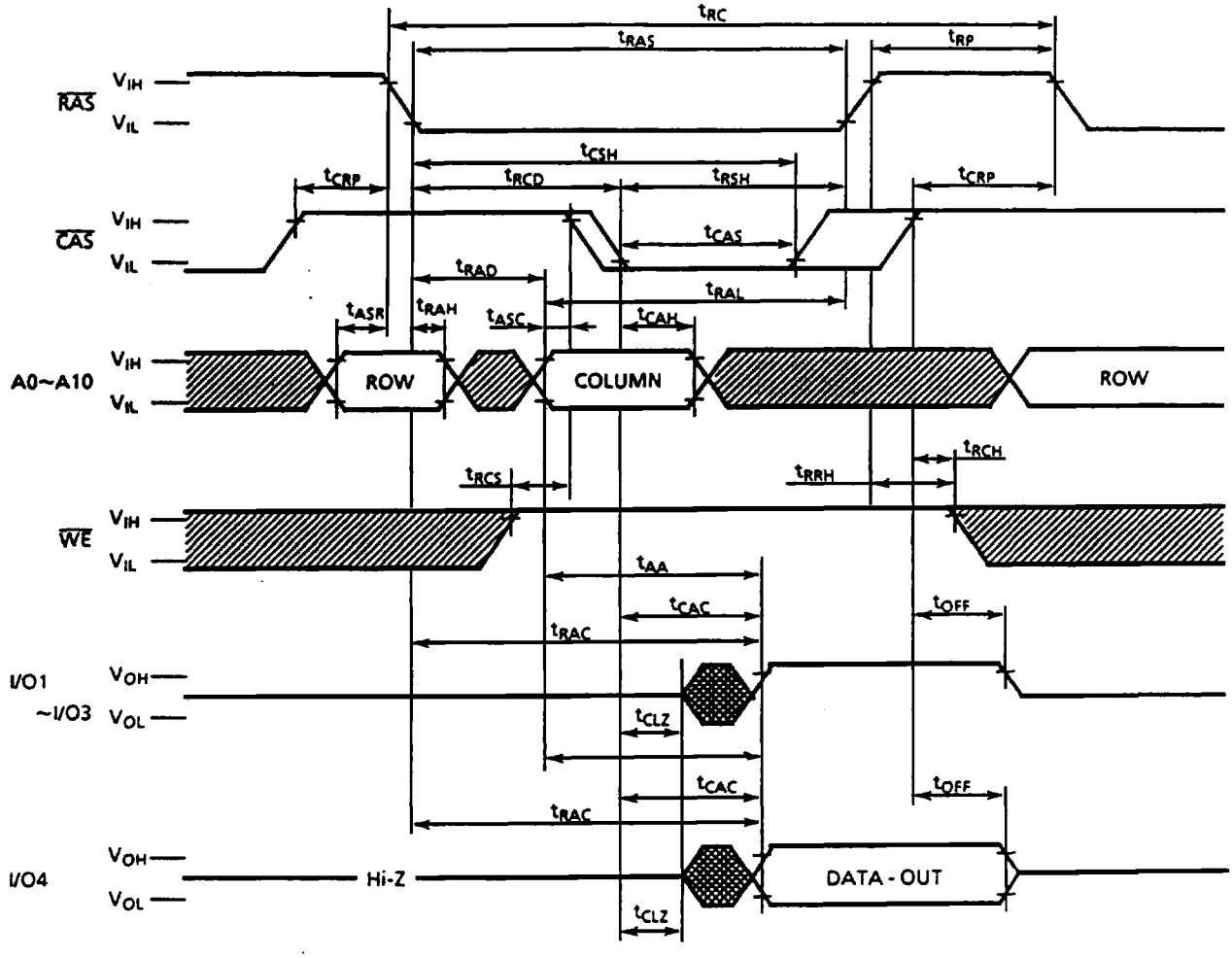
WE, CAS BEFORE RAS REFRESH CYCLE



▨ : "H" or "L"

Note : D_{IN}, $\overline{OE}$, A0~A10 : "H" or "L"

READ CYCLE IN THE TEST MODE

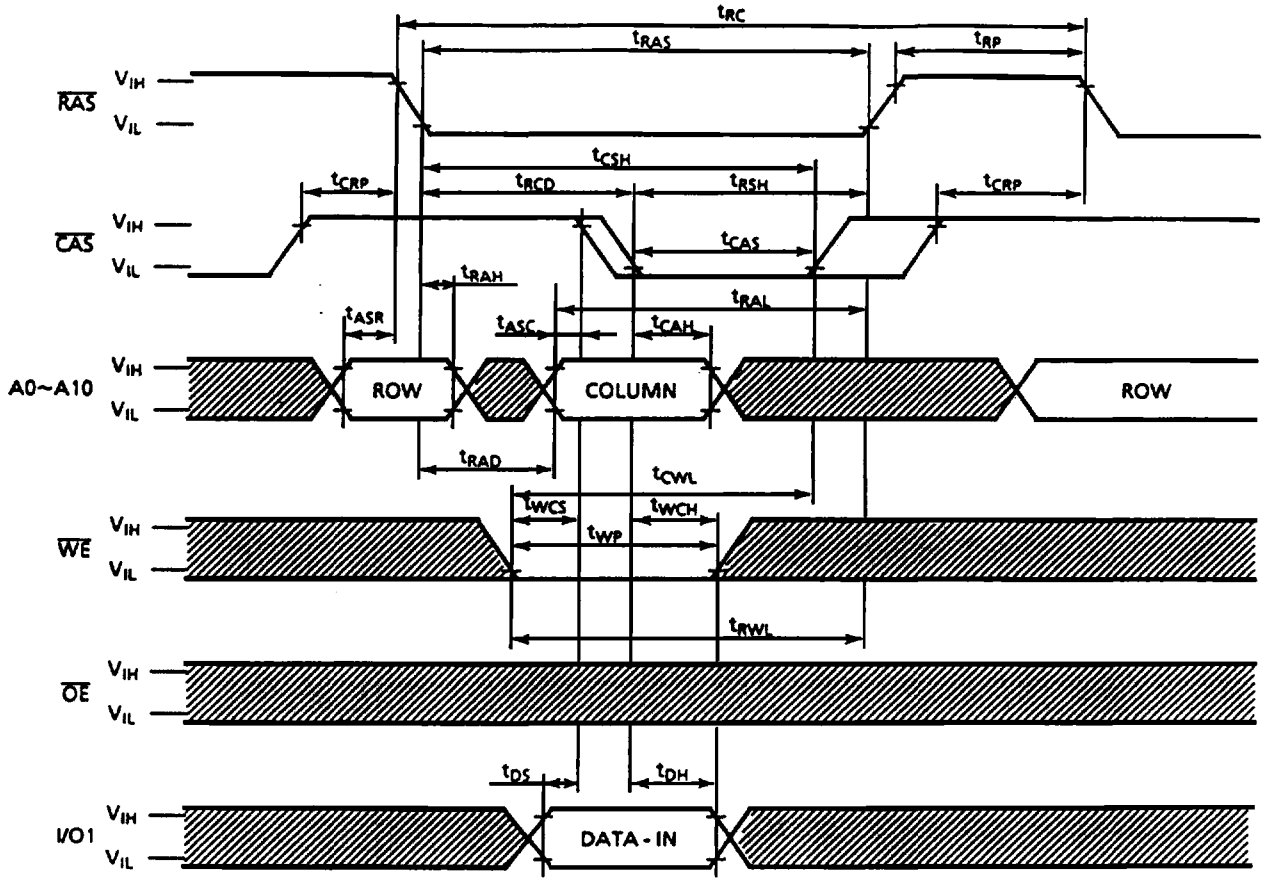


Note : $\overline{OE}$="L" , D_{IN}=Hi-Z

: "H" or "L"

: Invalid Data

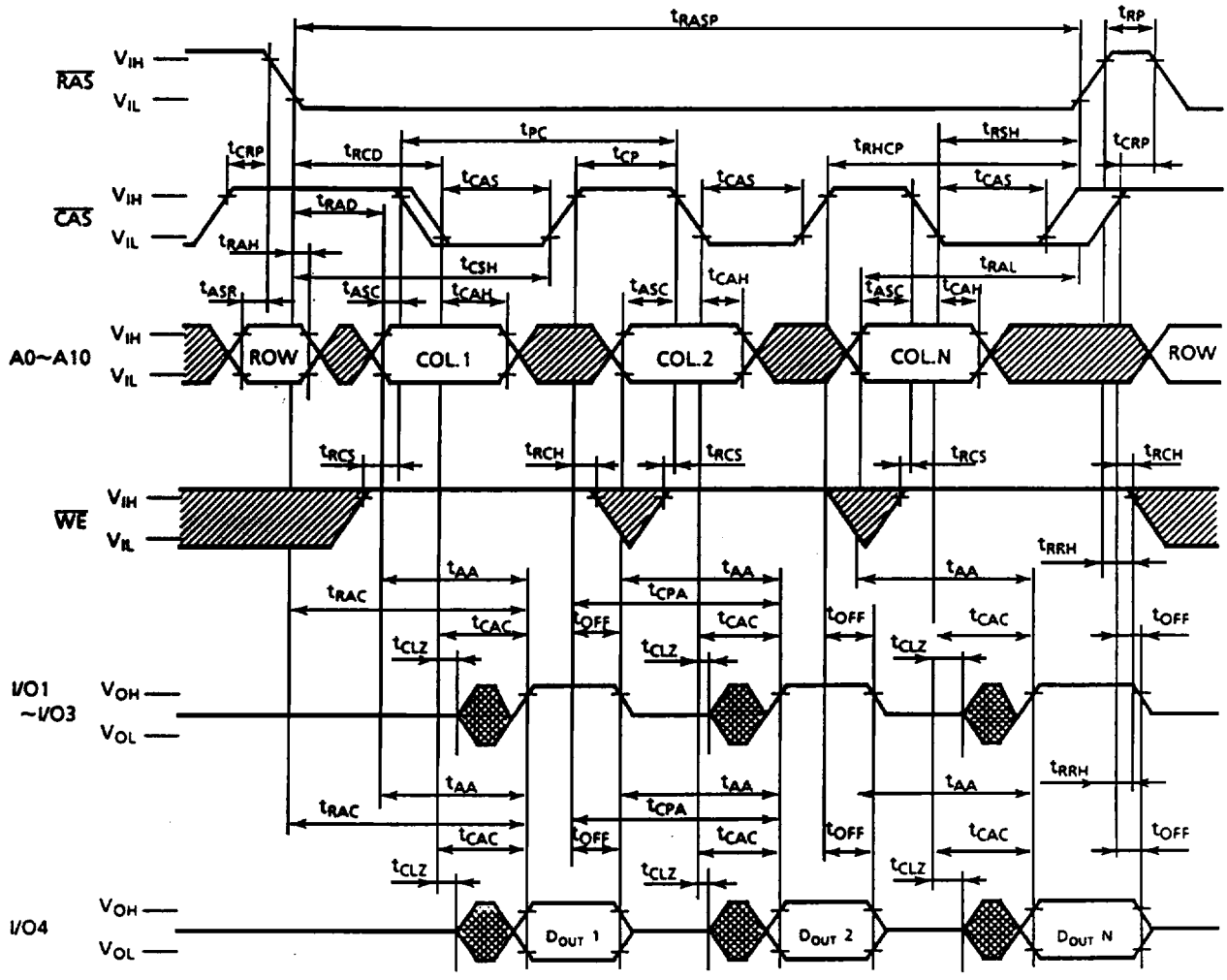
WRITE CYCLE (EARLY WRITE) IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = Hi-Z

: "H" or "L"

FAST PAGE MODE IN THE TEST MODE

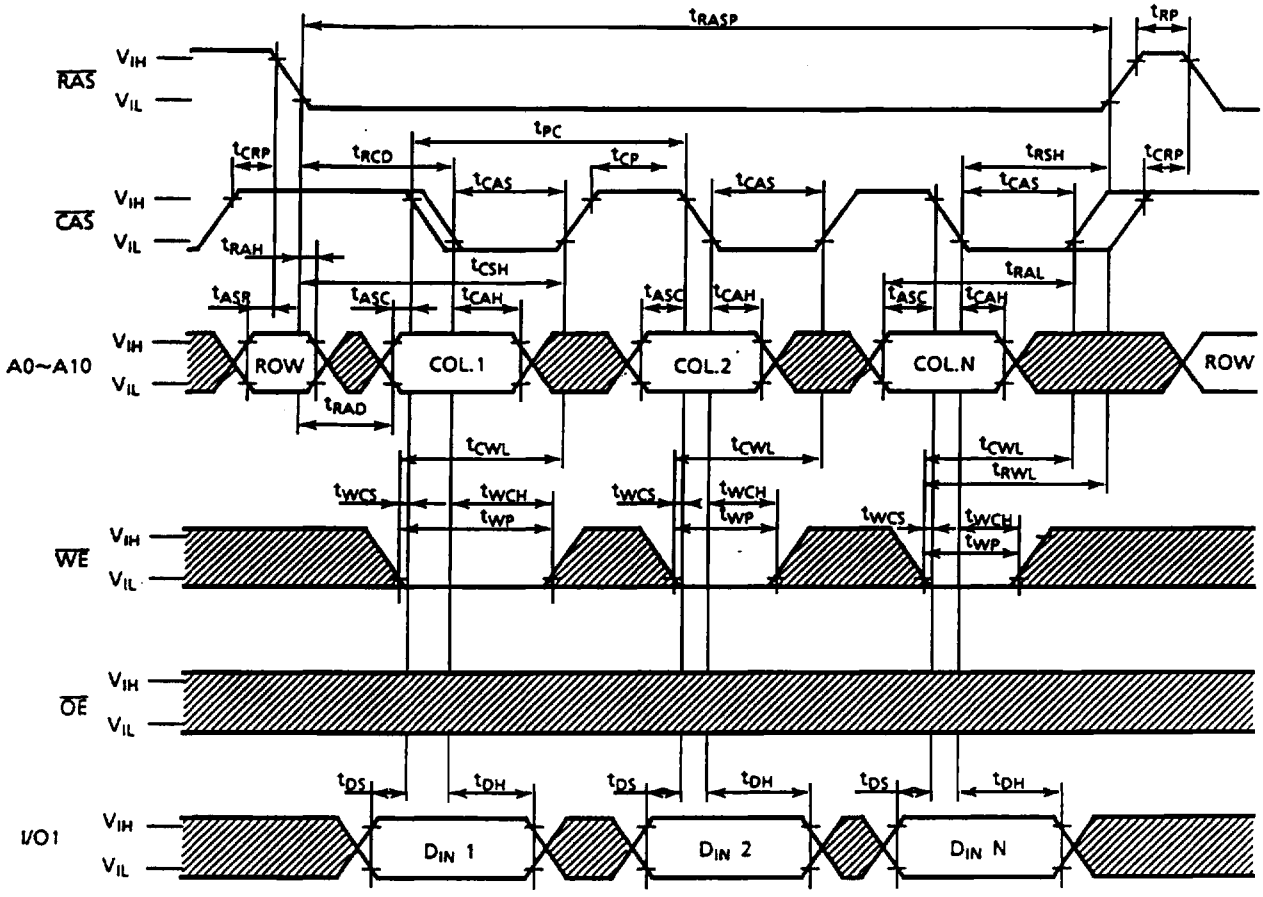


Note : $\overline{OE}$ = "L" , D_{IN} = Hi-Z

: "H" or "L"

: Invalid Data

FAST PAGE MODE WRITE CYCLE IN THE TEST MODE



Note : I/O2~I/O4 = "H" or "L" , D_{OUT} = Hi-Z

TEST MODE

The TC5117400CSJ/CST is the RAM organized 4,194,304 words by 4 bits, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel by using only I/O1. A1c , A0c are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s), the I/O4 pin indicates a "1". If they were not equal, the I/O4 pin would indicate a "0". I/O1 , I/O2 and I/O3 always indicate a "1" during test mode read cycle. Fig.1 shows the block diagram of TC5117400CSJ/CST. In "Test Mode", the 4M×4 DRAM can be tested as if it were a 1M×16 DRAM.

"$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle puts the device into "Test Mode". And "$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, "$\overline{WE}$, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle" Performs the refresh operation with the internal refresh address counter. The "Test Mode" function reduces test times (1/4 in case of N test pattern).

BLOCK DIAGRAM IN TEH TEST MODE

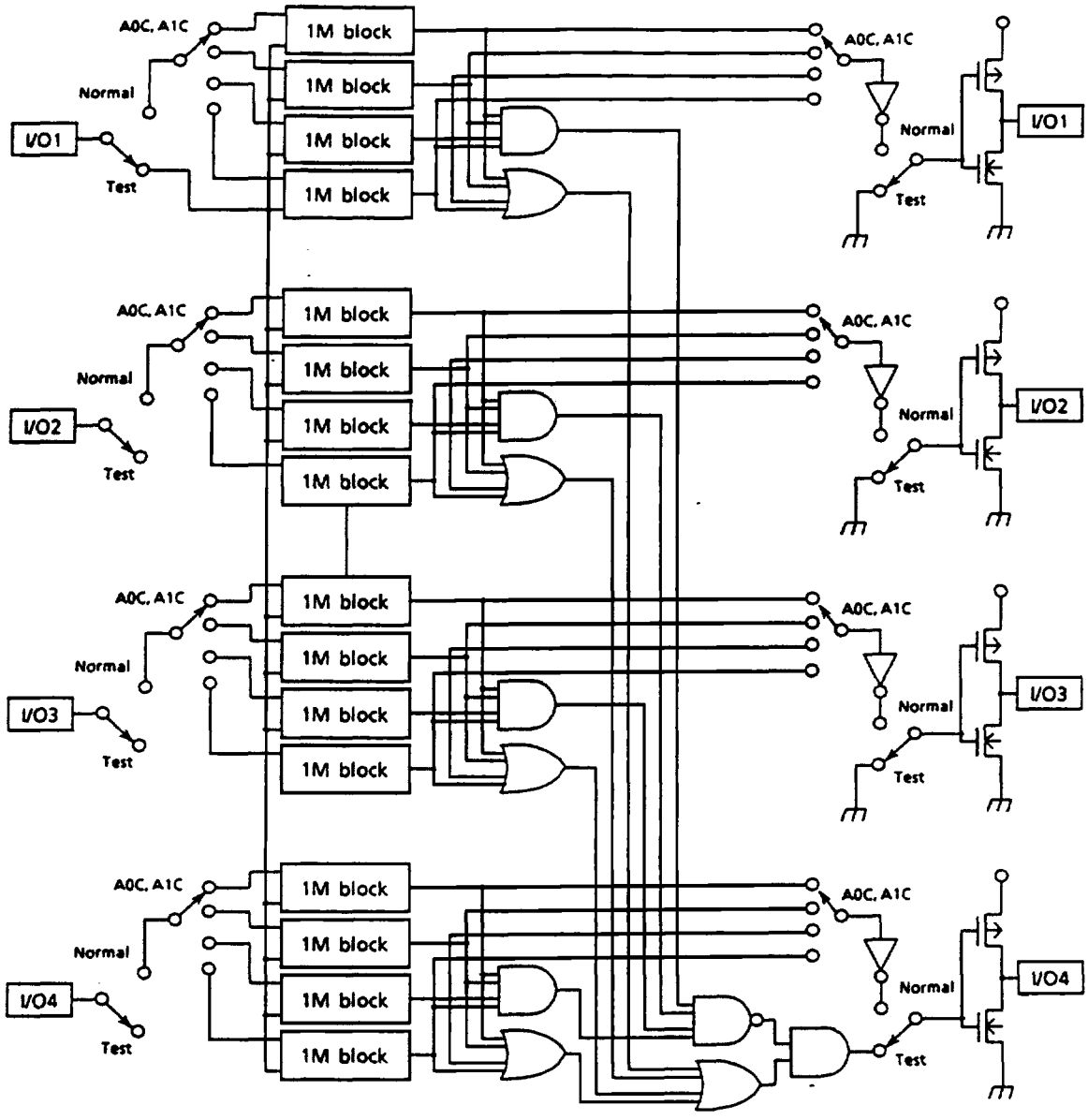
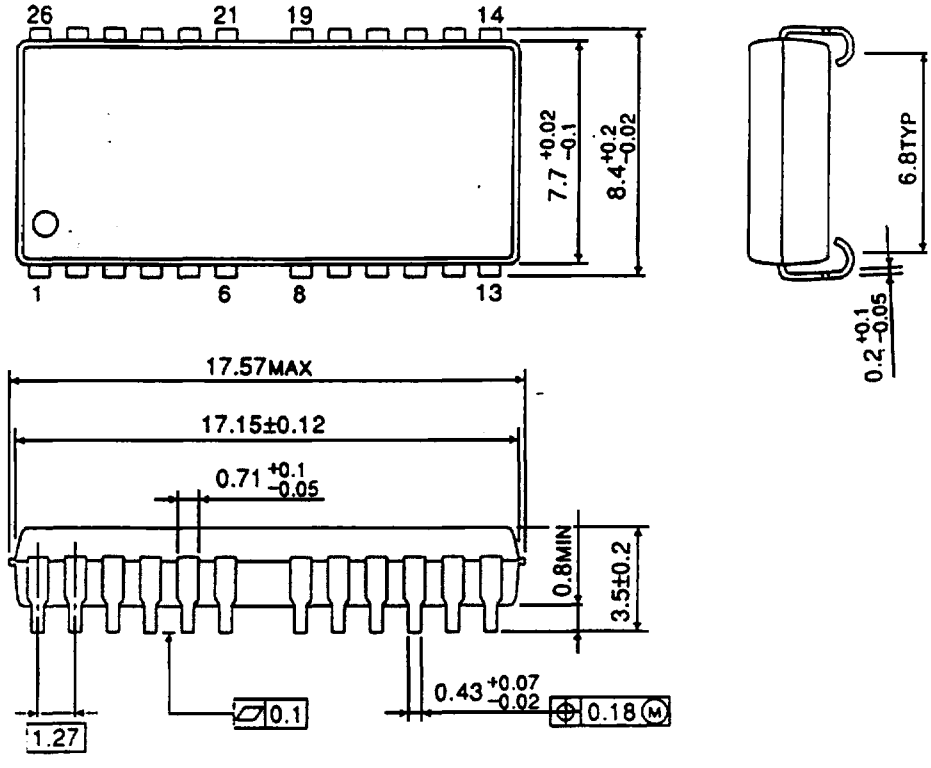


Fig. 1

OUTLINE DRAWINGS (SOJ26 – P – 300C)

Unit in mm



OUTLINE DRAWINGS (TSOP26 – P – 300D)

Unit in mm