Award Modular BIOS v4.50G for Soyo 30F2 VLB/PCI 486 board
11/24/94-OPTI-802G-822-2A4UKS21-00 REV. C2

CPU support list

Cmos_3Dh BIOS_uP_ID bit 0 = FPU	CPU string	Reset word	Other detection	Cmos_3Fh option flags	Detection sequence
00	80386DX	0300h – 030Fh		00	5
01	"				
02	80386SX	2300h – 230Fh		00	6
03	"				
04	RapidCAD	0340h – 034Fh		00	7
05	"				
06	Unknown	0000 – FFFFh		00	14
07	80486DX	0400h – 041Fh		00	10
08	80486SX	0420h – 042Fh		00	11
09	80487SX		80486SX + FPU	00	16
0A	80486SX2	0430h – 04FFh		40h	12
0B	80486DX2		80486SX2 + FPU or Reset word 440h–451h/490h and Cx DIV false	40h 50h	16 17
0C	Cx486SLC		Unkown CPU; Cx DIV OK; DIR0≠02h or 1Bh	00	18
0D	"				
0E	Cx486DLC		80486SX; and Cx DIV OK	00	19
0F	"				
10	P24T				
11	"				
12	"				
13	"				
14	"	1530h – 153Fh		50h	13
15	"				
16	Cx486S	0440h – 0450h		10h	8
17	"				
18	Cx486S2	0451h – 0451h		50h	9
19	"				
1A	PENTIUM				
1B	“	0500h – 05FFh		00	4

1C	Unused				
1D	"				
1E	"				
1F	"				
20	"				
21	"				
22	Cx486DX				
23	"				
24	"				
25	"	0490h – 0490h	DX4; Cx DIV OK; DIR0≠02h or 1Bh	10h	3/20
26	Cx486DX2				
27	"		DX4; Cx DIV OK; DIR0=02h or 1Bh	50h	20
28	Cx486SLC2		Unkown CPU; Cx DIV OK; DIR0=02h or 1Bh	50h	18
29	"				
2A	DX4				
2B	"	1480h – 148Fh 0480h – 048Fh		90h	1 2
2C	TI486SXL		Cx486SLC+TI test	10h	21
2D	"				
2E	TI486SXL2		TI486SXL; > 48MHz	50h	24
2F	"				
30	U5 486SX		FS: SALC ->
EAX=AB6B1B07h	10h	15
31	"				
32	Am486DX		??	10h	
33	"				
34	P54C				
35	"				
36	TI486SXLC		Cx486DLC+TI test	10h	21
37	"				
38	TI486SXLC2		TI486SXLC; > 48MHz	50h	24
39	"				
3A	Am486DX2		??	50h	
3B	"				
3C	P24D				
3D	"		CPUID: Intel ->
0470h – 047Fh	50h	22
3E	Am486DX4				
3F	"		80486DX2; ≥ 90MHz	90h	23

CMOS registers bit definition:

Bits 6-0 in **CMOS_3Dh** byte represent the BIOS_uP_ID and a “1” in bit 7 means L1 cache is present. The bits in **CMOS_3Fh** byte represent additional CPU data:

Bit 7 = clock tripling CPU
Bit 6 = clock doubling CPU
Bit 5 = reserved
Bit 4 = Green CPU (in older BIOS versions, this is bit 5)
Bits 3-0 are reserved.

Notes on software tests:

- FPU: A test to determine if the CPU has a Floating Point Unit (=Math coprocessor).
- Cx DIV: This is a test that identifies a Cyrix CPU, including IBM, ST, and TI CPUs based on the Cyrix design. These CPUs do not change unrelated flags in the Flags Register after a Divide operation. CPUs from other vendors do.
- DIR0: Device Identification Register 0 is present on all Cyrix design CPUs, except the Cx486S A-step. Its contents can be used to identify a specific Cyrix processor.
- TI test: This is a sequence of instructions acting on the test registers TR4 and TR5 that produces a specific result only on TI CPUs.
- FS: SALC: This undocumented instruction with opcodes 64h, 0D6h, produces a specific result in the EAX register only on UMC CPUs.
- CPUID: This instruction returns detailed information about a CPU. CPUID is supported by the Pentium and a handful of later 486’s. So most 486 CPUs don’t support this instruction and a more widespread use of CPUID is seen only in 1995 and later Award BIOSes.