CIRCUIT DESCRIPTION

BtV2115 Interface

Access to the BtV2300 is available only through the BtV2115 MediaStream Controller via a three-wire digital interface. The BtV2115 maintains an internal copy of the BtV2300's register data for fast MPU access.

Digital audio data and control data are transferred from the BtV2115 to the BtV2300 via the SA_IN pin. Digital audio data and control data are transferred from the BtV2300 to the BtV2115 via the SA_OUT pin. A clock signal (ACLK) is also transmitted from the BtV2115 to the BtV2300.

SA_IN Input

Manchester-encoded digital audio data and internal register data are input to the BtV2300 via the SA_IN pin. The format of the data on this pin is compatible with EIA-J CP-340 (1987) except that TTL levels are used. The SA_IN stream comes from the BtV2115. The BtV2300 uses digital techniques, instead of a PLL, to separate clock and data on the SA_IN input.

The smallest unit of data in the SA_IN stream is a subframe (shown in Figure 1), which consists a 4-bit preamble, a 20-bit 2's complement PCM sample of audio data (LSB first), and four AUX control bits. It is important to note that the SA_IN interface is real-time; as digital audio samples are received, they are converted to analog signals and output.

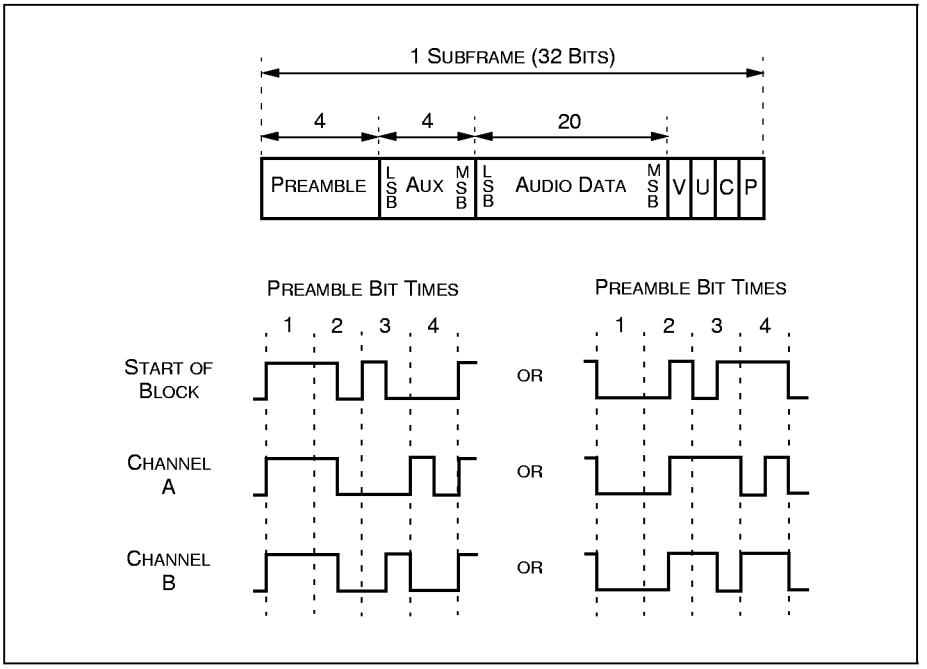
Two subframes (for two channels of audio) make a frame and a variable number of frames make a block. The 4-bit preamble of each subframe is used to identify that subframe as either subframe A (left channel), subframe B (right channel), or the first subframe (always subframe A) of a block.

The parity bit (P) is the even parity of all bits in the subframe, except the preamble. If a parity error is detected, the SA_IN decoder will become unlocked and incoming data will be ignored.

The validity bit (V) indicates if the audio samples in the subframe are secure and error-free (V = 0) or defective (V = 1). If a validity error (V = 1) is detected, the incoming data is ignored. Incoming data may intentionally be ignored by setting the validity bit low.

The channel status bits (C) and user data bits (U) of each subframe are ignored.

Figure 1. SA_IN and SA_OUT Subframe and Preamble Formats



The AUX bits of both the A and B subframes are used to transfer data to the internal control registers of the BtV2300. The eight aux bits of each SA_IN frame are used to address the BtV2300's internal eight-bit registers. The eight aux bits in the first frame of a block select the first register to be programmed. The internal address counter begins at this register and autoincrements on subsequent frames. For instance, if the first frame selects register N, the aux data from the second frame would be loaded into register N, the aux data from the third frame would be loaded into register N+1, and so on. When the address counter increments to the last register, autoincrementing stops and aux data is ignored until another block is received.

Programming a nonexistent register (address ≥ 18) will cause the BtV2300 to ignore incoming aux data until another block is received. A description of the BtV2300 registers begins on page 11.

SA_OUT Output

Digitized audio data and internal register data are output from the BtV2300 via the SA_OUT pin. The format of the data on this pin is compatible with EIA-J CP-340 (1987) except that TTL levels are used. The block length of the SA_OUT stream is 192 frames.

The BtV2300 revision ID is output in the aux bits of the first SA_OUT frame of each block. The ID for Rev. A is 0x06 during normal operation and 0x07 during offset calibration. The ID for Rev. B is 0x0E during normal operation and 0x0F during offset calibration. The aux fields of subsequent SA_OUT frames contain the data read back from APP[7:0]. When an APP pin is programmed as an input,

the externally applied value is read back. When programmed as an output, the programmed value is read back.

The channel status bits (C) and user data bits (U) of each subframe are set to "0".

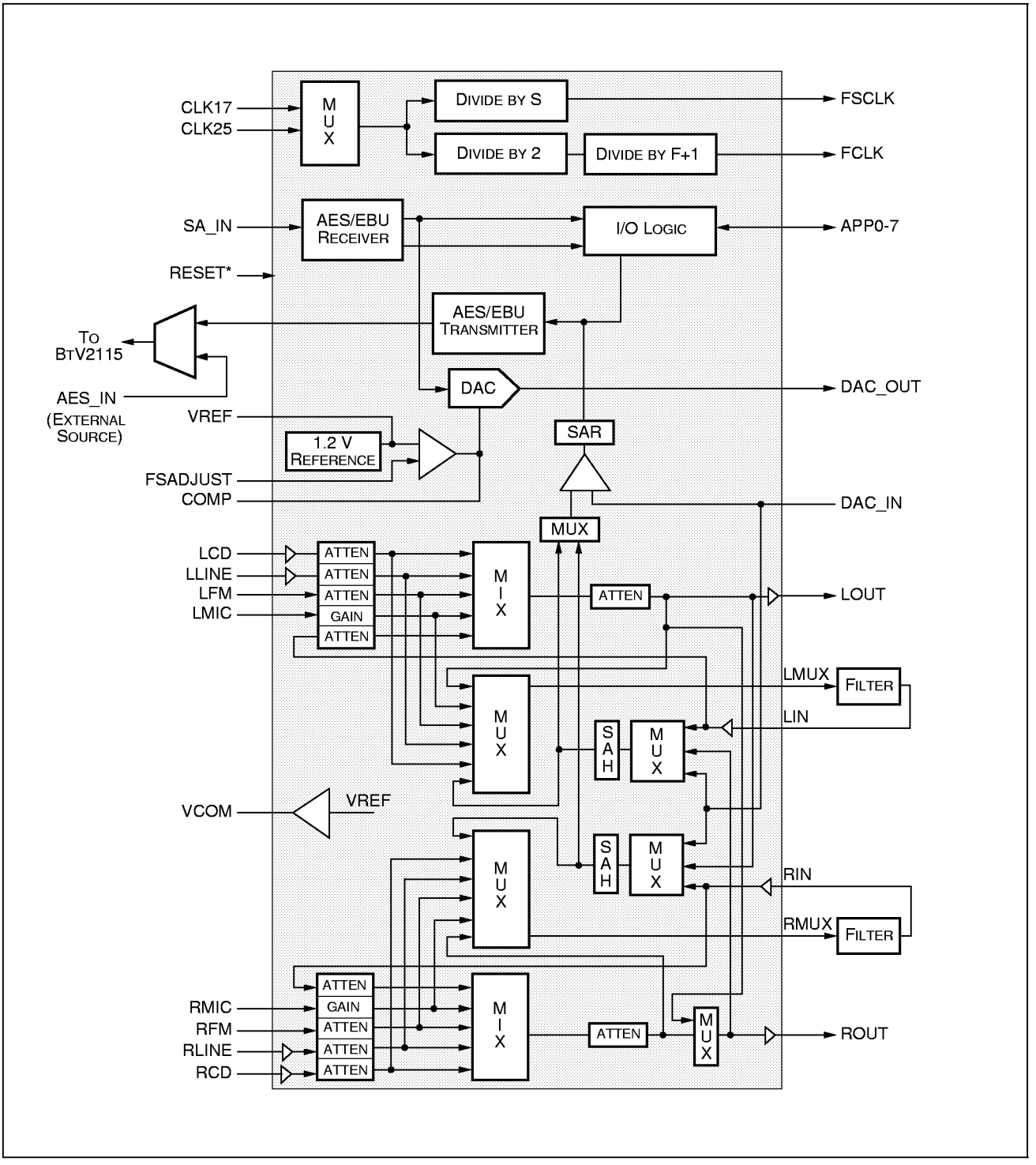
If the stereo output mode is selected, the digital audio data present on SA_OUT is "0" for both channels, with the invalid bits set (V = 1). All of the channel status bits are also set to "0".

The BtV2300 can be programmed to route its SA_IN input directly to the SA_OUT pin to be sent to the BtV2115. This allows the BtV2115 to process the digital outputs of consumer audio products (CD, MD, DAT and DCC players) without unnecessary digital to analog conversion. The SA_OUT pin can also be asynchronously three-stated through register programming to offer hardware access to the BtV2115.

Table 1. BtV2300 Part IDs for Rev. A and Rev. B

Part Revision	ID During Normal Operation	ID During Offset Calibration
Rev. A	0x06	0x07
Rev. B	0x0E	0x0F

Figure 2. BtV2300 Detailed Block Diagram



Analog Inputs

The BtV2300 has three types of analog inputs which can be selected through the MUX for A/D conversion, or mixed to provide a line-level output.

MIC Inputs

The MIC inputs (LMIC, RMIC) have +6 dB to +51 dB of gain, plus mute capability. Because the MUX has a minimum of +6 dB gain, the maximum input level of the MIC is 500 mVpp. Beyond this level, the MUX outputs (LMUX, RMUX) will clip. For every additional 6 dB of gain in the MIC path, the maximum input level at the MIC input decreases by one half.

Increasing the MIC input gain above +6 dB will increase both the noise floor and the harmonic distortion. Keeping the MIC gain between +6 dB and +21 dB will insure good sound quality. If additional gain is required, use an external amplifier as close as possible to the microphone jacks.

The MIC inputs are pulled to 1.5 V (VCOM) through 20 KΩ resistors. Audio signals should be coupled to the MIC inputs through a 1 µF or greater capacitor.

CD and LINE Inputs

The CD and Line inputs (LCD, RCD, LLINE, RLINE) have +6 dB to +51 dB of programmable attenuation as well as mute capability.

These inputs are internally buffered and have a high (>100 KΩ) input impedance. Audio signals should be coupled to these inputs through a 0.1 µF capacitor. In addition, these inputs must be pulled to VCOM through 1 MΩ resistors. These inputs may be DC coupled if the input signal is centered around VCOM. However, any offset from VCOM will introduce clicking when changing MUX or attenuation settings.

FM Inputs

The FM inputs are identical to the Line and CD inputs, except they are not internally buffered; their input impedance will vary from 20 KΩ to 12.8 KΩ. These inputs should be driven from a low impedance output (<<10 KΩ) to minimize gain error. The FM inputs are pulled internally to 1.5 V (VCOM). Audio signals should be coupled to these inputs through a 1 µF or greater capacitor.

Analog Multiplexer

The BtV2300 contains one analog multiplexer per channel to route LLINE/RLINE, LCD/RCD, LFM/RFM, LMIC/RMIC or left/right DAC to the LMUX/RMUX outputs. The multiplexers have selectable +6 dB or +12 dB gain. The minimum gain setting, +6 dB, compensates for the –6 dB attenuation of the input attenuators to give an overall gain of 0 dB. The LMUX/RMUX outputs must be applied to an external low pass filter as described in DAC Implementation and ADC Implementation.

Analog Mixer

The BtV2300 contains one analog mixer per channel to drive the main analog outputs, LOUT and ROUT, by summing LCD/RCD, LLINE/RLINE, LFM/RFM and LIN/RIN. The mixer outputs drive attenuators with –6 dB to –51 dB programmable attenuation, and mute capability. The mixers have +6 dB to +12 dB programmable gain. The minimum gain setting, +6 dB, compensates for the –6 dB attenuation of the input attenuators.

Internal A/D, D/A Conversion

The BtV2300 uses a single, time-multiplexed DAC for A/D and D/A conversion.

DAC Implementation

The DAC output is demultiplexed by two sample and holds which are clocked at 16xFs. (Note that the DAC data is updated at 1xFs; the sample and holds are oversampled to reduce their noise contribution.)

The DAC output must be postfiltered by an external filter. Because the DAC operates at 1xFs, the filter must have a corner frequency of Fs/2, and significant attenuation at Fs. Since these cutoffs must track the sample rate, a switched capacitor filter clocked by the BtV2300's FCLK output is recommended.

To postfilter the demultiplexed left and right DAC outputs, select the DAC through the multiplexer to the LMUX/RMUX outputs, apply the LMUX/RMUX signals to the external filters, and apply the filter's output to the LIN/RIN inputs. The lowpass filtered DAC outputs can be selected through the mixer to the LOUT/ROUT outputs.

ADC Implementation

When configured to perform A/D conversion, the BtV2300 uses the internal DAC, SAR and comparator to digitize the signals present on the LIN/RIN inputs. The internal sample and holds on the LIN/RIN inputs are clocked at 1xFs and there is a fixed delay of one half of a sample period between the sampling of the left and right channels.

Because the inputs are sampled at 1xFs, and because no internal anti-aliasing is performed, an external filter is needed to bandlimit the inputs to LIN/RIN to Fs/2. This filter (the same filter used to anti-alias the DAC outputs) should cut off sharply at Fs/2, and provide significant attenuation at Fs to limit aliasing of high frequency signals into the ADC output.

To filter and convert an analog signal, select the desired input through the multiplexer to the LMUX/RMUX outputs, apply the LMUX/RMUX outputs to the external filters, and apply the filters' outputs to the LIN/RIN inputs. The LIN/RIN inputs are then sampled for A/D conversion by the sample and holds.

Conversion Modes

The BtV2300 supports three conversion modes at sample rates up to 48 KHz.

Stereo Output Mode

The left and right audio samples from the SA_IN datastream are converted and demultiplexed. The DAC output must be selected on LMUX and RMUX for postfiltering. The left and right audio samples in the SA_OUT datastream are set to zero.

Stereo Input Mode

The left and right audio samples in the SA_OUT datastream contain the results of the A/D conversion of the LIN and RIN inputs. One of the analog inputs must be selected on LMUX and RMUX to be filtered and applied to LIN and RIN.

The left and right audio samples from the SA_IN datastream are ignored.

Mono I/O Mode

In Mono I/O mode, the left channel is used for digital input, and the right channel is used for analog input.

The left audio sample from the SA_IN datastream is converted and demultiplexed, and the right audio sample is ignored. The left channel's external filter is used for postfiltering, so the DAC output must be selected on LMUX, sending the audio to the left channel's external filter. The left channel mixer output is sent to ROUT as well as LOUT.

To play back stereo data in Mono I/O mode, the BtV2115 will average the left and right signals and send them to the BtV2300 in the left audio samples of the SA_IN stream.

The left and right audio samples in the SA_OUT datastream contain the result of the A/D conversion of the right channel input (RMIC, RLINE, etc.). The right channel's external filter is used for anti-aliasing. One of the right channel analog inputs must be selected on RMUX for filtering.

Voltage References

VREF The VREF pin is a bypass point for the internal reference circuitry, and should not be used to drive any external circuitry.

VCOM The VCOM pin is the output of an amplifier that steps the internal 1.2 V reference up to 1.5 V. VCOM may be used to bias external circuitry driving the BtV2300's analog inputs. All of the analog inputs (LLINE/RLINE, LCD/RCD, LIN/RIN, etc.) must be centered around VCOM since all of the analog signal paths are designed to operate at VCOM ± 1.0 V.

Offset Calibration

The BtV2300 nulls the offsets of the mixer and microphone amplifiers when a calibration is requested through bit 6 of register 7. Before performing the calibration, program the BtV2300 as follows:

Mute the mixer attenuators.

Mute all mixer inputs.

Set mixer gain to +12 dB.

Unmute the microphone and program the mic gain to 0x1F.

After the calibration is complete, the conditions may be changed as desired. Calibration status may be checked by reading the device ID (see the "SA_OUT Output" paragraph in the "BtV2115 Interface" section).

Clock Operation

Two clocks are input to the BtV2300, CLK17 and CLK25. Either CLK17 or CLK25 is divided by a factor "S" to generate the desired sample clock rate (FSCLK), as shown in Table 2. The FSCLK output is used to clock any external circuitry or test equipment that needs to be clocked at the sample rate (Fs). FSCLK has a duty cycle of 50%.

Table 2. Values of S for Various Sample Rates

Sample Rate (KHz)	Clock Select	Clock Frequency (MHz)	S Divisor		S / 128 Divisor (decimal)
			decimal	hex	
48.0	CLK25	24.576	512	0200	48.0
44.1	CLK17	16.9344	384	0180	44.1
32	CLK25	24.576	768	0300	32
22.05	CLK17	16.9344	768	0300	22.05
11.025	CLK17	16.9344	1536	0600	11.025
8.0	CLK25	24.576	3072	0C00	8.0

The S divisor is divided by 128 to generate the 128xFs clock used to sample the SA_IN input, clock the SA_OUT output, and generate clocking to the ADCs and DACs. The "unlock" bit must be set whenever the value of S is changed, and reset prior to the next block. See "Internal Registers" on page 11 for information regarding the "unlock" bit.

If the 7 LSBs of S are "0", the SA_IN and SA_OUT frame rate corresponds to the audio sampling rate. Thus, there is no dead time between frames since the bit rate is exactly 128x the frame rate. In this case, the 6 MSBs are used to generate a 128x Fs clock.

If the 7 LSBs of S are not "0", the SA_IN and SA_OUT frame rates still correspond to the audio sampling rate, however the bit rate is not exactly 128x the frame rate, thus there is dead time between frames. In this case, the 6 MSBs are used to generate a clock that is the next highest sample rate of 128x Fs. The 7 LSBs specify how much dead time occurs between frames to give additional precision to sample rate selection.

The FCLK output is used to clock external switched capacitor filters. Either CLK17 or CLK25 (whichever is selected) is divided by two and dividing this by a 6-bit divisor (F) generates one-half the FCLK cycle. The value of F should be such that FCLK is 50x the cutoff frequency, Fc, as shown in Table 3. FCLK has a duty cycle of 50%.

Table 3. Values of F for Various Sample Rates

Sample Rate (KHz)	Clock Select	Clock Frequency (MHz)	Cutoff Frequency Fc (KHz)	50x F Divisor (N – 1)		100x F Divisor (N – 1)	
				decimal	hex	decimal	hex
48.0	CLK25	24.576	30.720	3	03	1	01
44.1	CLK17	16.9344	21.168	3	03	1	01
32.0	CLK25	24.576	15.360	7	07	3	03
22.05	CLK17	16.9344	10.584	7	07	3	03
11.025	CLK17	16.9344	5.292	15	0F	7	07
8.0	CLK25	24.576	3.84	31	1F	15	0F

Internal Address Register

The AUX bits of the first frame of a block specify an 8-bit address, used to optionally start loading register data at a position other than at the beginning. By setting the 8-bit address to a value other than zero, data for any register may be loaded without having to load all the previous registers. The address register automatically increments after each frame within a block, and stops incrementing at address 18 (decimal).

INTERNAL REGISTERS

Register	Reg Bits	Name	Interpretation	Power-up Default Condition
0	7:0	SCLK S divisor	sdiv[7:0]	0000 0000
1	7	reserved	reserved	0000 0010
	6	Unlock		
	5	Clock input select	0 = CLK25 1 = CLK17	
	4:0	SCLK S Divisor	sdiv[12:8]	
2	7:6	reserved	reserved	0000 0101 assumes a 50x filter, 20kHz cutoff
	5:0	FCLK F divisor	fdiv[5:0]	
3	7:6	Input/output mode	00 = stereo out 01 = stereo in 10 = mono in, mono out 11 = reserved	0000 0000
	5:4	ADC configuration	00 = internal ADC 01 = reserved 10 = reserved 11 = reserved	
	3:2	DAC configuration	00 = internal DAC 01 = reserved 10 = reserved 11 = reserved	
	1	SA_OUT 3-state control	0=enabled 1=3-state	
	0	SA_OUT mode	0=ADC input 1=SA_IN input	
4	7:0	APP0-7 I/O configuration	appio[7:0] 0= input 1= output	0000 0000
5	7:0	APP0-7 output value	appout[7:0]	0000 0000

Register	Reg Bits	Name	Interpretation	Power-up Default Condition
6	7:6	Loop test	00 = normal operation 01= analog test loop (left) enabled 10 = analog test loop (right) enabled 11 = digital test loop enabled	0000 0000
	5	Power down enable	0=normal operation 1=power down mode	
	4:0	Mixer output attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
7	7	Channel Select for Updating Register 7 bits 5:0	0=write left and right channel 1=write right channel only	0000 0000
	6	Initiate Offset Calibration	0=normal operation 1=initiate calibration	
	5	MIC mute	0=mute 1=do not mute	
	4	Mux output gain	0=+6dB 1=+12dB	
	3	Mixer output gain	0=+6dB 1=+12dB	
	2:0	MUX input select	000 = mute 001 = CD 010 = LINE 011 = FM 100 = MIC 101 = mixer output 110 = DAC output 111 = reserved	
8	7:5	reserved	reserved	0000 0000
	4:0	CD left input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
9	7:5	reserved	reserved	0000 0000
	4:0	CD Right input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	

Register	Reg Bits	Name	Interpretation	Power-up Default Condition
10	7:5	reserved	reserved	0000 0000
	4:0	LINE left input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
11	7:5	reserved	reserved	0000 0000
	4:0	LINE right input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
12	7:5	reserved	reserved	0000 0000
	4:0	FM left input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
13	7:5	reserved	reserved	0000 0000
	4:0	FM right input attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
14	7:5	reserved	reserved	0000 0000
	4:0	MIC left input gain	00000=illegal 00001=+51dB .... 11111=+6dB	
15	7:5	reserved	reserved	0000 0000
	4:0	MIC right input gain	00000=illegal 00001=+51dB .... 11111=+6dB	

Register	Reg Bits	Name	Interpretation	Power-up Default Condition
16	7:5	reserved	reserved	0000 0000
	4:0	DAC left attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	
17	7:5	reserved	reserved	0000 0000
	4:0	DAC right attenuation	00000=mute(off) 00001=-51dB .... 11111=-6dB	

Note When increasing or decreasing the gain or attenuation values, the software should ensure that 1.5 dB increments are used. Large increments or decrements in gain or attenuation may result in audible artifacts.

The relationship between the left/right (A/B) AUX bits and the register bits is:

Register Address	Right Channel (subframe B) AUX Bits				Left Channel (subframe A) AUX Bits			
	3	2	1	0	3	2	1	0
	Register Address							
–	A7	A6	A5	A4	A3	A2	A1	A0
–	Register Bits							
0	7	6	5	4	3	2	1	0
1	7	6	5	4	3	2	1	0
:	:				:			
17	7	6	5	4	3	2	1	0

Frame number 0 corresponds to start of block.

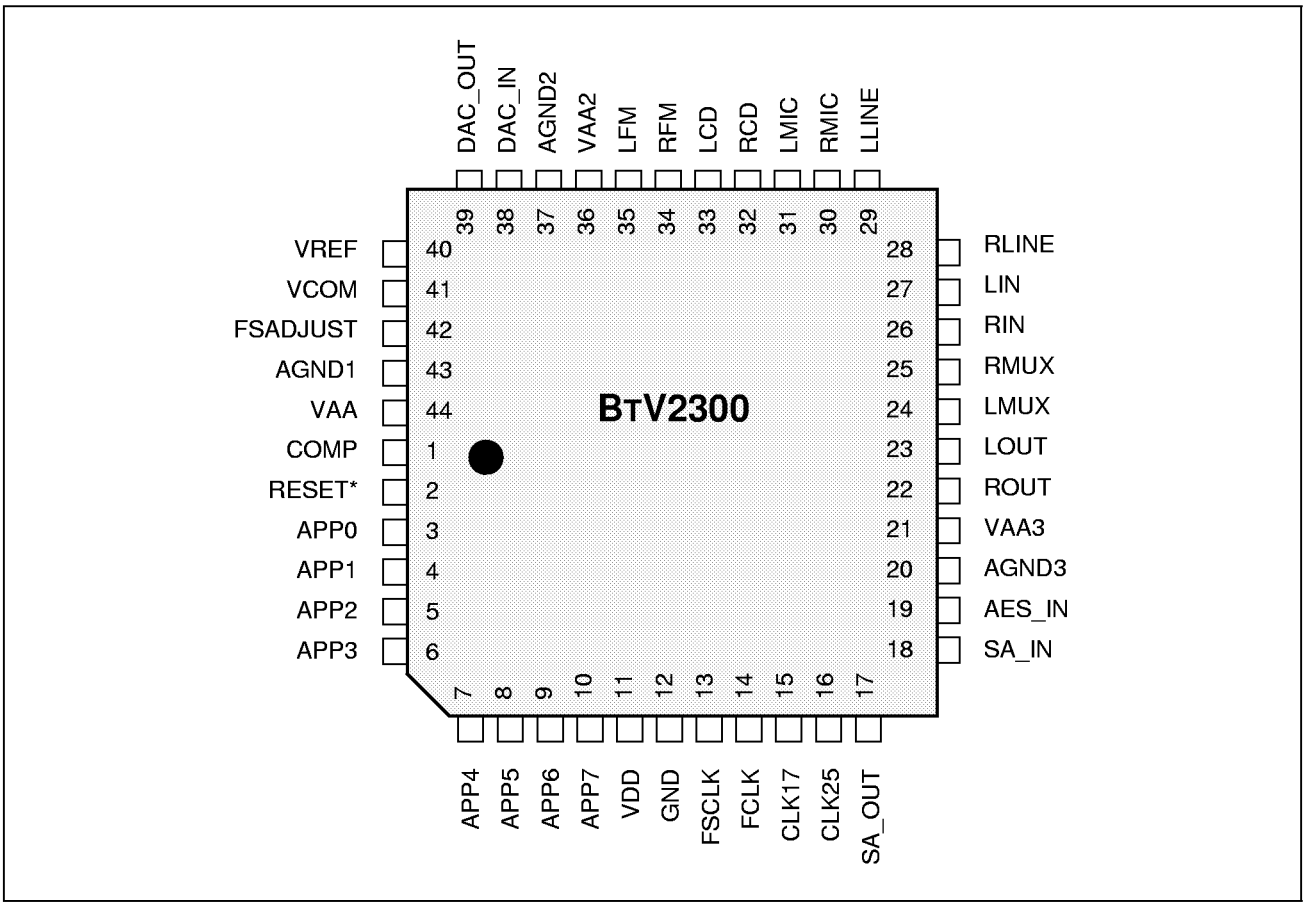
PIN INFORMATION

Pin Description

Pin Name	I/O	Pin #	Description
CLK17	I	15	16.9344 MHz clock input.
CLK25	I	16	24.576 MHz clock input.
FCLK	O	14	Filter clock output. This pin provides a clock (typically 50x F_c) to drive external switched-capacitor lowpass filters.
FSCLK	O	13	Sample-rate clock output. This pin provides a clock (1x F_S) to drive external devices.
RESET*	I	2	Reset control input. A logical zero for a minimum of eight CLK25 clock cycles initializes the device. RESET* must be a logical one for normal operation.
SA_IN	I	18	Serial audio input. Digital audio and control information is input via this pin. This input is not compatible with the standard AES/EBU and SPDIF interfaces since the BtV2300 has no PLL for clock recovery and the logic levels are different.
SA_OUT	O	17	Serial audio output. Digital audio and control information is output via this pin. This output is compatible with the standard AES/EBU and SPDIF interfaces, except for the logic levels.
VREF	I	40	Voltage reference. A 4.7 µF tantalum capacitor must be used to decouple this input to AGND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. This pin should not be used to provide a voltage to any external circuitry, except the bypass capacitor.
VCOM	O	41	1.5 V voltage reference decoupling pin. This pin should be decoupled to AGND as shown in Figure 5 in the chapter, “PC Board Considerations.” It should not drive any other external circuitry.
FSADJUST	–	42	Full-scale adjust control pin. A 19.1 KΩ 1% metal film resistor must be connected between this pin and AGND to control the full-scale output range on the DAC outputs.
COMP	–	1	Compensation pin. A 0.1 µF capacitor must be used to bypass this pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Name	I/O	Pin #	Description
(L, R) CD	I	33, 32	Left and right analog CD inputs. These inputs have a 1.5 V DC offset and should be AC-coupled to the signal source through a 0.1 µF capacitor.
(L, R) LINE	I	29, 28	Left and right analog line inputs. These inputs have a 1.5 V DC offset and should be AC-coupled to the signal source through a 0.1 µF capacitor.
(L, R) MIC	I	31, 30	Left and right analog microphone inputs. These inputs have a 1.5 V DC offset and should be AC-coupled to the signal source through a 1 µF capacitor.
(L, R) FM	I	35, 34	Left and right FM synthesizer analog inputs. These inputs have a 1.5 V DC offset and should be AC-coupled to the signal source through a 1 µF capacitor.
(L, R) MUX	O	24, 25	Left and right multiplexer analog outputs. Outputs to external antialiasing (switched capacitor) filters. These outputs have a 1.5 V DC offset.
(L, R) IN	I	27, 26	Left and right ADC analog inputs. The outputs of the external antialiasing (switched capacitor) filters drive these inputs. These inputs have a 1.5 V DC offset.
(L, R) OUT	O	23, 22	Left and right line-level analog outputs. These outputs may drive up to a 10 KΩ load. These outputs have a 1.5 V DC offset.
DAC_OUT	O	39	DAC analog output. This output is wired to the DAC_IN analog input.
DAC_IN	I	38	DAC analog input. This input is wired to the DAC_OUT analog output.
APP(0–7)	I/O	3–10	Application-specific inputs and outputs.
AES_IN	I	19	Digital audio serial interface input. This input may be selected to be output onto the SA_OUT pin. The use of this pin is discussed in the Application Section.
VAA	–	–	Analog power pins.
VDD	–	–	Digital power pins.
AGND	–	–	Analog ground pins.
GND	–	–	Digital ground pins.

Pin Assignments



PC BOARD CONSIDERATIONS

For optimum performance of the BtV2300, proper CMOS layout techniques should be studied in Application Note AN-16, before PC board layout is begun. This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the power and ground planes by providing good decoupling. The trace length between groups of VAA/VDD and AGND/GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended.

Component Placement

Components should be placed as close as possible to the associated pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the BtV2300 to be located as close as possible to its dedicated power supply regulator and the audio input/output connector.

Figure 3. VL Bus Board Layout

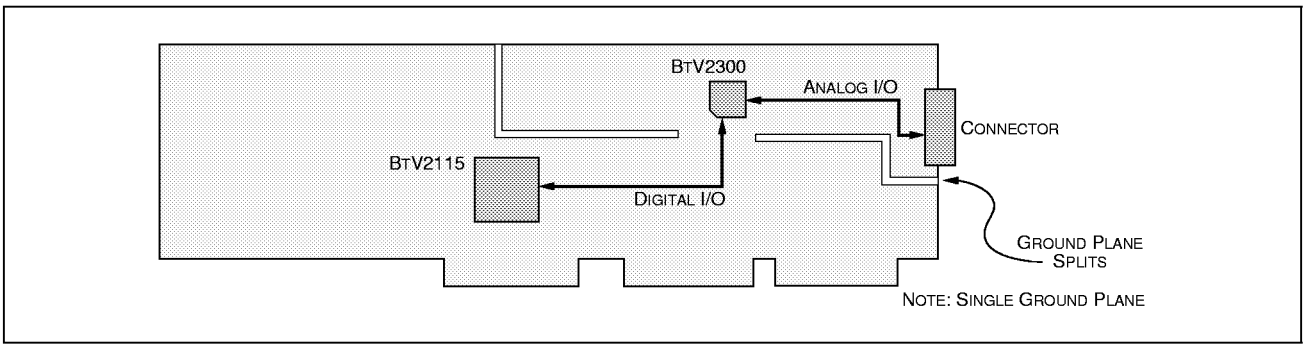


Figure 4. PCI Bus Board Layout

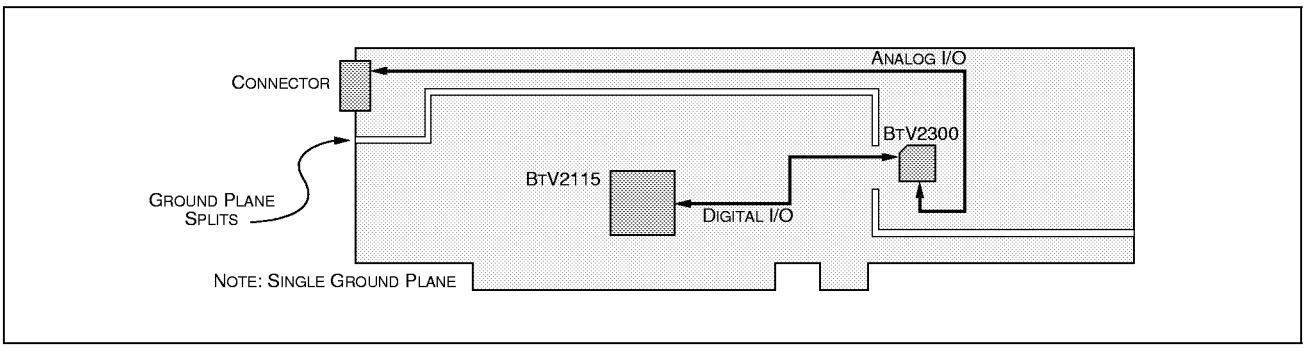


Figure 5. Typical Power Supply Connection Diagram

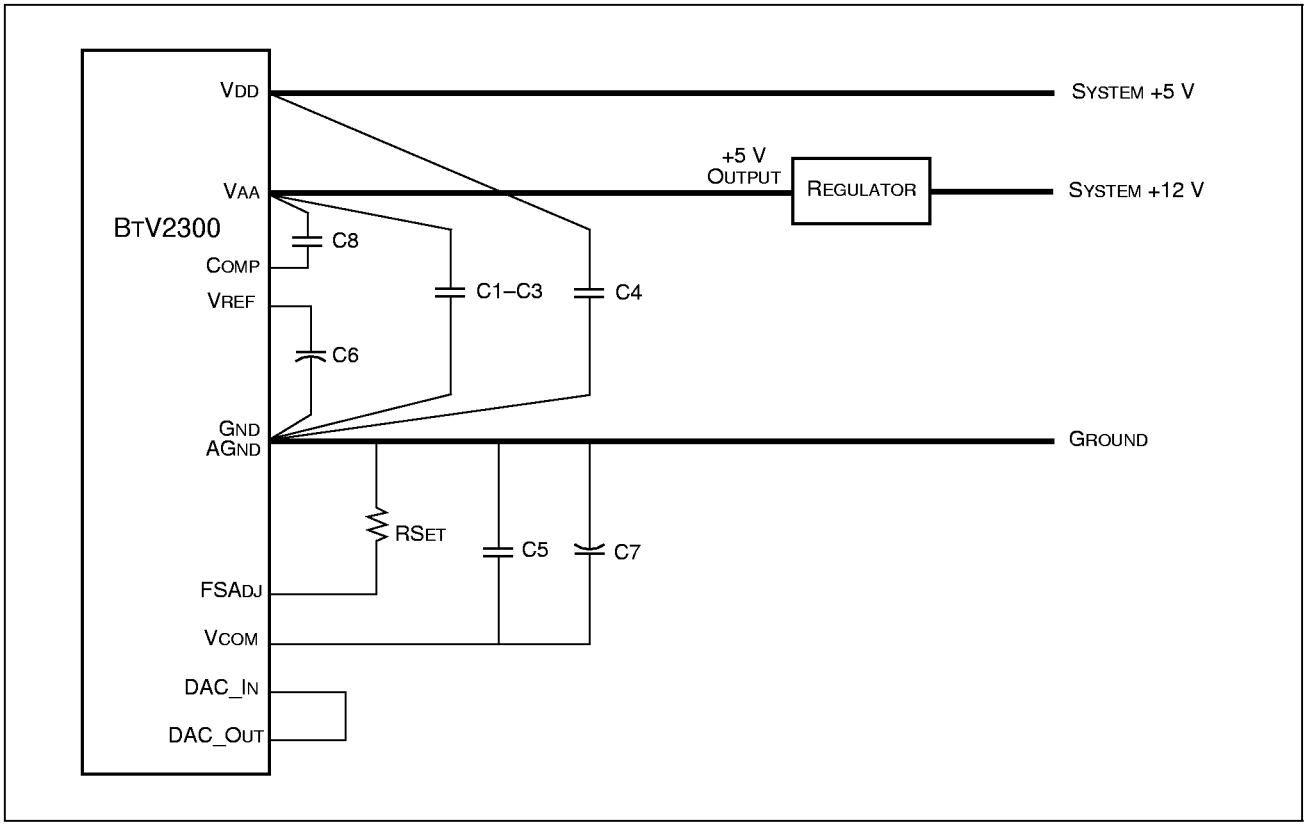


Table 4. Typical Power Supply Parts List

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	4.7 µF tantalum capacitor	
C7	1 µF tantalum capacitor	
C8	0.1 µF capacitor	
RSET	1% metal film resistor, 19.1 KΩ	Dale CMF-55C

Note The vendor numbers listed in Table 4 are only a guide. Substitution of devices with similar characteristics will not affect the performance of the BtV2300.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all BtV2300 power pins and related analog pins. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

A dedicated voltage regulator should provide power to the analog power plane, and this should provide power to all the BtV2300 VAA power pins and switched capacitor filters.

Another dedicated voltage regulator should provide –5 V power to the switched capacitor filters.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each group of VAA/VDD pins to AGND/GND. The capacitors should be placed as close as possible to the device VAA/VDD and AGND/GND pins and connected with short, wide traces.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. If low-frequency supply noise is present, a larger value will be required. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

VREF Decoupling

A 4.7 µF ceramic capacitor should be used to decouple this pin to AGND.

VCOM Decoupling

A 0.1 µF ceramic capacitor in parallel with a 1 µF tantalum capacitor should be used to decouple this pin to AGND.

Digital Signal Interconnect

The digital inputs and outputs of the BtV2300 should be isolated as much as possible from the analog inputs and outputs and other analog circuitry. Also, the digital signal traces should not overlay the analog output signal traces.

Most of the noise on the analog outputs will be caused by asynchronous clocks and power supply noise.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge input rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

Analog Signal Interconnect

The BtV2300 should be located as close as possible to the analog input/output circuitry and dedicated voltage regulator to minimize noise pickup.

The analog inputs and outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog input/output traces.

APPLICATION INFORMATION

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Power decoupling networks with large time constants should be avoided. They could delay VAA/VDD power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA and VDD pins (as well as all AGND and GND pins) are at the same potential and that the VAA/VDD supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage.

Analog Antialias Filtering

Typical antialias filtering for the BtV2300 is shown in Figure 6. Two Maxim MAX297 switched capacitor filters (recommended for best performance) are used to lowpass filter the inputs to the internal ADC and the internal DAC outputs. The MAX297 requires a 50xFc clock, which is generated by the BtV2300 (FCLK). The National Semiconductor LMF40 switched capacitor filters may also be used. For best operation, the filters should be configured to use a ±5 V power supply, and filters that use a 50xFc clock should be used.

The MAX297 is an eight pole elliptic filter, and provides good attenuation at 1.5xFc. The National Semiconductor MF4 type devices are four pole Butterworth filters and do not provide good attenuation until well above Fc. Therefore, MF4 filters may be used to cut system costs only if playback at sample rates less than 20 KHz are not required.

Figure 6. Lowpass Filter Implementation Using MAX297

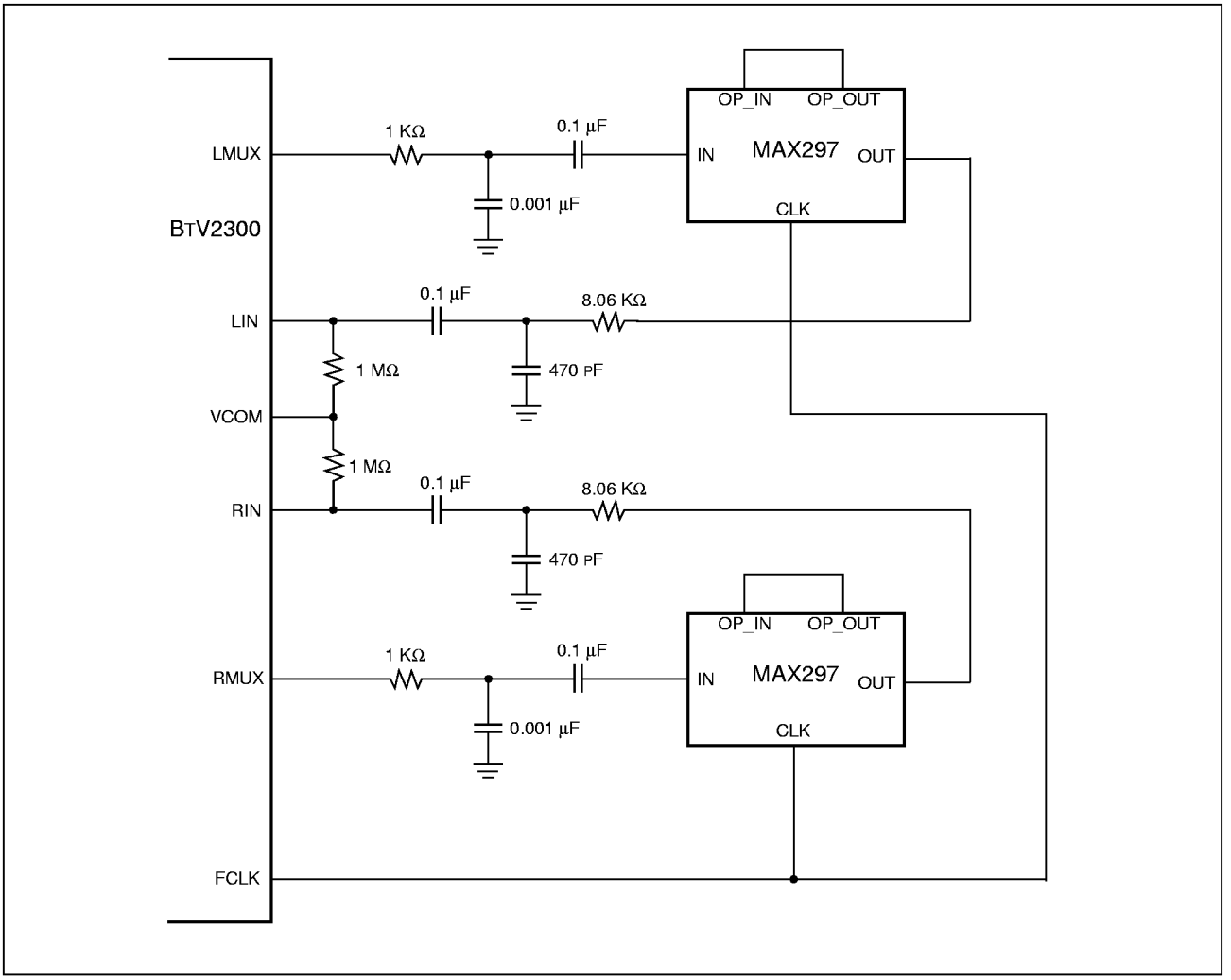
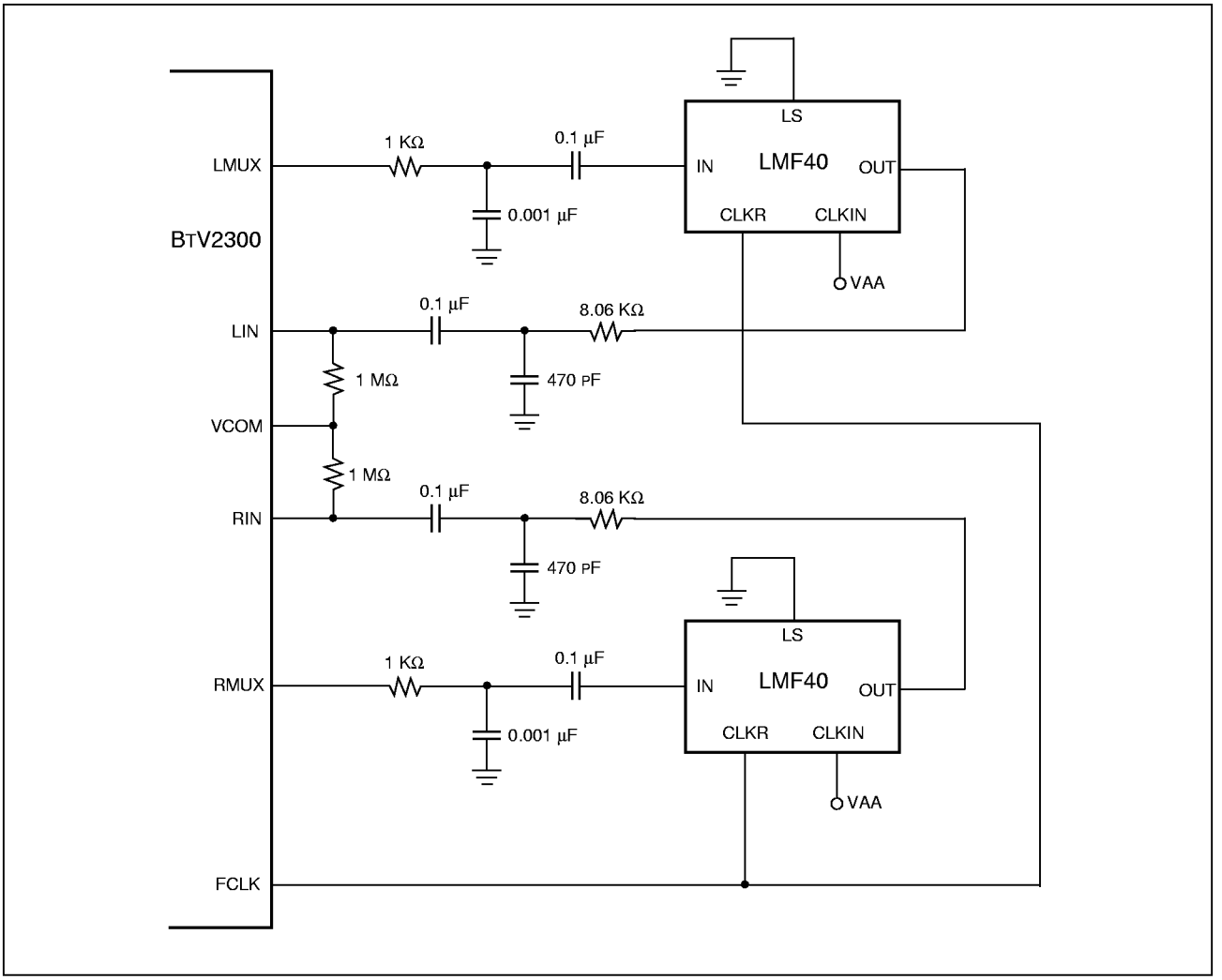


Figure 7. Lowpass Filter Implementation Using LMF40



If the stereo output mode is selected, the filters are used to lowpass filter the left and right channel internal DAC outputs prior to mixing with the CD, LINE, FM, and MIC analog inputs. The left and right internal DAC outputs are output via the (L, R) MUX pins in this case and fed back into the mixer via the (L, R) IN pins.

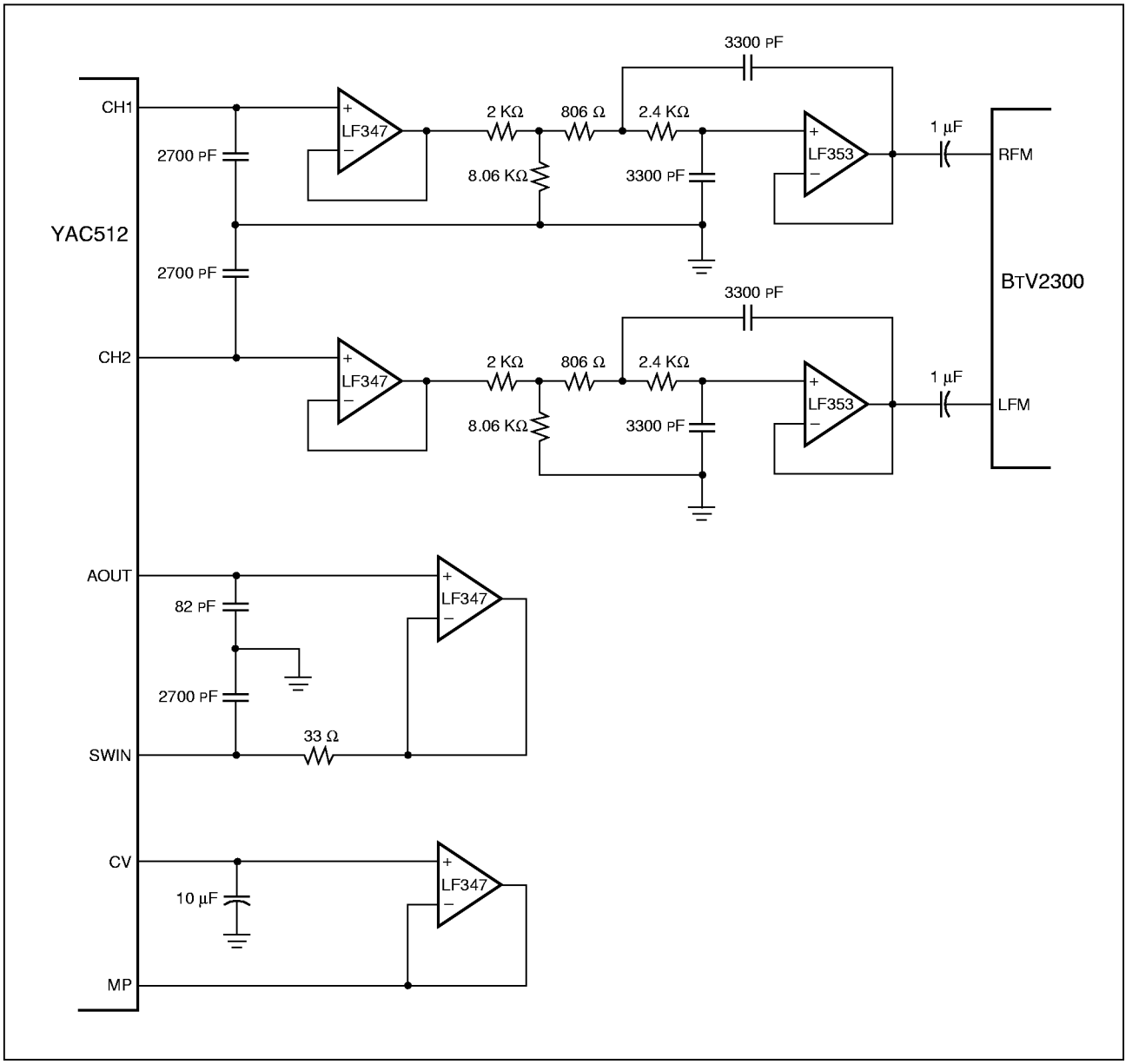
If the stereo input mode is selected, the filters are used to lowpass filter the (L, R) MUX outputs before digitizing.

If the mono in/out mode is selected, the left channel filter is used to lowpass filter the left channel internal DAC output before mixing (both the left and right inputs to the mixer are driven). The left DAC output is output via the L MUX pin. The right channel filter is used to lowpass filter the R MUX output prior to digitizing, and contains either the left channel CD, LINE, FM, or MIC signal. The right channel internal ADC then drives both the left and right channels of the SDOUT interface.

FM Synthesizer

Using the (L, R) FM line-level inputs, an external FM Synthesizer and stereo DAC (Yamaha YMF262 and YAC512, respectively) may be interfaced to the BtV2300, as shown in Figure 8.

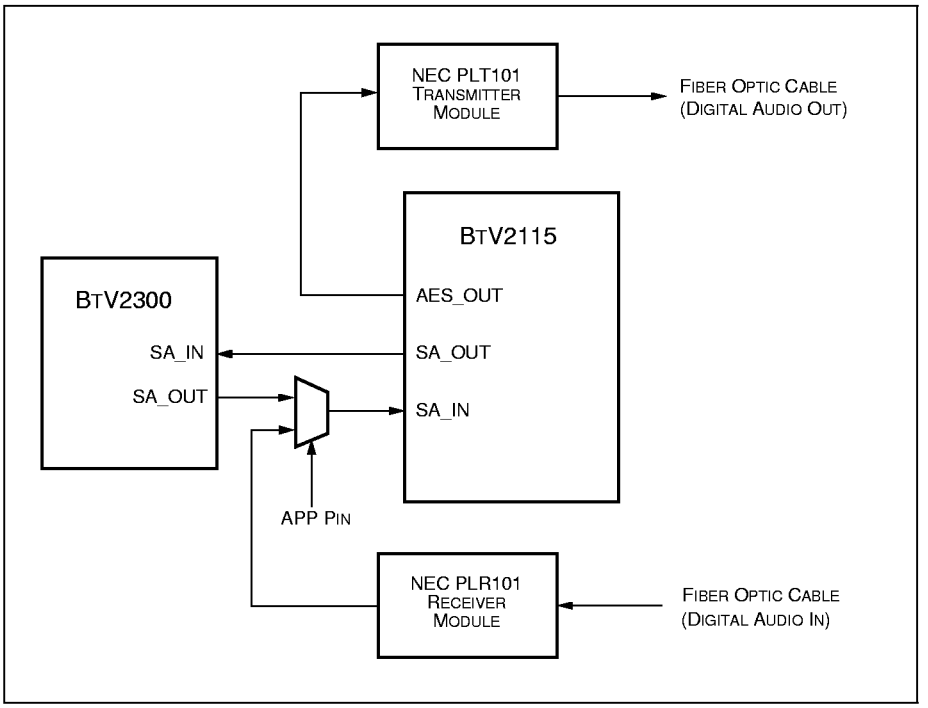
Figure 8. FM Synthesizer YAC512 Interfacing



AES_IN Fiber Optic Interface

The BtV2300 supports interfacing to serial digital audio interfaces from Compact Disc (CD), MiniDisc (MD), Digital Compact Cassette (DCC), Digital Audio Tape (DAT), etc. Figure 9 illustrates interfacing using a fiber optic interface (Toslink) common on consumer digital audio products.

Figure 9. AES_IN Fiber Optic Interfacing



A receiver module includes the fiber optic cable connector and optical-to-TTL circuitry. In this instance, a device such as the NEC PLR101 may be used. The TTL output of the receiver module drives the AES_IN pin. The data is passed onto the SA_OUT pin for processing and storage by the BtV2115. The NEC PLR101 requires only a single +5 V power supply.

A transmitter module converts the TTL SA_IN signal (generated by the BtV2115) to optical and also provides the fiber optic cable connector. In this instance, a device such as the NEC PLT101 may be used. The NEC PLT101 requires only a single +5 V power supply.

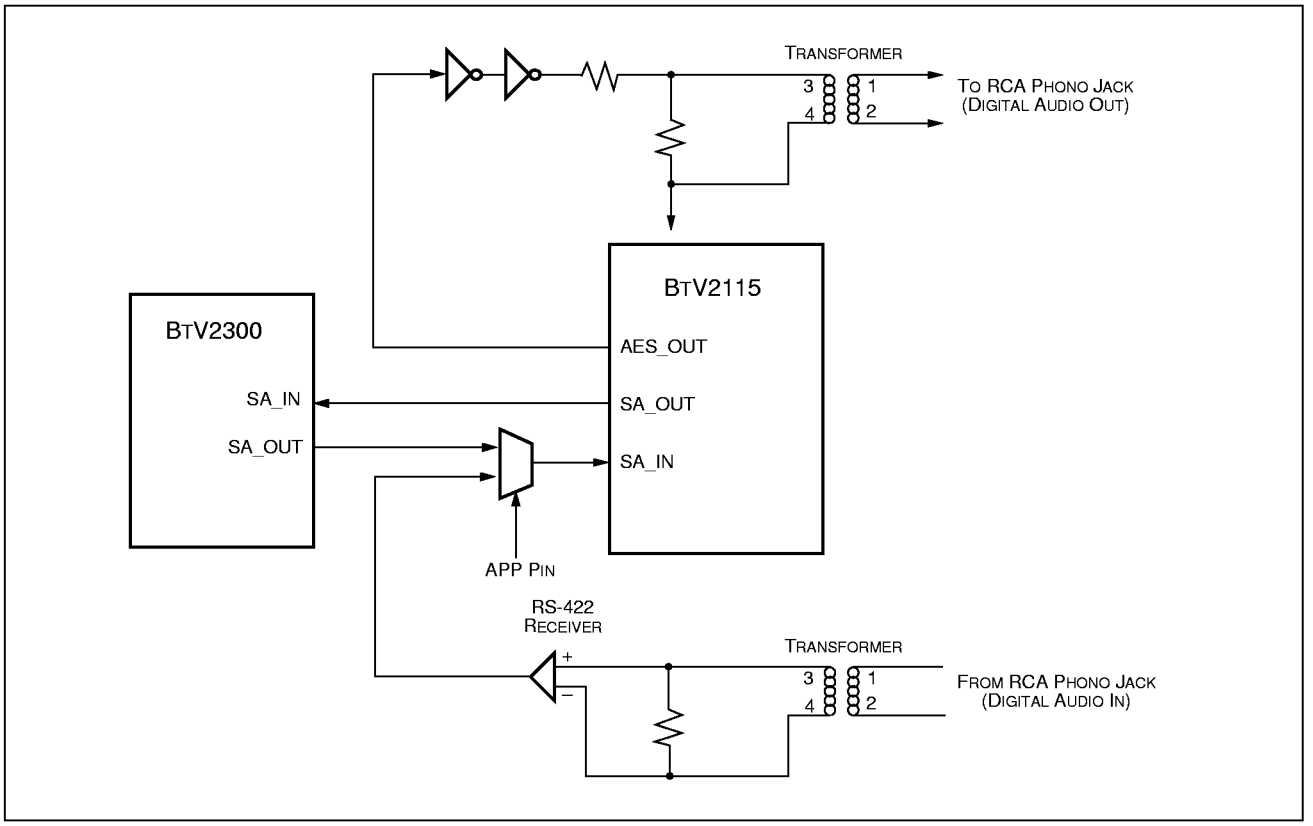
Another source for the Toslink receiver and transmitter modules is:

Sharp (GP1F31R and GP1F31T)

AES_IN Coaxial Interface

The BtV2300 supports interfacing to serial digital audio interfaces from Compact Disc (CD), MiniDisc (MD), Digital Compact Cassette (DCC), Digital Audio Tape (DAT), etc. Figure 10 illustrates interfacing using a coaxial interface common on consumer digital audio products. The connector for consumer applications is a standard RCA phono jack.

Figure 10. AES_IN Coaxial Interfacing



For coaxial digital audio output, the output impedance should be 75 Ω and the output drive should be 0.5 V ±20% (peak-to-peak) when measured across a 75 Ω load with no cable. The circuits in Figure 10 should use 1% resistors. The inverters are used to buffer the SA_IN pin from excessive loading.

For coaxial digital audio input, the input impedance should be 75 Ω. The circuits in Figure 10 should use 1% resistors. The RS–422 line receiver converts from RS–422 levels to TTL levels. Example RS–422 line receivers are:

- National Semiconductor DS9637A / µA9637A
- National Semiconductor DS9639A / µA9639A
- Texas Instruments SN75146
- Texas Instruments SN75157

The transformers should be capable of 1.5–7 MHz operation and provide isolation. Recommended transformers are available from:

Pulse Engineering
San Diego, CA
(619) 674-8100 (voice)
(619) 674-8262 (fax)
part number:
PE65612

Schott Corporation
Wayzata, MN
(612) 475-1173 (voice)
(612) 475-1786 (fax)
part numbers:
67128990 (pulse compatible)
67129000 (surface mount)
67129600 (single shield)

Scientific Conversions, Inc.
Novato, CA
(415) 892-2323 (voice)
(415) 892-2321 (fax)
part numbers:
SC916–01
SC937–01 (low profile)
SC937–02 (surface mount)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA, VDD	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		70	˚C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA, VDD (measured to GND)				7.0	V
Voltage on Any Signal Pin		GND–0.5		VDD+0.5	V
Ambient Operating Temperature	TA	–55		+125	˚C
Storage Temperature	TS	–65		+150	˚C
Junction Temperature	TJ			+150	˚C
Vapor Phase Soldering (1 minute)	TVSOL			220	˚C

This device employs high-impedance CMOS devices on all signal pins. Handle it as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can cause destructive latchup. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Analog Characteristics

TA = 25°C; VAA = 5.0 V, VDD = 5.0 V; Sinewave input (0 dB, 2 V P-P, 1 KHz); Sample Rate = 48 KHz; Measurement Bandwidth (except where noted) = 10 Hz–20 Hz; Minimum gain/attenuation settings.

	Parameter	Symbol	Min	Typ	Max	Units
(L,R)LINE, (L,R)CD, (L,R)IN , (L,R)FM Inputs	Input Impedance (L,R)LINE, (L,R)CD, (L,R)IN			>1.0		MΩ
	Input Impedance (L,R)FM		9.5			KΩ
	Nominal Full-scale Input Voltage			2.0		V P-P
	Absolute Gain Error to (L,R)MUX		–0.45		0.20	dB
	THD + N to (L,R)MUX			0.008		%
	Absolute Gain Error to (L,R)OUT		–0.99		–0.22	dB
	THD + N to (L,R)OUT			0.033		%
	Attenuation Range		43.5		46.1	dB
	Nominal Attenuator Step Size			1.5		dB
	Mute Attenuation		64.5			dB
(L,R)Mic Inputs	Input Impedance (L,R)MIC		15.3			KΩ
	Nominal Full-scale Input Voltage			0.5		V P-P
	Absolute Gain Error to (L,R)MUX		–1.05		–0.46	dB
	THD + N to (L,R)MUX			0.025		%
	Absolute Gain Error to (L,R)OUT		–1.73		–1.06	dB
	THD + N to (L,R)OUT			0.046		%
	Gain Range		28.36		30.07	dB
	Nominal Gain Step Size			1.5		dB
(L,R)MUX Outputs	Nominal Full-scale Output Voltage			2.0		V P-P
	DC Offset Voltage			1.45		V
	Optional Gain Step Size			6.0		dB

	Parameter	Symbol	Min	Typ	Max	Units
(L,R)OUT Outputs	Nominal Full-scale Output Voltage			2.0		V P-P
	DC Offset Voltage			1.45		V
	Optional Gain Step Size			6.0		dB
	Attenuation Range		43.5		46.1	dB
	Nominal Attenuator Step Size			1.5		dB
	Mute Attenuation		64.5			dB
D/A Conversion	Nominal Full-scale Output Voltage			1.0		V P-P
	Absolute Gain Error		–1.52		1.53	dB
	THD + N			0.049		%
	Dynamic Range			68.6		dB
A/D Conversion	Absolute Gain Error		–1.86		1.38	dB
	THD + N			0.174		%
	Dynamic Range			55.2		dB
Supplies	VAA Supply Current VAA Power Down Current	IAA		 1.1	74.1	mA mA
	VDD Supply Current VDD Power Down Current	IDD		 0.9	18.2	mA mA

Rms noise plus harmonic distortion in the 20 Hz–20 KHz frequency range expressed as a percent of the nominal full scale level. For line inputs, the signal is 1 KHz at 2 Vpp. For the microphone inputs, the signal is 1 KHz at 500 mVpp. For A/D and D/A conversion, the input signal is 1 KHz at 1 Vpp.

S/N: Ratio of rms noise in the 20 Hz–20 KHz frequency range to the nominal full scale level expressed in dB. Signal levels are same as used in the THD+N measurement.

Dynamic Range: Ratio of rms noise plus harmonic distortion in the 20 Hz–20 KHz frequency range to the nominal full scale level with a 1 KHz, –40dB signal.

Attenuation Range: Difference in attenuation between 6.0 dB and 51.0 dB attenuation steps expressed in dB. Nominally 45.0 dB.

Gain Range: Gain provided by mic amplifier at 24.0 dB setting plus mux gain at 6.0 dB setting. Nominally 30.0 dB.

Absolute Gain Error: Deviation from nominal gain expressed in dB. Gain error is measured with attenuators set to 6.0 dB and mixer, mux gain at 6.0 dB.

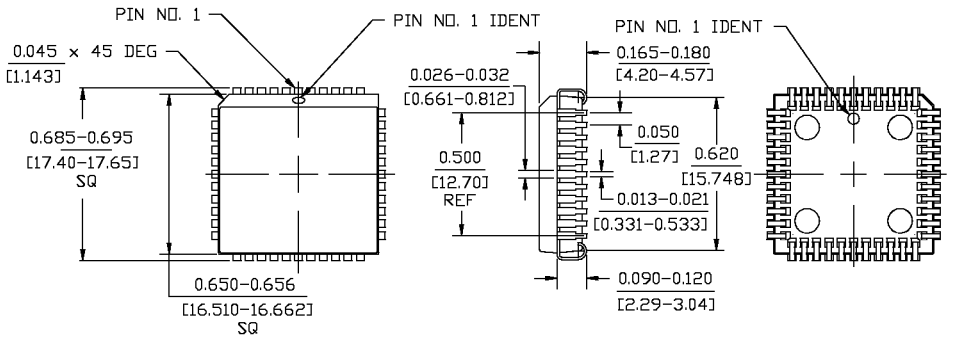
Digital Characteristics

	Parameter	Symbol	Min	Typ	Max	Units
CLK17, CLK25, SA_IN, AES_IN	Input High Voltage	VIH	2.2			V
	Input Low Voltage	VIL			0.8	V
RESET	Input High Voltage	VIH	2.4			V
	Input Low Voltage	VIL			0.8	V
APP[0:7]	Input High Voltage	VIH	2.2			V
	Input Low Voltage	VIL			0.8	V
	Output High Voltage (I_{OH} = 100 µA)	VOH	4.0			V
	Output Low Voltage (I_{OL} = –100 µA)	VOL			0.4	V

Note: Test conditions (unless otherwise specified): "Recommended Operating Conditions". As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Package Mechanical Drawing

Figure 11. 44-Pin PLCC Package Mechanical Drawing



Revision History

Table 5. BtV2300 Datasheet Revision History

Revision	Date	Change	Description
A	9/20/94	Initial Release	
B	12/16/94		
C	2/3/95		
D	8/11/95		