ESS Technology, Inc.

Maestro-2™ PCI Audio Accelerator Data Sheet

DESCRIPTION

The Maestro-2™ digital audio accelerator is a highly integrated PCI audio solution that brings advanced audio features to notebook and desktop systems. These features include a 64-voice wavetable synthesizer with Downloadable Sample (DLS) and complete DirectSound™ acceleration. The Maestro-2 proprietary technology supports both Microsoft®'s PC97 and PC98 logo requirements and DOS game compatibility.

The Maestro-2 device works with any AC'97 compliant CODEC including ESS Technology's own ES1918 AC'97 CODEC.

The dual-audio engine Maestro-2 architecture consists of a 64-voice pipelined wavetable synthesizer and a proprietary audio signal processor. Together they can simultaneously handle multiple audio streams of different data types, high-quality MIDI synthesis, and voice compression and decompression. Each channel/stream has an independent pan, tremolo, vibrato, and tone filter. The synthesizer also performs advanced audio effects such as reverb, chorus, treble, bass, flange, echo, and 3-D spatial enhancement.

WaveCache™ technology reduces the system cost by storing data (synthesis samples, WAV files, algorithms) in host memory. The data is retrieved using high-speed PCI bus cycles during playback or recording.

Microsoft's DirectSound API is accelerated by digitally mixing as many as 32 PCM streams of any frequency down to a single output stream of 48 kHz. This "final" buffer can then be piped to any CODEC available to the system. This acceleration frees up the CPU to perform other tasks.

The Maestro-2 audio accelerator supports a number of different legacy audio schemes, including Distributed DMA protocol, PC/PCI DMA, and Transparent DMA. This ensures complete DOS game compatibility over the PCI bus.

The Maestro-2 power management complies with Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.0, and PCI Power Management Interface (PPMI) 1.0.

The Maestro-2 audio accelerator is available in an industry-standard 100-pin Thin Quad Flat Package (TQFP).

FEATURES

- 500-MIPS-equivalent processor performance to accelerate multi-stream PC audio
- 64-Voice wavetable synthesizer
- Proprietary WaveCache technology
- HRTF 3-D positional audio under DirectX™ 5.0
- Enhanced effects (reverb, chorus, echo, vibrato, etc.)
- Distributed and PC/PCI DMA, Compaq®/Intel® serial IRQ support and Transparent DMA
- AC-3 speaker virtualization
- 2-Button hardware master volume control
- I^2S/Zoomed Video support
- AC'97 CODEC interface
- Up to 20-bit ADC/DAC audio resolution
- Complies with Microsoft's ACPI 1.0 and PPMI 1.0 (D0~D3)
- 3.3 V power supply, 5 V – input tolerant
- Supports up to 12 GPIO pins
- Secondary CODEC interface
- 100-Pin TQFP package

BENEFITS

- High-Performance audio
- High-Speed PCI bus cycles when accessing data stored in system memory
- Highest performance engine for DirectSound acceleration
- Enhanced sound images, product differentiation
- Ensures complete DOS game compatibility regardless of core logic legacy support
- Scalable for high-end, high-fidelity audio
- Adjusts volume independent of applications
- Zoomed Video MPEG audio playback application
- Flexibility in layout
- Supports OnNow, Microsoft's design initiative for power management
- Optimal power saving and simplified layout
- Flexibility for system management schemes
- Small real estate for economical notebook design

CONTENTS

FIGURES

TABLES

MAESTRO-2 BLOCK DIAGRAMS

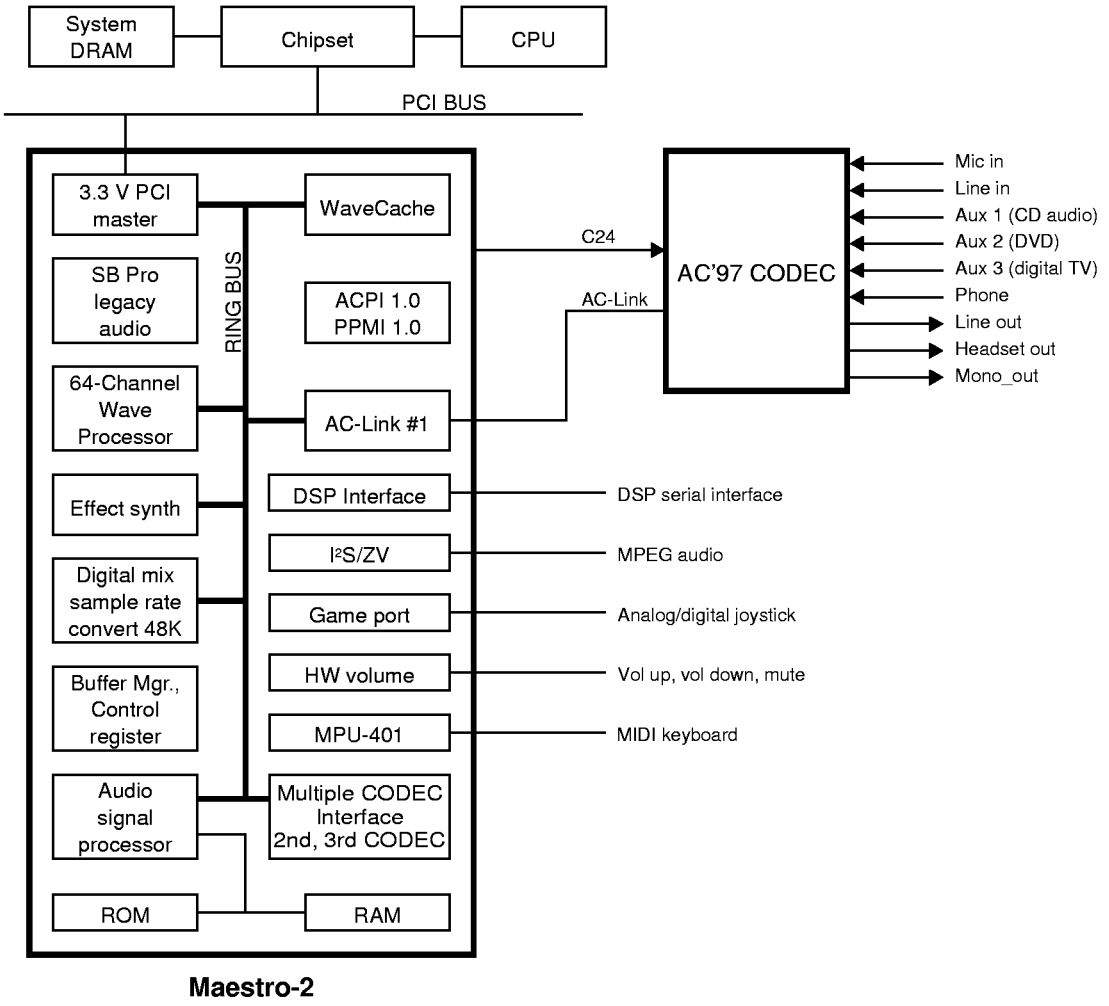


Figure 1 Maestro-2 Block Diagram

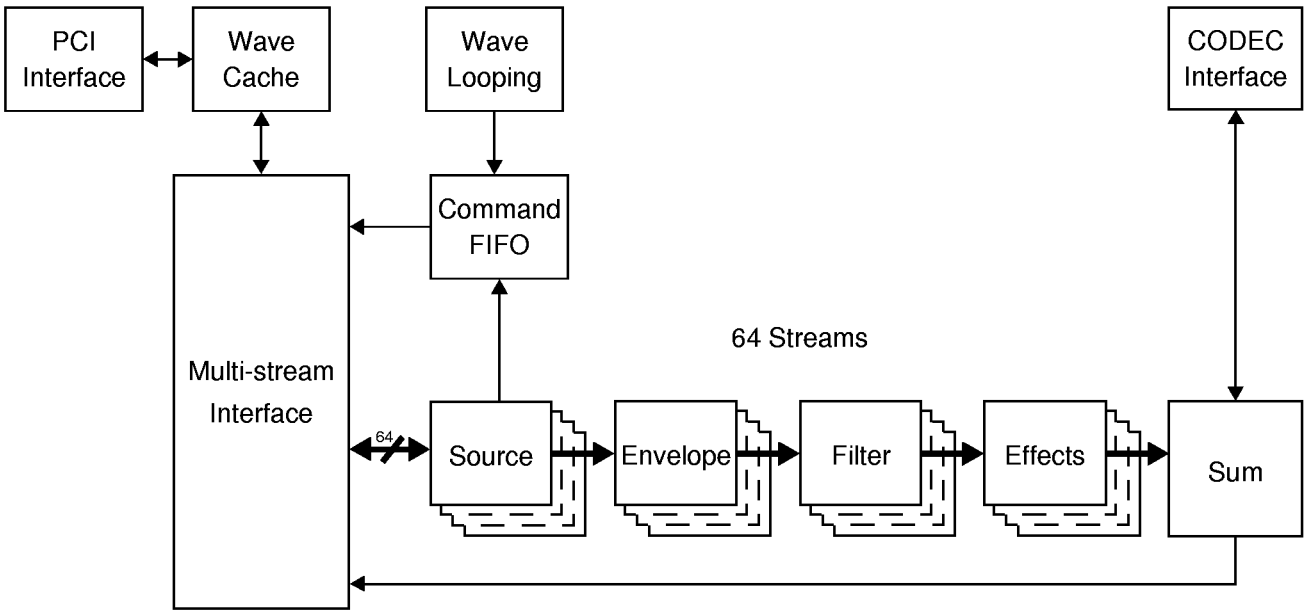


Figure 2 Wave Processor Portion

PINOUT

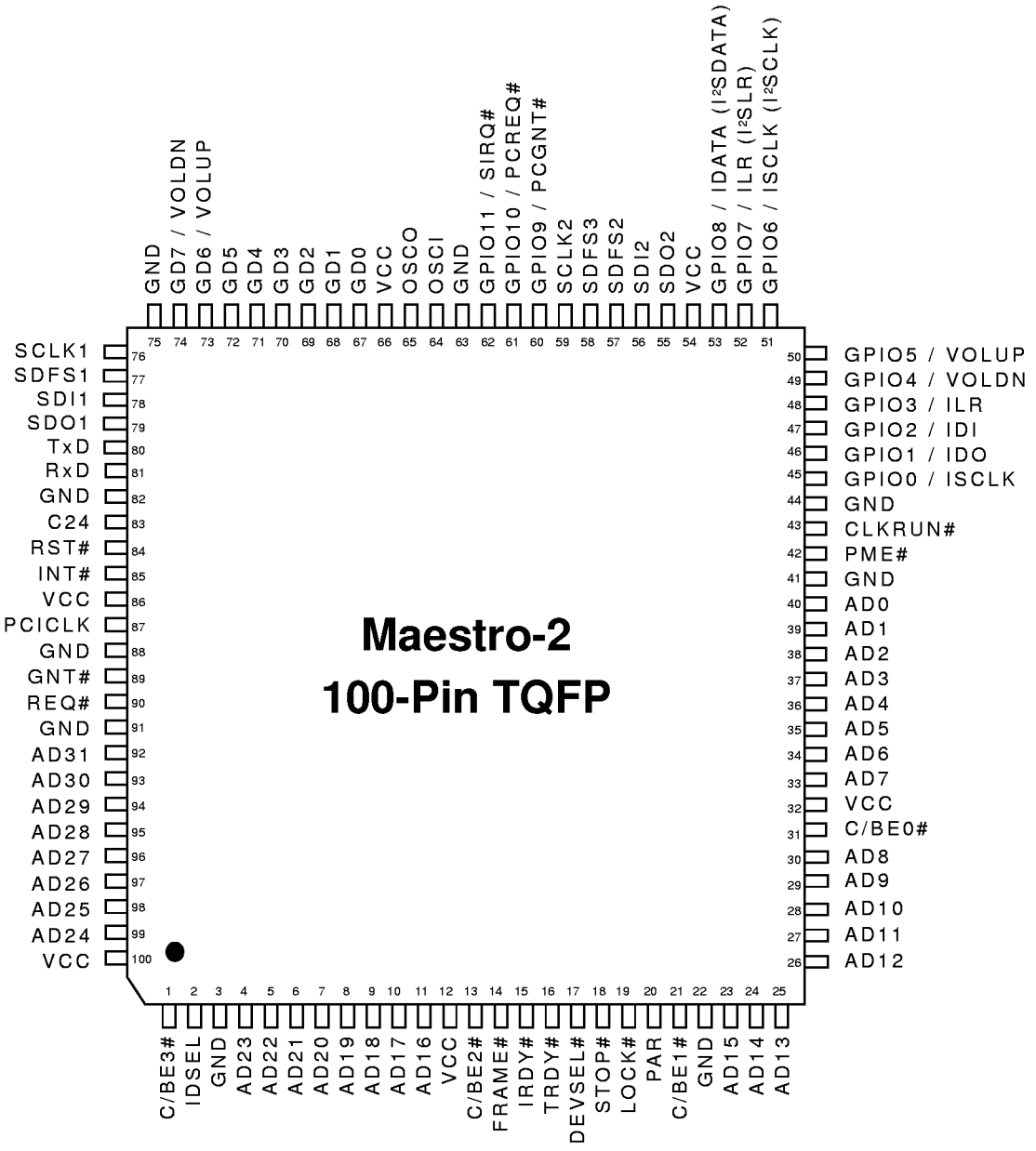


Figure 3 Maestro-2 Pinout

PIN DESCRIPTION

Name	Number	I/O	Definition
C/BE[3:0]#	1,13,21,31	I/O	Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction. They indicate active-low byte enable information for the current data phase during the data phases of a transaction. These pins are inputs during slave operation and outputs during bus mastering operation.
IDSEL	2	I	ID select, active-high. This pin is used as a chip select during PCI configuration read and write cycles.
AD[31:0]	92:99,4:11, 23:30,33:40	I/O	Multiplexed address and data lines.
FRAME#	14	I/O	Cycle frame, active-low. The current PCI bus master drives this pin to indicate the beginning and duration of a transaction.
IRDY#	15	I/O	Initiator ready, active-low. The current PCI bus master drives this pin to indicate that as the initiator it is ready to transmit or receive data (and complete the current data phase).
TRDY#	16	I/O	Target ready, active-low. The current PCI bus master drives this pin to indicate that as the target device it is ready to transmit or receive data (and complete the current data phase).
DEVSEL#	17	I/O	Device select, active-low. The PCI bus target device drives this pin to indicate that it has decoded the address of the current transaction as its own chip select range.
STOP#	18	I/O	Stop transaction, active-low. The current PCI bus target drives this pin active to indicate a request to the master to stop the current transaction.
LOCK#	19	I/O	Lock.
PAR	20	I/O	Parity, active-high. This pin indicates even parity across AD[31:0] and C/BE[3:0]# for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.
PME#	42	O	Power management enable interrupt output to wake up the system.
CLKRUN#	43	I/O	Input for clock status and output to start/speed-up clock.
GPIO0	45	I/O	Dual-purpose pin. GPIO0 is general purpose input/output 0. Selected by Maestro2_Base+68h[11:0].
ISCLK		I	ISCLK is the serial shift clock for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2_Base+36h[15] = 1.
GPIO1	46	I/O	Dual-purpose pin. GPIO1 is general purpose input/output 1. Selected by Maestro2_Base+68h[11:0].
IDO		O	IDO is the serial data output for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2_Base+36h[15] = 1.
GPIO2	47	I/O	Dual-purpose pin. GPIO2 is general purpose input/output 2. Selected by Maestro2_Base+68h[11:0].
IDI		I	IDI is the serial data input for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2_Base+36h[15] = 1.
GPIO3	48	I/O	Dual-purpose pin. GPIO3 is general purpose input/output 3. Selected by Maestro2_Base+68h[11:0].
ILR		I	ILR is the frame sync signal for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2_Base+36h[15] = 1.
GPIO4	49	I/O	Dual-purpose pin. GPIO4 is general purpose input/output 4. Selected by Maestro2_Base+68h[11:0].
VOLDN		I	VOLDN is a volume decrease input. Selected by setting PCI 52h[7:5] to 1x0. Alternatively, the VOLUP/VOLDN pair at pins 73 and 74 may be used.

Name	Number	I/O	Definition
GPIO5	50	I/O	Dual-purpose pin. GPIO5 is general purpose input/output 5. Selected by Maestro2_Base+68h[11:0].
VOLUP		I	VOLUP is a volume increase input. Selected by setting PCI 52h[7:5] to 1x0. Alternatively, the VOLUP/VOLDN pair at pins 73 and 74 may be used.
GPIO6	51	I/O	Dual-purpose pin. GPIO6 is general purpose input/output 6. Selected by Maestro2_Base+68h[11:0].
ISCLK (I^2SCLK)		I	ISCLK (I^2SCLK) is the I^2S serial clock. Selected by setting Maestro2_Base+36h[15] = 1.
GPIO7	52	I/O	Dual-purpose pin. GPIO7 is general purpose input/output 7. Selected by Maestro2_Base+68h[11:0].
ILR (I^2SLR)		I	ILR (I^2SLR) is the I^2S frame sync. Selected by setting Maestro2_Base+36h[15] = 1.
GPIO8	53	I/O	Dual-purpose pin. GPIO8 is general purpose input/output 8. Selected by Maestro2_Base+68h[11:0].
IDATA (I^2SDATA)		I	IDATA (I^2SDATA) is the I^2S data input pin. Selected by setting Maestro2_Base+36h[15] = 1.
SDO2	55	I/O	Serial data out. Strap pin (with internal pull-up): 1 = AC-link #2; 0 = Multi-CODEC interface.
SDI2	56	I	Serial data in.
SDFS2	57	O	Serial data frame sync.
SDFS3	58	O	Serial data frame sync.
SCLK2	59	I/O	Serial data clock. Output pin when the multi-CODEC interface is used. Input pin when the AC-link #2 interface is used.
GPIO9	60	I/O	Dual-purpose pin. GPIO9 is general purpose input/output 9. Selected by Maestro2_Base+68h[11:0].
PCGNT#		I	PCGNT# is the PC/PCI grant input. Selected by setting PCI 50h[10:8] = 010.
GPIO10	61	I/O	Dual-purpose pin. GPIO10 is general purpose input/output 10. Selected by Maestro2_Base+68h[11:0].
PCREQ#		O	PCREQ# is the PC/PCI request output. Selected by setting PCI 50h[10:8] = 010.
GPIO11	62	I/O	Dual-purpose pin. GPIO11 is general purpose input/output 11. Selected by Maestro2_Base+68h[11:0].
SIRQ#		I/O	SIRQ# is the serial interrupt request. Selected by setting PCI 40h[14] = 1.
OSCI	64	I	49.152 or 50.000 MHz crystal input. Refer to the Maestro-2 reference design for an update.
OSCO	65	O	49.152 or 50.000 MHz crystal output. Refer to the Maestro-2 reference design for an update.
GD[3:0]	70:67	I/O	Game port data.
GD[5:4]	72:71	I	Game port data.
GD6	73	I	Dual-purpose pin. GD6 is a game port data input pin.
VOLUP		I	VOLUP is a volume increase input. Selected by setting PCI 52h[7:5] = 1x1. Alternatively, the VOLDN/VOLUP pair at pins 49 and 50 may be used.
GD7	74	I	Dual-purpose pin. GD7 is a game port data input pin.
VOLDN		I	VOLDN is a volume decrease input. Selected by setting PCI 52h[7:5] = 1x1. Alternatively, the VOLDN/VOLUP pair at pins 49 and 50 may be used.
SCLK1	76	I	Serial clock. In AC'97 configuration, this pin is an input which drives the timing for the AC'97 interface.
SDFS1	77	O	Serial data frame sync. In AC'97 configurations, this pin is an output which indicates the framing for the AC'97 link.
SDI1	78	I	Serial audio data input.

Name	Number	I/O	Definition
SDO1	79	O	Serial audio data out.
TxD	80	O	MIDI transmit data.
RxD	81	I	MIDI receive data.
C24	83	O	24.576 or 25.000 MHz clock output depending on the XTAL input. For CODEC clock source.
RST#	84	I	Reset.
INT#	85	O	Interrupt request, active-low. This pin is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.
PCICLK	87	I	PCI bus clock. This clock times all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.
GNT#	89	I	Bus master grant, active-low. The system arbiter drives this pin to indicate to the device that access to the PCI bus has been granted.
REQ#	90	O	Bus master request, active-low tri-state output. This pin indicates to the system arbiter that this device is requesting access to the PCI bus. This pin must be tri-stated when RST# is active.
VCC	12,32,54,66, 86,100	Pwr	+3.3 volts.
GND	3,22,41,44,6 3,75,88,91	Pwr	Ground.

STRAP SELECTED OPTION

Pin Name	Pin Number	Default State at Reset	Condition	Description
SDO2	55	Pull-up	Low	Multiple CODEC interface is enabled for pins 59:55 (SCLK2, SDFS3, SDFS2, SDI2, SDO2).
			High	AC-Link #2 interface is enabled for pins 59:55 (SCLK2, SDFS3, SDFS2, SDI2, SDO2).

MULTI-FUNCTION PIN ASSIGNMENT

Function	Pin Names	Pin Numbers	Selection Settings
DSP Serial Interface	ISCLK,IDO,IDI,ILR	48:45	PCI 52h[4] = 1 and Maestro2_Base+36h[15]=1
General-Purpose Interface	GPIO[11:0]	62:60,53:45	Maestro2_Base+68h[11:0]
Hardware Volume Control	VOLUP,VOLDN	50,49	PCI 52h[7:5] = 1x0
	VOLUP,VOLDN	73,74	PCI 52h[7:5] = 1x1
I^2S Interface	ISCLK,ILR,IDATA	53:51	Maestro2_Base+36h[15] = 1
Legacy Audio Interface	PCGNT#,PCREQ#	61:60	PCI 50h [10:8] = 010
	SIRQ#	62	PCI 40h[14] = 1

FUNCTIONAL PIN GROUPING

Function	Pins	Pin Number
PCI Bus Pins	IDSEL	2
	AD[31:0]	92:99,4:11, 23:30,33:40
	C/BE[3:0]#	1,13,21,31
	FRAME#	14
	IRDY#	15
	TRDY#	16
	DEVSEL#	17
	STOP#	18
	LOCK#	19
	PAR	20
	CLKRUN#	43
	RST#	84
	INT#	85
	PCICLK	87
	GNT#	89
	REQ#	90
ACPI Pin	PME#	42
Legacy Audio Interface	PCGNT# *	60
	PCREQ# *	61
	SIRQ# *	62
MPU-401 Interface	TxD	80
	RxD	81
General-Purpose I/O Pins	GPIO0 *	45
	GPIO1 *	46
	GPIO2 *	47
	GPIO3 *	48
	GPIO4 *	49
	GPIO5 *	50
	GPIO6 *	51
	GPIO7 *	52
	GPIO8 *	53
	GPIO9 *	60
	GPIO10 *	61
	GPIO11 *	62
CODEC #1 Interface	SCLK1	76
	SDFS1	77
	SDI1	78
	SDO1	79

Function	Pins	Pin Number
Serial CODEC / AC-link #2 Interface	SDO2	55
	SDI2	56
	SDFS2	57
	SDFS3	58
	SCLK2	59
Clocks	OSCI	64
	OSCO	65
	C24	83
Game Port Interface	GD[3:0]	70:67
	GD[5:4]	72:71
	GD6 *	73
	GD7 *	74
Hardware Volume Control Pins	VOLDN *	49,74
	VOLUP *	50,73
I^2S Interface	ISCLK (I^2SCLK) *	51
	ILR (I^2SLR) *	52
	IDATA (I^2SDATA) *	53
DSP Serial Interface	ISCLK *	45
	IDO *	46
	IDI *	47
	ILR *	48
Power Pins	VCC	100,86,66, 54,32,12
	GND	91,88,75,63, 44,41,22,3

* These pins share more than one function.

POWER MANAGEMENT

The Maestro-2 is a high-performance device with low power consumption. Besides the low-power CMOS technology used to process the Maestro-2, various features are designed into the device to provide benefits from popular power-saving techniques. These features and techniques are discussed in this section.

CLKRUN Protocol

The PCI CLKRUN feature is one of the primary methods of power management on the PCI bus interface of the Maestro-2 for the notebook computer. Since some chipsets do not implement CLKRUN, this is not always available to the system designer, and alternate power-saving features are provided.

PCI Power Management Interface (PPMI)

The PCI Power Management Interface (PPMI) specification establishes the infrastructure required to let the operating system control the power of PCI functions. This is done by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI functions can be assigned one of five power management states that result in varying levels of power savings.

The five power-management states of PCI functions are:

- D0 – full power
- D1 and D2 – intermediate states
- D3 hot – off state; power supply is on
- D3 cold – off state; power supply is off

For the operating system to manage the device power states on the PCI bus, the PCI function should support four power-management operations:

– capabilities reporting
– power status reporting
– setting the power state
– system wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of new capabilities is indicated by setting bit [4] in the PCI Status register and providing access through a capabilities pointer to a capabilities list.

The capabilities pointer provides access to the first item in the linked list of capabilities. For the Maestro-2, the capabilities pointer is mapped to an offset, C0h, indicated in the PCI Configuration register at 34h. The first byte of each capability register block is required to be a unique ID of the capability. PCI power management has been assigned an ID of 01h. The next byte is a pointer to the next pointer item in the list of capabilities. There are no more items in the list, so the next item pointer is set to zero. The registers following the next item pointer are specific to that function's capability. The PPMI capability implements the register block outlined in Table 1.

The Power-Management Capabilities register (PCI Configuration register C2h in the Maestro-2) is a static read-only register that provides information on the capabilities of the functions related to power-management. The Power-Management Control/Status register enables control of power-management states and enables and monitors power-management events. The Data register is an optional register that displays state-dependent power measurements such as power consumed or heat dissipation.

Table 1 Power-Management Registers

Register Name				**Offset**
Power-Management capabilities		Next-Item pointer	Capability ID	0
Data	PMCSR bridge support extensions	Power-Management control status (CSR)		4

ACPI Transition Diagram

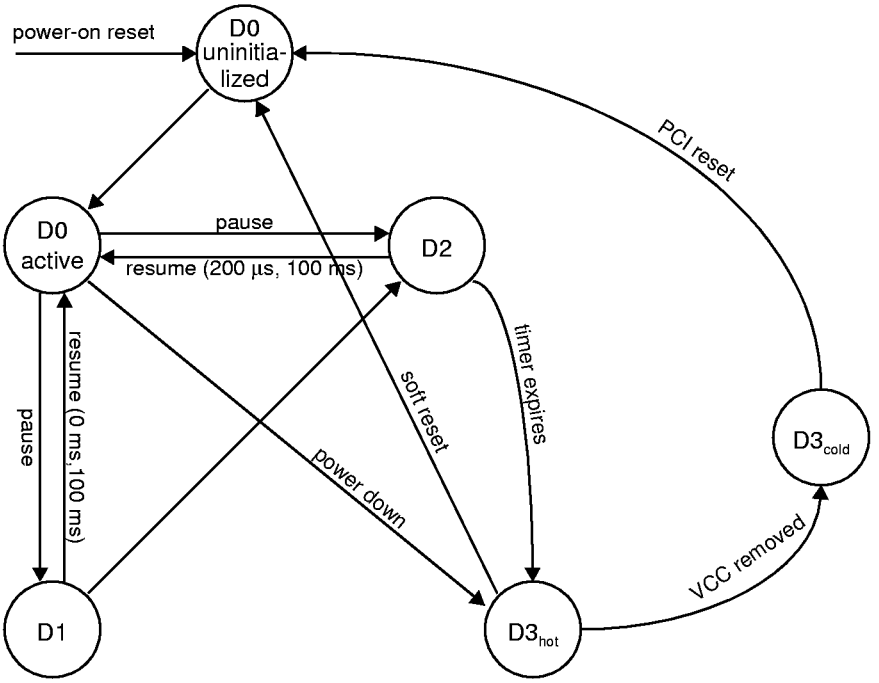


Figure 4 ACPI Transition Diagram

DISABLING MAESTRO-2 AUDIO

To disable Maestro-2 audio in both notebook and motherboard implementations:

1. Set PCI 04h[2:0] = 000.

   This disables Maestro-2 response to all inputs and outputs and Bus Master cycles.

2. Set PCI 40h[7] = 1.

   This disables Maestro-2 response to all legacy audio functions.

PCI CONFIGURATION REGISTERS

Register Summary

Table 2 PCI Configuration Registers Summary

2F	20	1F	0	Offset
Device ID		Vendor ID		00h
Device capability		Status	Command	04h
Base class code	Sub-class code	Programming interface identifier	Revision ID	08h
BIST capability	Header type	Latency timer	Cache line size	0Ch
Reserved		Maestro-2 I/O space base address		10h
Reserved				14h
Reserved				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID (R/W protected)		Subsystem vendor ID (R/W protected)		2Ch
Reserved				30h
Reserved			Capability pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt pin	Interrupt line	3Ch
Reserved		Legacy audio control		40h
Reserved		Reserved		44h
Reserved		Reserved		48h
Reserved		Reserved		4Ch
Maestro-2 configuration B		Maestro-2 configuration A		50h
Reserved		ACPI control		54h
Reserved		Reserved		58h
Reserved		Reserved		5Ch
Reserved		Distributed DMA		60h
Power-Management capabilities		Next-Item pointer	Capability ID	C0h
Reserved		Power-Management control/status		C4h

All reserved locations are read-only with a default value of zero.

Register Descriptions

Vendor ID (00h, 01h, R)

Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Vendor ID	Identifies ESS as the manufacturer of this device. The ID for ESS is 125Dh.

Device ID (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies Maestro-2 as this device. This ID 1968h is assigned by ESS Technology, Inc.

Command (04h, R/W)

0	0	0	0	0	BM	MS	IO
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:3	–	Read-only. Returns 0 when read.
2	BM	Bus Master enable/disable. 1 = Enable bus master. 0 = Not bus master.
1	MS	Memory Space access enable/disable. 1 = Enable memory space access. 0 = Disable memory space access.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Status (05h, R)

0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	–	Read-only. Returns 00h when read.

Device Capability (06h, 07h, R)

Device capability															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	DC	The device capability code is 0290h.

Revision ID (08h, R)

Revision ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	Revision ID	Identifies the revision of this device. The ID 00h is assigned by ESS Technology, Inc.

Programming Interface Identifier (09h, R)

Programming interface identifier							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	PII	Identifies the programming interface of this device. The ID 00h is assigned by ESS Technology, Inc. as a default interface.

Sub-Class Code (0Ah, R)

Sub-Class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. The ID 01h is assigned by ESS Technology, Inc. as an audio device.

Base Class Code (0Bh, R)

Base class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. The ID 04h is assigned by ESS Technology, Inc. as a multimedia device.

Cache Line Size (0Ch, R/W)

Cache line size							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CLS	Identifies the cache line size of this device as 00h.

Latency Timer (0Dh, R/W)

Latency timer				0	0	0	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	LT	Number of clocks times 16.
3:0	–	Read-only. Returns 0 when read.

Header Type (0Eh, R)

SM	Configuration space layout						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SM	Single-/multi-function device. The Maestro-2 supports single-function operation. 0 = Single-function device.
6:0	CSL	Configuration space layout. Read-only. Defines layout for bytes 10h and up of the PCI configuration space header. Maestro-2 supports a 00h header type.

BIST Capability (0Fh, R)

Built-in self test capability							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BIST	Built-in self test capability is 00h.

Maestro-2 I/O Space Base Address (10h, 11h, R/W)

IOSB[15:8]								0	0	0	0	0	0	0	ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 256-Byte I/O space.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

Subsystem Vendor ID (2Ch, 2Dh, R)

Subsystem vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID	Read/write protected. Customizable through register programming. Writable when PCI 50h[0] = 1.

Subsystem ID (2Eh, 2Fh, R)

Subsystem ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID	Read/write protected. Customizable through register programming. Writable when PCI 50h[0] = 1.

Capability Pointer (34h, R)

Capability pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CP	This register provides a pointer into the PCI configuration header where the PCI power management register block resides. PCI header doublewords at C0h and C4h provide the power management (PM) registers. Each socket has its own capability pointer register. This register is read-only and returns C0h when read.

Interrupt Line (3Ch, R/W)

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the Maestro-2 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (Maestro-2's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. The default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Pin (3Dh, R)

Interrupt pin							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IP	Interrupt pin information. Indicates which interrupt pin the Maestro-2 is using. This register is read-only and returns 01h when read, which indicates INTA#.

Minimum Grant (3Eh, R)

Minimum grant							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	MG	Min_Gnt. Identifies the burst period needed. This register is read-only and returns 02h when read, which corresponds to 500 ns.

Maximum Latency (3Fh, R)

Maximum latency							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	ML	Max_Lat. Identifies how often bus access is needed. This register is read-only and returns 18h when read, which corresponds to 6 ms.

Legacy Audio Control (40h, 41h, R/W)

LA	SIR	MIDIIRQ			SBIRQ			DMACH		IA	MQ	MI	GM	FM	SB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	LA	Legacy audio disable. 0 = Enable legacy audio. 1 = Disable legacy audio (default).
14	SIR	Serial IRQs enable. 0 = Disable serial IRQs (default). 1 = Enable serial IRQs.
13:11	MIDIIRQ	MIDI I/O IRQ select. Read-only. Default to 010.
10:8	SBIRQ	Sound Blaster IRQ select.

Bit 10	Bit 9	Bit 8	IRQ Selection
0	0	0	IRQ5
0	0	1	IRQ7
0	1	0	IRQ9
0	1	1	IRQ10
1	x	x	Reserved

Bits	Name	Description
7:6	DMACH	Sound Blaster DMA channel select.

Bit 7	Bit 6	DMA Channel Selection
0	0	Channel 0
0	1	Channel 1 (default)
1	0	Reserved
1	1	Channel 3

5	IA	I/O address aliasing control. 0 = Disable address aliasing. 1 = Enable address aliasing (default). Selects 10-bit I/O.
4	MQ	MPU-401 IRQ enable. 0 = Disable MPU-401 IRQ. 1 = Enable MPU-401 IRQ (default).
3	MI	MPU-401 I/O enable. 0 = Disable MPU-401 I/O. 1 = Enable MPU-401 I/O (default).
2	GM	Game port enable. 0 = Disable game port. 1 = Enable game port (default).
1	FM	FM synthesis enable. 0 = Disable FM synthesis. 1 = Enable FM synthesis (default).
0	SB	Sound Blaster enable. 0 = Disable Sound Blaster channel. 1 = Enable Sound Blaster channel (default).

Legacy Audio Support

The Maestro-2 supports the following legacy audio addresses.

Table 3 Supported Legacy Audio Addresses

Legacy Audio Resources	I/O Address Base
Sound Blaster Pro	220h/240h
FM synthesis	388h
MPU-401	300h/320h/330h/340h
DMA	Channel 0, 1, 3
IRQ	5, 7, 9, 10

Maestro-2 Configuration A (50h, 51h, R/W)

Reserved	GM	R	DMAP	PW	R	M4D	S2	R	S(V)ID
15 14 13	12	11	10 9 8	7	6 5	4 3	2	1	0

Bit Definitions:

Bits	Name	Description
15:13	–	Reserved.
12	GM	High-performance game port mode enable. 0 = Disable game port. 1 = Enable game port.
11	–	Reserved.
10:8	DMAP	ISA DMA policy. Bit 10 Bit 9 Bit 8 DMA Policy 0 0 0 Distributed DMA 0 0 1 Transparent DMA 0 1 0 PC/PCI DMA 0 1 1 Reserved 1 x x Reserved
7	PW	EN_PW. Posted write enable. 0 = Disable Maestro-2 posted write. 1 = Enable Maestro-2 posted write.
6:5	–	Reserved.
4:3	M4D	MPU_401_DECODE. Bit 4 Bit 3 MPU-401 I/O 0 0 33x 0 1 30x 1 0 32x 1 1 34x
2	S2	SB240. Sound Blaster decode. 0 = Sound Blaster decode is 22x. 1 = Sound Blaster decode is 24x.
1	–	Reserved.
0	SID	Write-enable bit for PCI subsystem ID (SID) and subsystem vendor ID (SVID). 0 = Read-only (default). 1 = Read/write.

Maestro-2 Configuration B (52h, 53h, R/W)

ICx	CIS	CxS	R	PMC	CLKSL	R	HWV	DHE	HVI	DE	Reserved
15	14	13	12	11	10 9	8	7	6	5	4	3 2 1 0

Bit Definitions:

Bits	Name	Description
15	ICx	Internal clock multiplier enable. 0 = Disable internal clock multiplier. 1 = Enable internal clock multiplier.
14	CIS	Maestro-2 clock input select. 0 = Select the clock from an external crystal oscillator. 1 = Select the clock from the internal clock multiplier.
13	CxS	Clock multiplier mode select. 0 = Select mode 0. 1 = Select mode 1.
12	–	Reserved.
11	PMC	Power management control for CLKRUN# enable. 0 = Disable PM control for CLKRUN#. 1 = Enable PM control for CLKRUN#.
10:9	CLKSL	Clock divider select for Sound Blaster. Bit 10 Bit 9 Clock Divider 0 0 Divided by 48 0 1 Divided by 49 1 0 Divided by 50 1 1 Reserved
8	–	Reserved.
7	HWV	Hardware volume control enable. 0 = Disable hardware volume control. 1 = Enable hardware volume control.
6	DHE	Reduced debounce for hardware volume control enable. 0 = Disable reduced debounce. 1 = Enable reduced debounce.
5	HVI	Up/down hardware volume button input select. 0 = Select input from GPIO[5:4]. 1 = Select input from GD[7:6].
4	DE	DSP interface enable. 0 = Disable the DSP interface/CHI bus. 1 = Enable the DSP interface/CHI bus.
3:0	–	Reserved.

ACPI Control A (54h, 55h, R/W)

R	24	R	GLUE	DAA	PIF	HV	GPIO	DSP	SB	FM	RB	MIDI	GP	WP
15	14	13 12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control A register sets the state (D1 or D2) of the stop clock for each module (24 MHz clocks, GLUE, DAA, PCI interface, hardware volume, modem/GPIO, DSP interface, Sound Blaster, FM, ring bus/AC-link, MIDI, game port, and Wave Processor).

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14	24	ACPI stop clock control for the 24 MHz clock to the C24 output. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
13:12	–	Reserved.
11	GLUE	ACPI stop clock control for GLUE. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
10	DAA	ACPI stop clock control for DAA power-down control. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.

Bits	Name	Description
9	PIF	ACPI stop clock control for the PCI interface. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
8	HV	ACPI stop clock control for hardware volume control. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
7	GPIO	ACPI stop clock control for Modem/GPIO. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
6	DSP	ACPI stop clock control for the DSP interface. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
5	SB	ACPI stop clock control for Sound Blaster. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
4	FM	ACPI stop clock control for FM. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
3	RB	ACPI stop clock control for Ring Bus/AC-link. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
2	MIDI	ACPI stop clock control for MIDI. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
1	GP	ACPI stop clock control for the game port. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.
0	WP	ACPI stop clock control for the Wave Processor. 0 = Set stop clock to state D1. 1 = Set stop clock to state D2.

ACPI Control B (56h, 57h, R/W)

R	24	R	GLUE	DAA	PIF	HV	GPIO	DSP	SB	FM	RB	MIDI	GP	WP
15	14	13 12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control B register enables the clock at the state (D1 or D2) set for each module in the ACPI Control A register.

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14	24	ACPI stop clock enable for the 24 MHz clock to the C24 output. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
13:12	–	Reserved.
11	GLUE	ACPI stop clock enable for GLUE. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
10	DAA	ACPI stop clock enable for DAA power-down control. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
9	PIF	ACPI stop clock enable for the PCI interface. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
8	HV	ACPI stop clock enable for hardware volume control. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
7	GPIO	ACPI stop clock enable for Modem/GPIO. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
6	DSP	ACPI stop clock enable for the DSP interface. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
5	SB	ACPI stop clock enable for Sound Blaster. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
4	FM	ACPI stop clock enable for FM. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
3	RB	ACPI stop clock enable for Ring Bus/AC-link. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
2	MIDI	ACPI stop clock enable for MIDI. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
1	GP	ACPI stop clock enable for the game port. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.
0	WP	ACPI stop clock enable for the Wave Processor. 0 = Stop clock at state D1/D2 disabled. 1 = Enable stop clock at state D1/D2.

Distributed DMA Control (60h, 61h, R/W)

DMA[15:4]	0	0	0	DE
15 14 13 12 11 10 9 8 7 6 5 4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	DMA[15:4]	Distributed DMA base address.
3:1	–	Always write 0.
0	DE	Distributed DMA enable. 0 = Disable distributed DMA. 1 = Enable distributed DMA

Capability ID (C0h, R)

Capability ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CID	This register identifies the linked list item as the register for PCI power management. This register is read-only and returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Next-Item Pointer (C1h, R)

Next-Item pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NIP	This register is used to indicate the next item in the linked list of the PCI power management capabilities. Since Maestro-2 functions only include one capabilities item, this register is read-only and returns 00h when read.

Power-Management Capabilities (C2h, C3h, R)

0	1	1	1	0	1	1	0	0	0	1	0	0	0	0	1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:11		PME_Support. This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PCE# signal while in that power state. Bit [15] = 0. PME# cannot be asserted from $D3_{cold}$. Bit [14] = 1. PME# can be asserted from $D3_{hot}$. Bit [13] = 1. PME# can be asserted from D2. Bit [12] = 1. PME# can be asserted from D1. Bit [11] = 0. PME# can not be asserted from D0. Value of bits 15:11 = 01110.
10		D2_Support. This bit indicates that this function supports the D2 power management state. Value of bit 10 = 1.
9		D1_Support. This bit indicates that this function supports the D1 power management state. Value of bit 9 = 1.
8:6	–	Reserved. Value of bits 8:6 = 000.
5		DSI. The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. Value of bit 5 = 1.
4		Reserved. Value of bit 4 = 0.
3		PME clock. This bit indicates that no PCI clock is required for the function to generate PME#. Value of bit 3 = 0.
2:0		Version. This 3-bit field indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification. Value of bits 2:0 = 001.

Power-Management Control/Status (C4h, R/W)

0	0	0	0	0	0	PWR STATE	
7	6	5	4	3	2	1	0

The default value of this register 00h. This register determines and changes the current power state of the Maestro-2 function. The contents of this register are not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state.

Bit Definitions:

Bits	Name	Description
7:2	–	Bits [7:2] are read-only and return 0 when read.
1:0	PS	Power state. This 2-bit field is used both to determine the current power state of a function, and to set the function into a new power state. This field is encoded as: Bit 1 Bit 0 Power State 0 0 D0 0 1 D1 1 0 D2 1 1 $D3_{hot}$

PME Control (C5h, R/W)

PME ST	0	0	0	0	0	0	PME EN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	PME ST	PME# status. Write: 1 = Clear PME# status. Read: 1 = PME# is active.
6:1	–	Bits [6:1] are read-only and return 0 when read.
0	PME EN	PME# enable. 0 = Disable PME. 1 = Enable PME.

WAVECACHE

The WaveCache dynamically prefetches from the system memory and manages samples for the Wave Processor (WP). The WaveCache is capable of handling up to 64 separate data streams for the WP. The types of different data streams supported include 16-bit mono, 16-bit stereo, 8-bit mono, 8-bit stereo, and 8-bit differential. The WaveCache also interfaces with the Task-Oriented Signal Processor (TOSP) to handle FM synthesis data streams.

Applicable Registers

Address	Name
Maestro2M_Base +10h, +11h	WaveCache Index register
Maestro2M_Base+12h, +13h	WaveCache Data register
Maestro2M_Base+14h,+15h	WaveCache Control register

WaveCache Configurations

The WaveCache has three different configurations:

- WP configuration
- TOSP configuration
- Test configuration

These configurations are set by WaveCache Control register bits [0], and [9:7].

The primary configuration, the WP configuration, is where the WaveCache manages samples for the WP. The CPU may write into WaveCache Control registers or WaveCache channel buffers using the WaveCache Index and Data register.

In the TOSP configuration, the WaveCache serves as a general-purpose data buffer for the TOSP. Only the TOSP may access the WaveCache in this configuration.

The Test configuration is for device test purposes, in which only the CPU may read/write the WaveCache. It is enabled by setting bit [0] of the WaveCache control register to 1.

WaveCache Access

The host may access the WaveCache with limitations using the WaveCache Index and Data registers. By setting up the Index register first, the actual read/write to and from the WaveCache registers occur when the indexed data register is read or written. The host may write to the WaveCache in either WP configuration or Test configuration modes, but may only read from the WaveCache when in Test configuration mode.

Table 4 WaveCache Indexed Data Registers

Index	Register
1F4 – 1FF	Wavetable Base Address register 1:0
1F0 – 1F3	PCM/Status FIFO Base Address register 3:0
n* (08 hex)	Channel n Control register, n = 61:0
other locations	Channel buffers

Wavetable Base Address **(R/W)**

Data[27:12]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

There are a total of twelve Wavetable Base Address registers. Up to four disjoint table addresses can be specified in these twelve registers. The purpose of these registers is to allow the WP channels to deal with only logical addresses.

The Maestro-2M supports wavetable sizes from 1 MB to 8 MB in system memory. This wavetable is divided into four equal sizes and these wavetable quarters can reside in physically disjoint locations mapped by the twelve base address registers. Depending on the different wavetable sizes, different top channel address bits (2 bits) are used to select the corresponding base address register and thus the quarter wavetable. Physical address is calculated by adding the base address and the WP address together.

Table 5 WaveCache Top Channel and Physical Address

Top Channel Address Bits	Physical Address
WPWA[1][18:15] (1 MB)	m = 14 (1 MB)
WPWA[19:16] (2 MB)	m = 15 (2 MB)
WPWA[20:17] (4 MB)	m = 16 (4 MB)
WPWA[21:18] (8 MB)	m = 17 (8 MB)
0000	WTBAR0[27:12] + WPWA[m:0][2]
0001	WTBAR1[27:12] + WPWA[m:0]
0010	WTBAR2[27:12] + WPWA[m:0]
0011	WTBAR3[27:12] + WPWA[m:0]
0100	WTBAR4[27:12] + WPWA[m:0]
0101	WTBAR5[27:12] + WPWA[m:0]
0110	WTBAR6[27:12] + WPWA[m:0]
0111	WTBAR7[27:12] + WPWA[m:0]
100-	WTBAR8[27:12] + WPWA[m+1:0]
101-	WTBAR9[27:12] + WPWA[m+1:0]
110-	WTBAR10[27:12] + WPWA[m+1:0]
111-	WTBAR11[27:12] + WPWA[m+1:0]

1. WPWA (WP WaveSpace Address) is measured in words.
2. When the WaveCache adds WTBARn addresses (bytes) and WPWA addresses (words), its address mapping hardware automatically performs the necessary shifting.

PCM/Status FIFO Base Address (R/W)

PCM/Status FIFO base address[27:12]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 6 PCM Top Channel and Physical Address

Top Channel Address Bits	Physical Address
WPWA[1][22:21]	m = 20
00	PCMBAR0[27:12] + WPWA[m:0][2]
01	PCMBAR1[27:12] + WPWA[m:0]
10	PCMBAR2[27:12] + WPWA[m:0]
11	PCMBAR3[27:12] + WPWA[m:0]

1. WPWA (WP WaveSpace Address) is measured in words.
2. When the WaveCache adds PCMBARn addresses (bytes) and WPWA addresses (words), its address mapping hardware automatically performs the necessary shifting.

The PCM/Status FIFO Base Address register is used in one of the following two situations:

3. The WP writes status information to the System Status FIFO.
4. WPWA22 is '1' in accessing system memory.

Channel Control for Channels 0-61 (R/W)

Tag address[15:3]													8B	SA	DA
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	TA	Address tag. Before a WP channel is activated, an invalid tag address must be loaded into the Tag address bits. Tag address[15:3] corresponds to physical address [15:3]. An invalid tag is an address that is at least 10 hex away from the starting sample address of the channel. For example, if a channel is accessing samples in: – incremental address style: [Channel starting address - 10h] can be written to bits [15:3]. – decremental address style: [Channel starting address +10h] can be written to bits [15:3].
2	8B	8-Bit format. To play 8-bit unsigned-magnitude samples, set bit [2]. In this format, MSB bits [15] and [7] of the input samples are toggled.
1	SA	Stereo format. 1 = Channel samples are in interleaved stereo format. Left and right samples are confined to paired adjacent channels. For example: channels 0/1 are stereo paired channels, and channels 1/2 are not. The SA bits of both paired channels must be set to 1.
0	DA	Decremental addressing. 1 = Channel is accessing samples in decremental address order. 0 = Channel is accessing samples in incremental address order.

Programming the WaveCache

The outlined steps for programming the WaveCache are:

1. Determine the size and locations of the wavetable in system memory.
2. Program the WaveCache Control register:
   – WaveCache configuration = WP configuration
   – Wavetable size
   – EN_WaveCache = 1
3. Program the Wavetable Base Address registers.
4. Program the WP channels:
   – Program Channel Control register for the following:
   data format
   incremental/decremental addressing
   invalid tag address
   – Program the WP Channel Parameter registers
5. Repeat step 4 for all channels.

CODEC/MIXER INTERFACE

The Maestro-2 supports the AC'97 CODEC mode, which supports interface to AC97-compliant CODECs.

Applicable Registers

Address	Name
Maestro2_Base +30h	CODEC Command/Status
Maestro2_Base +32h, +33h	CODEC Data register

AC'97 Interface

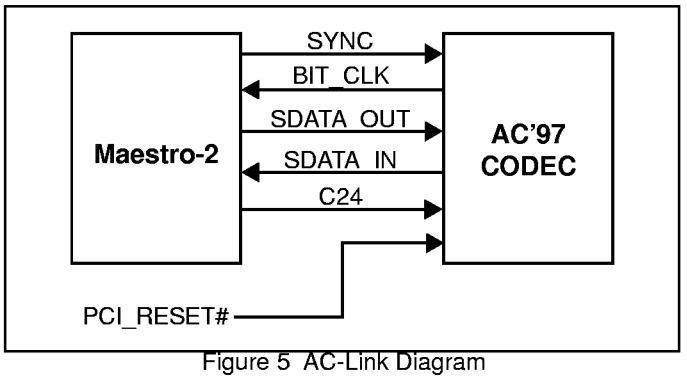


Figure 5 AC-Link Diagram

AC'97 Serial Interface Timing

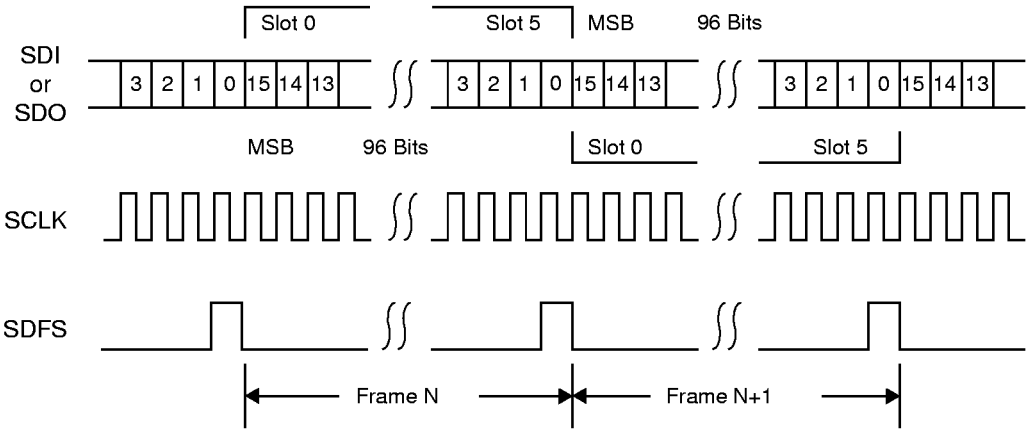


Figure 6 Serial Interface Timing

APPLICATION SPECIFIC SIGNAL PROCESSOR

Applicable Registers

Address	Name
Maestro2_Base +80h, +81h	ASSP Memory Index Port
Maestro2_Base +82h, +83h	ASSP Memory Port
Maestro2_Base +84h, +85h	ASSP Data Port
Maestro2_Base +A0h	ASSP Control A register
Maestro2_Base +A2h	ASSP Control B register
Maestro2_Base +A4h	ASSP Control C register
Maestro2_Base +A6h	ASSP Control D register
Maestro2_Base +A8h	Host Write Index register
Maestro2_Base +AAh	Host Write Data register
Maestro2_Base +ACh	ASSP to Host IRQ Status register

ASSP Memory Mapping

ASSP can access internal memory only. There are 1.512K words of space for program usage and 3.608K words of space for data usage.

Table 7 ASSP Memory Mapping

Type of Memory	Addresses	Description
Program memory	0h – 1FFh	512 W SRAM
	0800h – 0BFFh	1 KW SRAM
Data memory	0 – 005Fh	96 W registers
	400h – 5FFh	512 W wavecache
	1000h – 17FFh	2 KW SRAM
	2000h – 2BFFh	3 KW ROM (mapped to 1K ROM physically)

ASSP I/O Mapping

Table 8 ASSP I/O Mapping

Addresses	Description
0000h – 0FFFh	FM
1000h – 1FFFh	Hardware volume status input
2000h – 2FFFh	Ring bus input full
3000h – 3FFFh	Ring bus output empty
4000h – 4FFFh	ASSP DMA I/O port
5000h – 5FFFh	ASSP-to-host IRQ
6000h – 6FFFh	I²S time stamp
7000h – 7FFFh	I²S data input even DWord = left, odd DWord = right
8000h – 8FFFh	DSP serial bus data input
9000h – 9FFFh	ES2818 reset
A000h – AFFFh	ASSP stop clock

DMA Control Registers

Host DMA Base Address Low (IO 4000h, W)

A[15:2]														Reserved	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:2	A[15:2]	Dword address corresponding to A[15:2] of the system memory.
1:0	–	Reserved. Fixed at 0 for Dword addressing.

Host DMA Base Address High (IO 4001h, W)

Reserved				A[27:16]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved. Fixed at 0h for Dword addressing.
11:0	A[27:16]	Dword address corresponding to A[27:16] of the system memory.

ASSP DMA Base Address (IO 4002h, W)

R	R/W	Reserved											Offset		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

An IO write cycle to 4002h triggers the ASSP DMA transfer.

The ASSP DMA base address is fixed at 1300h in data memory. A 3-bit offset extends the address range from 1300h to 1370h.

Each ASSP DMA transfer is fixed at 32 bytes.

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14	R/W	Read/write host/ASSP memory. 1 = Read ASSP memory; write host memory. 0 = Read host memory; write ASSP memory.
13:3	–	Reserved.
2:0	Offset	Offset address from the ASSP DMA base address

Data Transfer Between ASSP and Host Memories

The Maestro-2 supports two methods of data transfer between ASSP and host memory. CPU access through 32-bit IO is supported for small transfers. For large transfers, DMA is supported for transferring data to and from ASSP memory. Both the ASSP program and data memory spaces are accessible using these two methods. DMA operation can also be used for dynamic downloading of ASSP programs. Both types of transfer put the ASSP in a hold state.

32-Bit I/O Transfer Operation

To perform an IO transfer between the CPU and the ASSP:

1. Program the ASSP Memory Index port (Maestro2_Base +80h, +81h) with the ASSP starting address in word boundary using 16-bit IO.
2. Set the ASSP Memory port (Maestro2_Base+82h, +83h) bits [1:0] to select either program or data memory. See Table 9 for the settings.
3. Send a 32-bit read or write IO operation to the ASSP Data port (Maestro2_Base +84h, +85h) starting with the programmed ASSP address programmed in step 1. 16-Bit IO operations are not supported. The ASSP Memory Index port auto-increments for subsequent IO operations.

DMA Transfer Operation

The following explains how to set up the ASSP to perform DMA between the Host and the ASSP. The ASSP controls the DMA operation by writing to I/O ports 4000h to 4002h.

1. The low 16 bits and the high 16 bits of the host memory base address are written into I/O ports 4000h and 4001h.
2. I/O port 4002h bit [14] controls the direction of the DMA operation by specifying whether it is from the host memory or from the ASSP memory. Bits [2:0] control the offset address from the DSP DMA base address.
3. At the end of the DMA transfer, the END of ASSP DMA interrupt is sent to the ASSP.

Each DSP DMA transfer is fixed at 32 bytes.

Table 9 ASSP Address Map

ASSP Transfer Address [17:16]	Mapped ASSP Resources
10	Program memory
11	Data memory

Messaging Between the CPU and the ASSP

Outside of DMA transfers, the CPU can send messages to the ASSP with associated interrupts to the ASSP. The messages are sent through two 8-bit registers:

- Host Write Index register
- Host Write Data register

The ASSP receives an interrupt whenever the Host Write Data register is written by the CPU. The ASSP can read the data and the index sent by the CPU from the I/O port.

The ASSP has the ability to generate one of eight software interrupts to the CPU. The CPU may examine the ASSP Interrupt Status register to determine the nature of the interrupt.

ASSP Interrupts

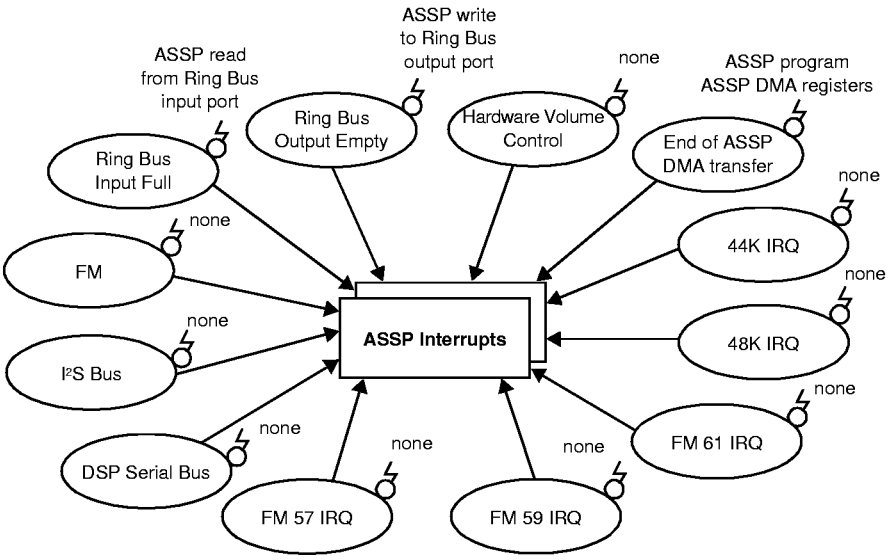


Figure 7 ASSP Interrupt Map

Table 10 ASSP Interrupts

Interrupt	Function
0	ASSP reset
1	ASSP FM
2	ASSP hardware volume control
3	ASSP 44K IRQ
4	ASSP 48K IRQ
5	ASSP ring bus input full
6	ASSP ring bus output empty
7	ASSP end of ASSP DMA transfer
8	ASSP FM channel 57 IRQ
9	ASSP FM channel 59 IRQ
10	ASSP FM channel 61 IRQ
11	ASSP DSP serial bus input
12	ASSP I²S input

I/O PORTS

Port Summary

Table 11 Maestro-2 I/O Port Summary

Function	Port	Register (Number of Bytes)	Notes
Direct Sound Processor	Maestro2_Base+00h	Data (2)	
	+02h	Index (2)	
	+04h	Interrupt Status (2)	
	+06h	Sample_Count (2)	Read-only
WaveCache	Maestro2_Base+10h	WaveCache Index (2)	
	+12h	WaveCache Data (2)	
	+14h	WaveCache Control (2)	
Host Interrupt	Maestro2_Base+18h	Host Interrupt Control (2)	
	+1Ah	Host Interrupt Status (1)	
Hardware Volume Control	Maestro2_Base+1Bh	Hardware Volume Control (1)	
	+1Ch	Shadow of Mixer for Voice (1)	
	+1Dh	HWV Counter for Voice (1)	
	+1Eh	Shadow of Mixer for Master (1)	
	+1Fh	HWV Counter for Master (1)	
High-Performance Game Port	Maestro2_Base+20h	Delay 0 (2)	
	+24h	Delay 1 (2)	
	+28h	Delay 2 (2)	
	+2Ch	Delay 3 (2)	
CODEC Interface	Maestro2_Base+30h	Command / Status (1)	
	+32h	Data (2)	
Ring Bus	Maestro2_Base+34h	Ring Bus Control (4)	
GPI/O General-Purpose I/O	Maestro2_Base+60h	GPIO Data (2)	
	+64h	GPIO Mask (2)	
	+68h	GPIO Direction (2)	
ASSP Application Specific Signal Processor	Maestro2_Base+80h	ASSP Memory Index Port (4)	
	+84h	ASSP Memory Data Port (2)	
	+A2h	ASSP Control register A (1)	
	+A4h	ASSP Control register B (1)	
	+A6h	ASSP Control register C (1)	
	+A8h	Host Write Index register (1)	
	+AAh	Host Write Data register (1)	
	+ACh	ASSP to Host Interrupt Status (1)	

Port Descriptions

Data (Maestro2_Base+00h, +01h, R/W)

Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Data	Data.

Index (Maestro2_Base+02h, +03h, R/W)

Index															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Index	Index.

Interrupt Status (Maestro2_Base+04h, +05h, R/W)

IRQ status															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	IRQ status	Interrupt status.

Sample_Count (Maestro2_Base+06h, +07h, R)

Sample count															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Sample count	Sample_count. Read-only.

WaveCache Index (Maestro2_Base+10h, +11h, R/W)

0	0	0	0	0	0	0	WCA								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:9	–	Reserved. Always write 0.
8:0	WCA	WaveCache index.

WaveCache Data (Maestro2_Base+12h, +13h, R/W)

WCDA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:0	WCD	WaveCache data.

WaveCache Control (Maestro2_Base+14h, +15h, R/W)

0	0	0	0	0	0	XCH	EW	CEN	WTS[1:0]		R	SGC		R	WT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:10	–	Reserved.
9	XCH	Channels 56/57, channels 58/59 enable. 1 = Enable ch56/57, ch58/59 as the extra playback/record channel. 0 = Disable ch56/57, ch58/59 as the extra playback/record channel.
8	EW	EN_WaveCache. WaveCache operation enable. 1 = Enable WaveCache operation. 0 = Disable WaveCache operation.
7	CEN	Channels 60/61 enable. 1 = Enable ch60/61 as the playback/record channels. 0 = Disable ch60/61 as the playback/record channels.
6:5	WTS	Wavetable size. Bit 6 Bit 5 Wavetable Size 0 0 1 MB 0 1 2 MB 1 0 4 MB 1 1 8 MB
4	–	Reserved.
3:2	SGC	Scatter and gather DMA control. Bit 3 Bit 2 Channels 0 0 Disable 0 1 Channels 40-47 are in SG mode; Channels 52-55 cannot read PCI memory through WaveCache 1 0 Channels 32-47 are in SG mode; Channels 48-55 cannot read PCI memory through WaveCache 1 1 Reserved
1	–	Reserved.
0	WT	WaveCache test mode enable. 1 = Enable WaveCache test mode. CPU may read/write WaveCache in this mode.

Host Interrupt Control (Maestro2_Base+18h, +19h, R/W)

MR	DR	R	PGE	R	CR	R	HIE	R	DIE	R	DSIE	MIE	SI
15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	MR	Maestro-2 software reset enable. 0 = Disable Maestro-2 software reset. 1 = Enable Maestro-2 software reset.
14	DR	DirectSound software reset enable. 0 = Disable DirectSound software reset. 1 = Enable DirectSound software reset.
13:11	–	Reserved.
10	PGE	Hardware volume control to PME# generation enable.
9	–	Reserved.
8	CE	CLKRUN# generation enable. 0 = Disable CLKRUN# generation. 1 = Enable CLKRUN# generation.
7	–	Reserved.
6	HIE	Hardware volume control interrupt enable. 0 = Disable hardware volume control interrupt. 1 = Enable hardware volume control interrupt.
5	–	Reserved.
4	DIE	ASSP software interrupt enable. 0 = Disable ASSP software interrupt. 1 = Enable ASSP software interrupt.
3	–	Reserved.
2	DSIE	DirectSound interrupt enable. 0 = Disable DirectSound interrupt. 1 = Enable DirectSound interrupt.
1	MIE	MPU-401 receive interrupt enable. 0 = Disable MPU-401 receive interrupt. 1 = Enable MPU-401 receive interrupt.
0	SIE	Sound Blaster interrupt enable. 0 = Disable Sound Blaster interrupt. 1 = Enable Sound Blaster interrupt.

Host Interrupt Status (Maestro2_Base+1Ah, R/W)

R	IHWV	R	ID	R	4V	4M	BS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	IHWV	Hardware volume control interrupt. 0 = No hardware volume control interrupt. 1 = Hardware volume control interrupt pending.
5	–	Reserved.
4	ID	ASSP software interrupt. 0 = No ASSP interrupt. 1 = ASSP interrupt pending.
3	–	Reserved.
2	4V	DirectSound interrupt. 0 = No DirectSound interrupt. 1 = DirectSound interrupt pending.
1	4M	MPU-401 receive interrupt. 0 = No MPU-401 receive interrupt. 1 = MPU-401 receive interrupt pending.
0	BS	Sound Blaster interrupt. 0 = No Sound Blaster interrupt. 1 = Sound Blaster interrupt pending.

Hardware Volume Control (Maestro2_Base+1Bh, R/W)

Reserved	Split
7 6 5 4 3 2 1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved.
0	Split	Hardware volume/counter control register split. 1 = Split volume register from counter register. 0 = Do not split volume from counter register.

Shadow of Mixer Register for Voice (Maestro2_Base+1Ch, R/W)

Shadow of mixer register for voice
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	SMV	Shadow of the mixer register for voice.

HW Volume Control Counter for Voice (Maestro2_Base+1Dh, R/W)

Hardware volume control counter for voice
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	HCV	Hardware volume control counter for voice.

Shadow of Mixer Register for Master (Maestro2_Base+1Eh, R/W)

Shadow of mixer register for master
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	SMM	Shadow of the mixer register for master.

HW Volume Control Counter for Master (Maestro2_Base+1Fh, R/W)

Hardware volume control counter for master
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	HCM	Hardware volume control counter for master.

Joystick 1 X-Delay (Maestro2_Base+20h,+21h, R/W)

2A	2B	1A	1B	Delay[11:0]
15 14 13 12				11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 1 Y-Delay (Maestro2_Base+24h,+25h, R/W)

2A	2B	1A	1B	Delay[11:0]
15 14 13 12				11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 X-Delay (Maestro2_Base+28h,+29h, R/W)

2A	2B	1A	1B	Delay[11:0]
15 14 13 12				11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 Y-Delay (Maestro2_Base+2Ch,+2Dh, R/W)

2A	2B	1A	1B	Delay[11:0]
15 14 13 12				11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

CODEC Command / Status (Maestro2_Base+30h, W)

RW	AD[6:0]
7	6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7	RW	Read/Write. 0 = Write cycle. 1 = Read cycle.
6:0	AD[6:0]	CODEC register address.

CODEC Command / Status (Maestro2_Base+30h, R)

0	0	0	0	0	0	0	ST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved. Always read 0.
0	ST	Read/write status. 0 = CODEC register read/write is done. 1 = CODEC register read/write is in progress.

CODEC Data (Maestro2_Base+32h,+33h, W)

WT CODEC Data[15:0]
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	WT	16 bits of data to be written to the CODEC.

CODEC Data (Maestro2_Base+32h,+33h, R)

RD CODEC Data[15:0]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	RD	16 bits of data read from the CODEC.

Ring Bus Destination Control Format (Maestro2_Base+34h,+35h, R/W)

ADCL_DC				MODEM_DC				DirectSound_DC				ASSP_DC			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	ADCL_DC	ADCL_DC[3] = (Bit [15]) Mono/stereo select. 0 = Mono. 1 = Stereo. ADCL_DC[2:0] Destination ID select. Bit 14 Bit 13 Bit 12 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Modem input 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
11:8	MODEM_DC	MODEM_DC[3] = (Bit [11]) Mono/stereo select. 0 = Mono. 1 = Stereo. MODEM_DC[2:0] Destination ID select. Bit 10 Bit 9 Bit 8 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Modem input 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
7:4	DS_DC	DirectSound_DC[3] = (Bit [7]) Mono/stereo select. 0 = Mono. 1 = Stereo. DirectSound_DC[2:0] Destination ID select. Bit 6 Bit 5 Bit 4 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Modem input 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
3:0	ASSP_DC	ASSP_DC[3] = (Bit [3]) Mono/stereo select. 0 = Mono. 1 = Stereo. ASSP_DC[2:0] Destination ID select. Bit 2 Bit 1 Bit 0 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Modem input 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved

Ring Bus Destination Control Format (Maestro2_Base+36h,+37h, R/W)

I²S/CHI	R	ER	ES	AR	IDP	IDR	R	MIC_DC				Reserved			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	I²S/CHI	I²S input and DSP serial bus enable. 0 = Disable I²S input and DSP serial bus. 1 = Enable I²S input and DSP serial bus.
14	–	Reserved.
13	ER	EN_RING. Ring bus enable. 0 = Disable ring bus. 1 = Enable ring bus.
12	ES	Serial AC-link enable. 0 = Disable serial AC-link. 1 = Enable serial AC-link.
11	AR	AC'97 software reset. 0 = Disable AC97 software reset. 1 = Enable AC97 software reset.
10	IDP	IO DMA playback enable. 0 = Disable playback of IO DMA. 1 = Enable playback of IO DMA.
9	IDR	IO DMA record enable. 0 = Disable recording of IO DMA. 1 = Enable recording of IO DMA.
8	–	Reserved.
7:4	MIC_DC	MIC_DC[3] = (Bit [7]) Mono/stereo select. 0 = Mono. 1 = Stereo. MIC_DC[2:0] Destination ID select. Bit 6 Bit 5 Bit 4 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Modem input 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
3:0	–	Reserved.

GPIO Data (Maestro2_Base+60h, +61h, R/W)

Reserved	GPIO data
15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11:0	GPD	GPIO data. Data input or output is controlled by the GPIO Direction register (Maestro2_Base+68h, +69h). During input the data acts as a polarity control, combining with the external input signal to the internal circuits.

GPIO Mask (Maestro2_Base+64h, +65h, R/W)

Reserved	GPIO write mask
15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11:0	GPWM	GPIO write mask. 1 = Mask write. 0 = Unmask write.

GPIO Direction (Maestro2_Base+68h, +69h, R/W)

Reserved	GPIO direction
15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11:0	GPD	GPIO direction. 1 = Output. 0 = Input (default).

ASSP Memory / Index Port (Maestro2_Base+80h,+81h, R/W)

ASSP memory/index
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	AM/I	Host-to-ASSP 16-bit memory index port. Points to 64K word of ASSP memory.

ASSP Memory Port (Maestro2_Base+82h,+83h, R/W)

ADT	Reserved	MSS
15	14 13 12 11 10 9 8 7 6 5 4 3 2	1 0

Bit Definitions:

Bits	Name	Description
15	ADT	Aggressive DMA timing. 1 = Enable aggressive DMA timing. 0 = Disable aggressive DMA timing.
14:2	–	Reserved.
1:0	MSS	DMA memory space selection. Bit 1 / Bit 0 / Memory Space 0 x Reserved 1 0 ASSP program memory 1 1 ASSP data memory

ASSP Data Port (Maestro2_Base+84h,+85h, R/W)

ASSP data
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Each time this register is accessed for a read or write, the ASSP Memory/Index port (Maestro2_Base+80h, +81h) is incremented by 1. The index port is 4K word paged and consecutive access cannot cross this 4K word boundary.

Bit Definitions:

Bits	Name	Description
15:0	AD	16-bit data (word) port.

ASSP Control A (Maestro2_Base+A2h, R/W)

Reserved	36CLK	Reserved	FPLU	33/49CLK	Reserved	0WS
7	6	5	4	3	2	1 0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	36CLK	36 MHz DSP clock select. 1 = Select 36 MHz DSP clock. **NOTE:** You must enable bits [31:30] (enable internal clock multiplier) before enabling this bit.
5	–	Reserved.
4	FPLU	Fast PLU enable. 1 = Enable fast PLU. 0 = Disable fast PLU.
3	33/49 CLK	33 MHz or 49 MHz ASSP clock select. 1 = Enable 49.152 MHz ASSP clock. 0 = Enable 33 MHz ASSP clock.
2:1	–	Reserved.
0	0WS	ASSP 0-wait state enable. 1 = Enable ASSP 0-wait state. 0 = Disable ASSP 0-wait state.

ASSP Control B (Maestro2_Base+A4h, R/W)

Reserved			CRE	Reserved			ARST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	–	Reserved.
4	CRE	Clock run/enable. 1 = Stop ASSP clock. 0 = Enable ASSP clock.
3:1	–	Reserved.
0	ARST	ASSP reset/run. 1 = Run ASSP. 0 = Reset ASSP.

ASSP Control C (Maestro2_Base+A6h, R/W)

Reserved				HWP	Reserved		AHI
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	–	Reserved.
3	HWP	Host write port enable. 0 = Disable host write port. 1 = Enable host write port.
2:1	–	Reserved.
0	AHI	ASSP-to-host interrupt request enable. 0 = Disable ASSP-to-host IRQ. 1 = Enable ASSP-to-host IRQ.

Host Write Index (Maestro2_Base+A8h, R/W)

HWIR[7:0]							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HWIR[7:0]	Host write index register. An interrupt to ASSP is deasserted when the host writes this index port.

Host Write Data (Maestro2_Base+AAh, R/W)

HWDR[7:0]							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HWDR[7:0]	Host write data register. An interrupt to ASSP is generated when the host writes this data port.

ASSP to Host IRQ Status (Maestro2_Base+ACh, R/W)

ASSP IRQ status							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	AIS	ASSP to host software interrupt request status. Read for pending interrupt status. 1 = Interrupt pending. 0 = No interrupt pending. Write 1 to clear pending interrupt request. The bits in this register are set to 1 by ASSP to request interrupts from the host. A read checks the status of the interrupt. Writing 1 clears a pending request by the host only.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
DC power voltage	VDD	-0.3 to VDD+0.3	V
Input voltage	VIN	-0.3 to VDD+0.3	V
Operating temperature range	TO	0 to 70	Deg C
Storage temperature range	TST	-40 to 125	Deg C
Maximum power dissipation at TJ = 125 °C	PDMAX	300	mW

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Operating Conditions

DVdd	3.3 V ± 10%
TA	25°
External Load	50 pF

Table 12 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit (conditions)
Input low voltage	VIL	-0.5	–	0.8	V
Input high voltage	VIH	2.0	–	DVdd + 0.5	V
Output high voltage	VOH	2.4	–	DVdd	V
Output low voltage	VOL	0.0	0.2	0.4	V
Input leakage current	–	-10	–	10	µA
Output leakage current	–	-10	–	10	µA
Output buffer drive current	–	–	5	–	mA

POWER MANAGEMENT CHARACTERISTICS

Table 13 Current Consumption

Operating Mode	Typical IDDD at 3.3 V	Power Consumption: (IDDD x 3.3 V) Watt
Fully on	75 mA	0.248 W
ASSP clock stopped [a]	55 mA	0.182 W
Every module is clock-stopped except the PCI interface module	4 mA	0.013 W
Every module is clock-stopped and the PCI interface is stopped via CLKRUN#	700 µA	0.002 W

a. ASSP is responsible for FM hardware emulation and digital-filtering algorithm. The clock is controlled by the driver and could be dynamically stopped and resumed, depending on if the ASSP is in use.

TIMING SPECIFICATIONS

AC-Link Timing Specifications

AC-Link Timing Diagrams

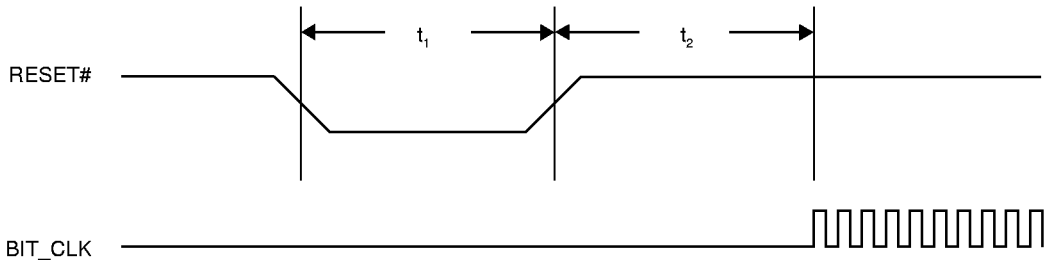


Figure 8 Cold Reset

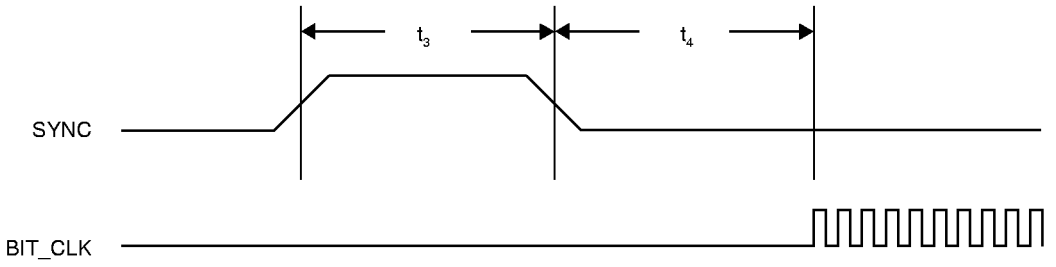


Figure 9 Warm Reset

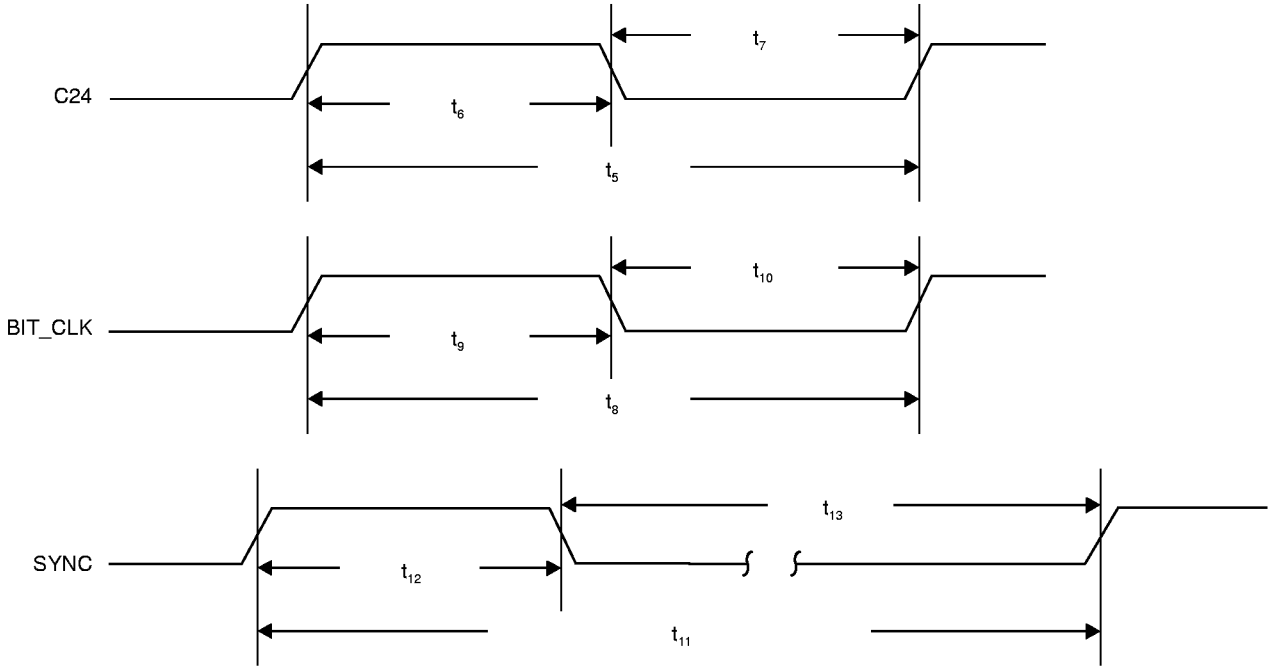


Figure 10 Clocks

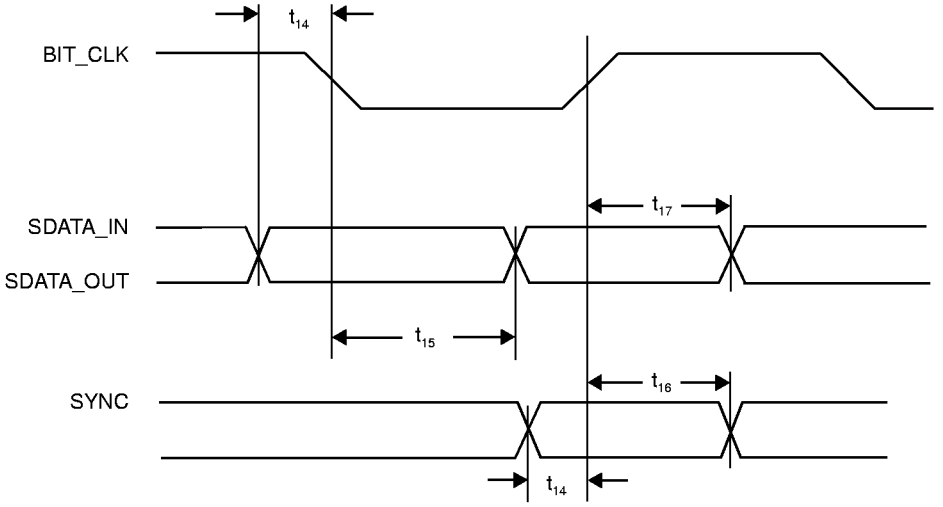


Figure 11 Data Setup and Hold

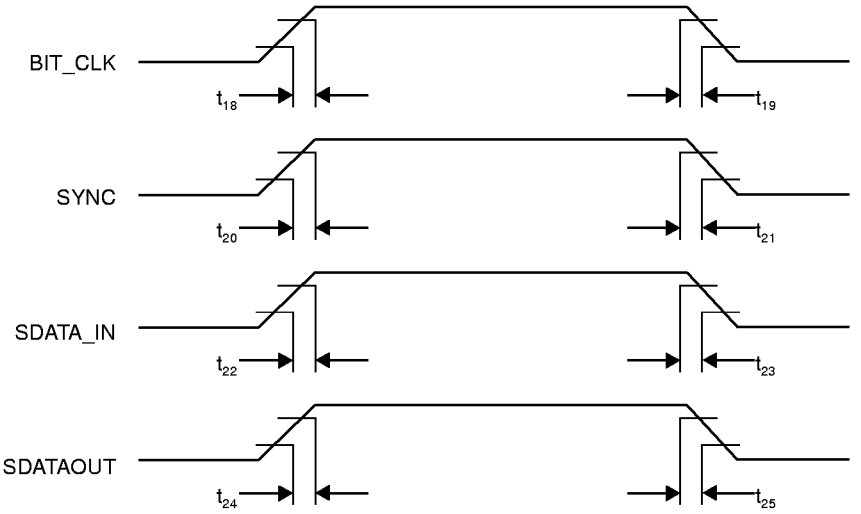
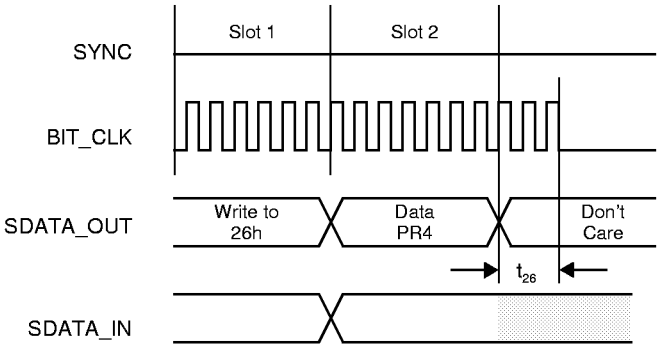


Figure 12 Signal Rise and Fall Times



Note: BIT_CLK not to scale.

Figure 13 AC-Link Low Power Mode Timing

AC-Link Timing Characteristics

Table 14 AC-Link Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_1	RESET# active-low pulse width	1.0			µS
t_2	RESET# inactive to BIT_CLK start-up delay	162.8			nS
t_3	SYNC active-high pulse width		1.3		µS
t_4	SYNC inactive to BIT_CLK start-up delay	162.8			nS
	C24 frequency		25.0		MHz
t_5	C24 period		40.0		nS
t_6	C24 high pulse width	20.41	20.72	21.03	nS
t_7	C24 low pulse width	18.97	19.28	19.59	nS
	BIT_CLK frequency		12.5		MHz
t_8	BIT_CLK period		80.0		nS
t_9	BIT_CLK high pulse width	32.0	40.0	48.0	nS
t_{10}	BIT_CLK low pulse width	32.0	40.0	48.0	nS
	SYNC frequency		48.8		KHz
t_{11}	SYNC period		20.49		µS
t_{12}	SYNC high pulse width		1.28		µS
t_{13}	SYNC low pulse width		19.21		µS
t_{14}	Setup to falling edge of BIT_CLK	15.0			nS
t_{15}	Hold from falling edge of BIT_CLK	5.0			nS
t_{16}	Valid delay from BIT_CLK rising edge	4		10	nS
t_{17}	Valid delay from BIT_CLK rising edge	4		10	nS
t_{18}	BIT_CLK rise time	2		6	nS
t_{19}	BIT_CLK fall time	2		6	nS
t_{20}	SYNC rise time	2		6	nS
t_{21}	SYNC fall time	2		6	nS
t_{22}	SDATA_IN rise time	2		6	nS
t_{23}	SDATA_IN fall time	2		6	nS
t_{24}	SDATA_OUT rise time	2		6	nS
t_{25}	SDATA_OUT fall time	2		6	nS
t_{26}	End of Slot 2 to BIT_CLK, SDATA_IN low			1.0	µS

PCI Bus Timing Specifications

PCI Bus Timing Diagrams

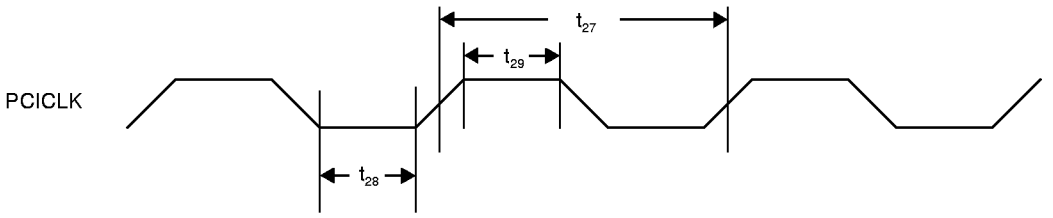


Figure 14 PCI Clock Timing

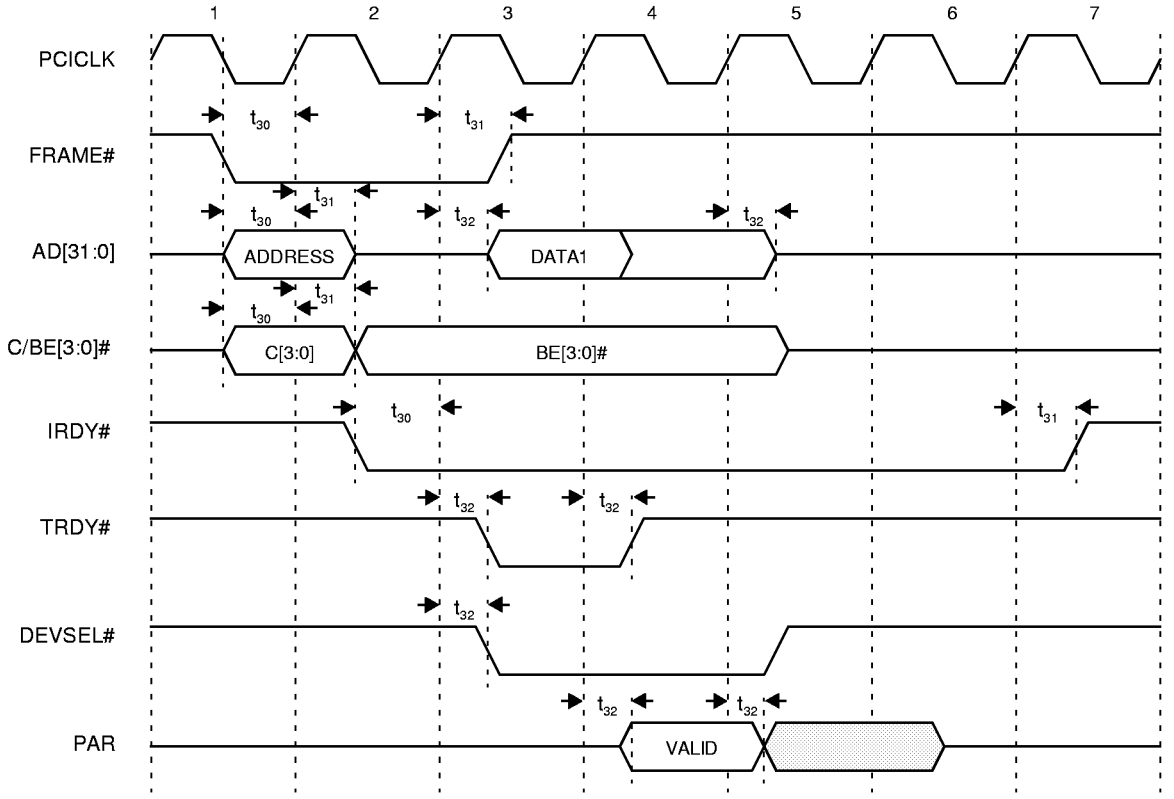


Figure 15 PCI Bus I/O Read Cycle

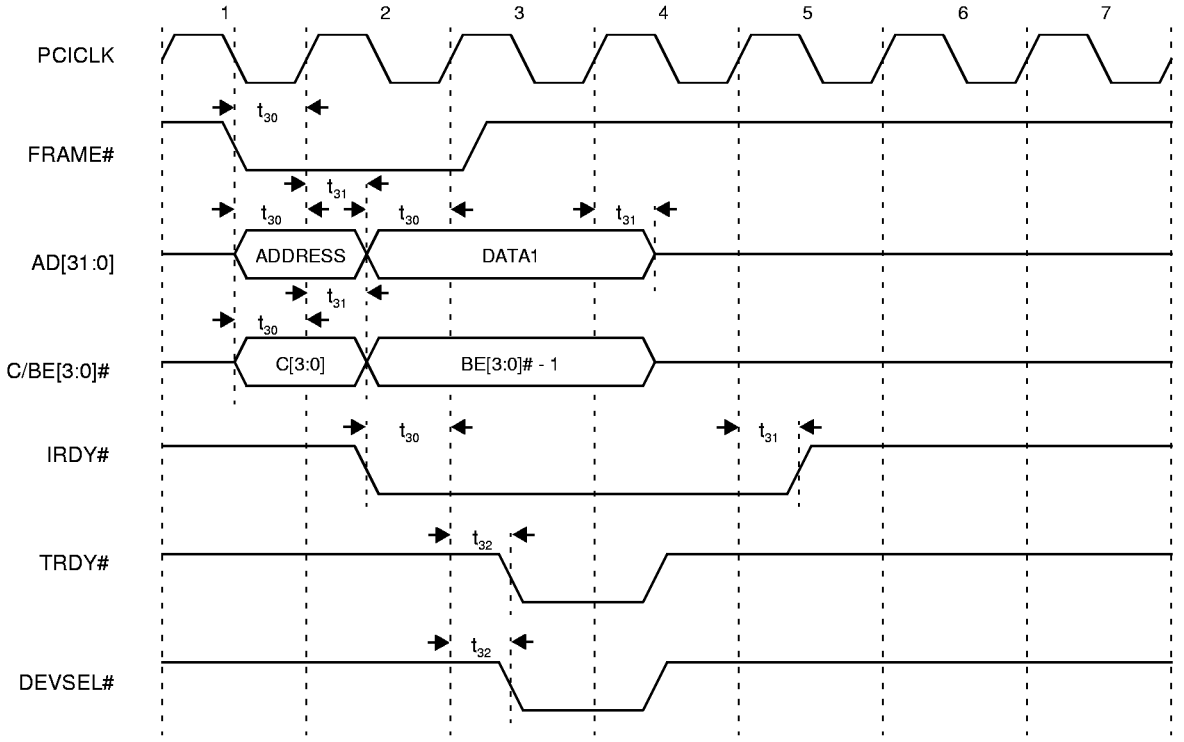


Figure 16 PCI Bus I/O Write Cycle

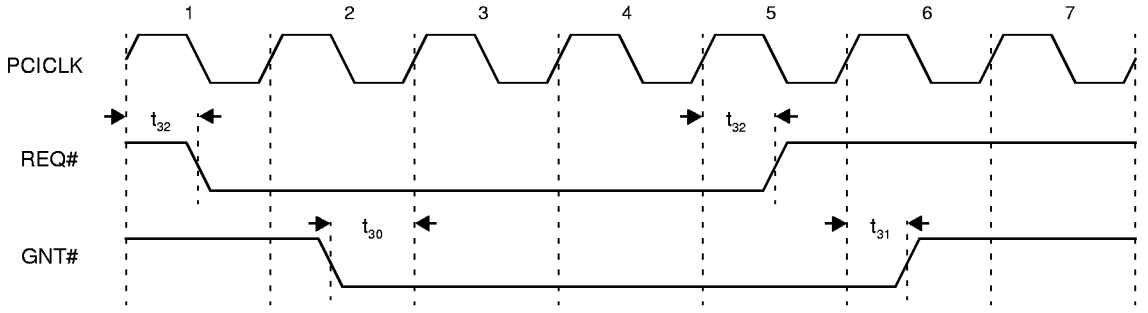


Figure 17 PCI Bus Master Request

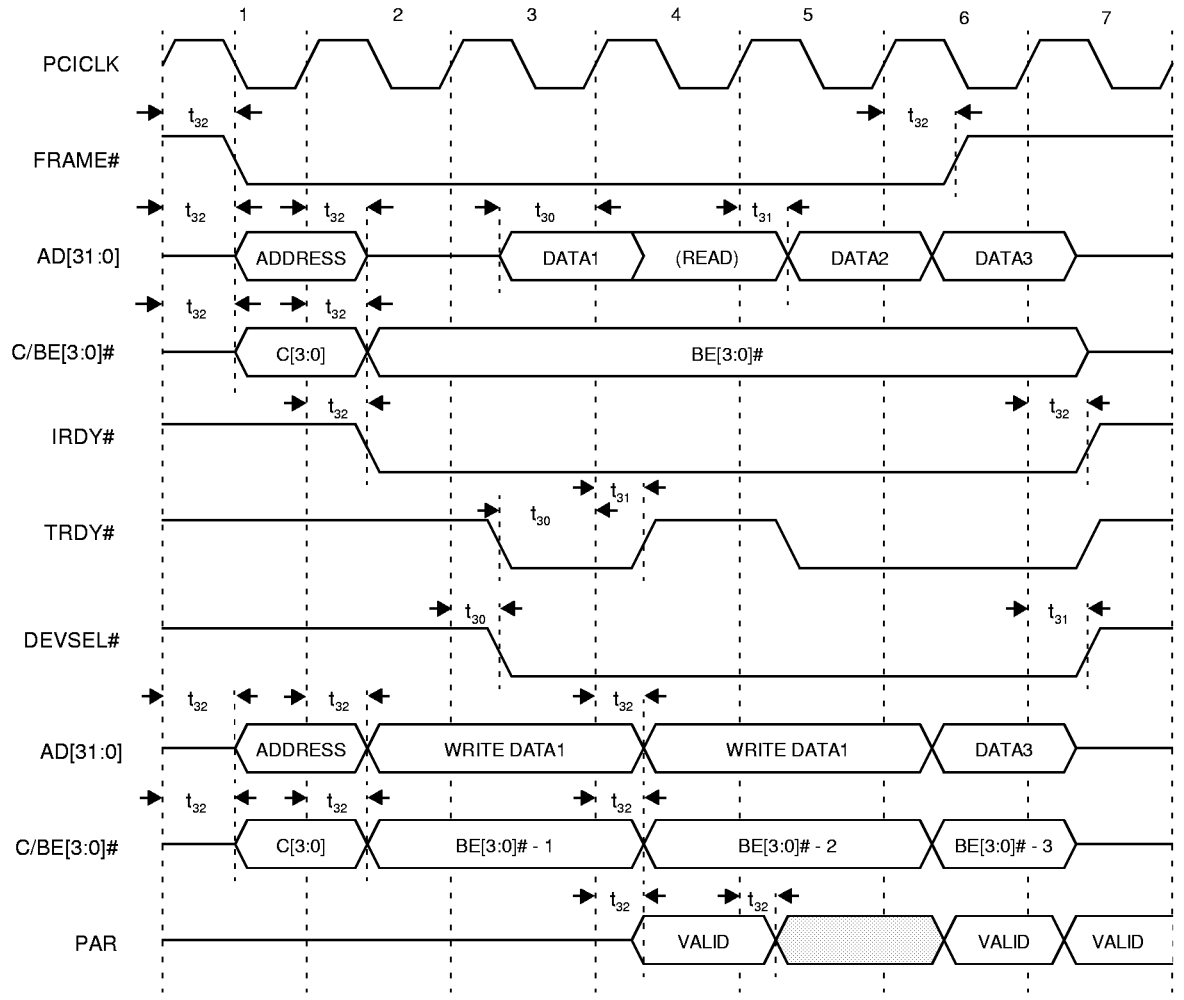


Figure 18 PCI Bus Master Read/Write Cycle

PCI Bus Timing Characteristics

Table 15 PCI Bus Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units (Conditions)
t_{27}	PCI bus clock cycle time	30			nS
t_{28}	PCI bus clock low pulse width	11			nS
t_{29}	PCI bus clock high pulse width	11			nS
t_{30}	Input setup time to PCICLK	7			nS
t_{31}	Input hold time to PCICLK	0			nS
t_{32}	Output propagation delay Time from PCICLK	2		11	nS (0 pF load) (50 pF load)

I²S Port Timing Specifications

I²S Port Timing Diagrams

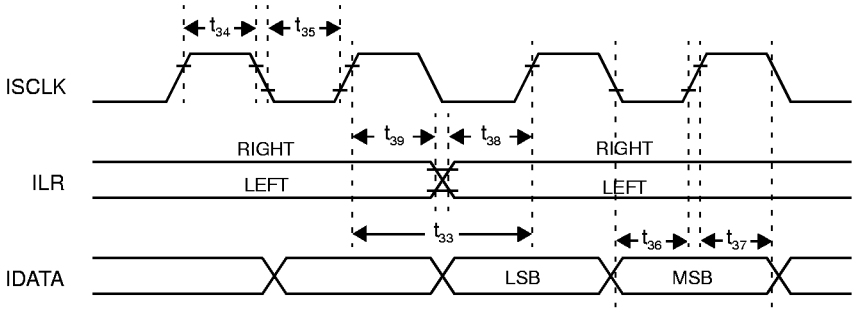


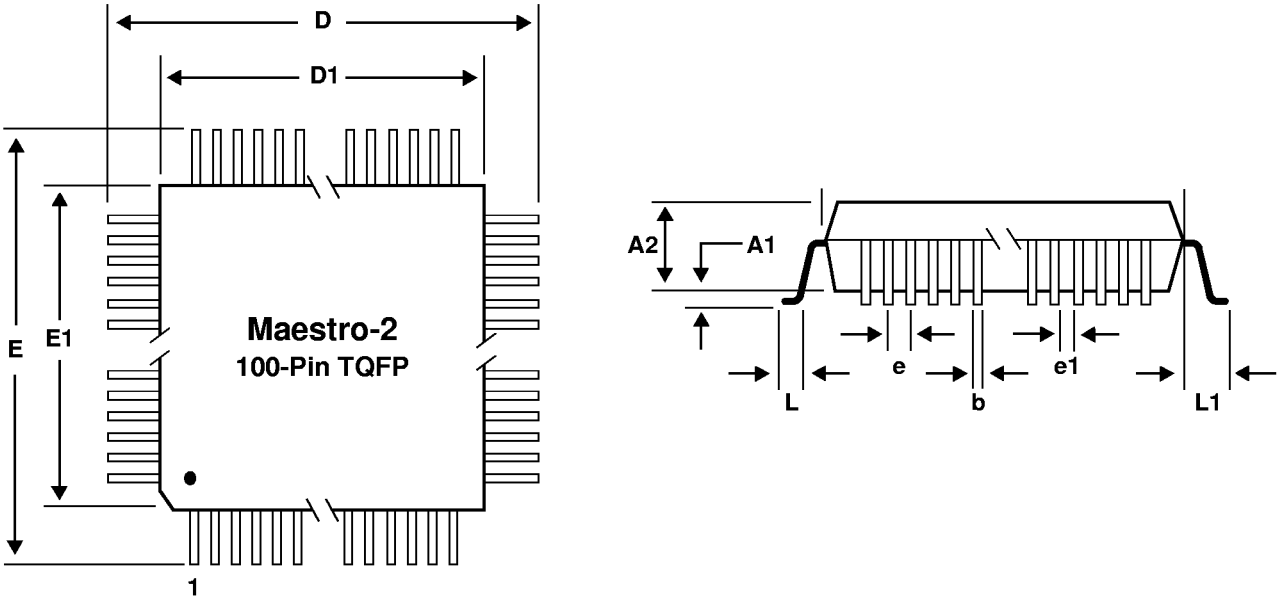
Figure 19 I²S Port Timing

I²S Port Timing Characteristics

Table 16 I²S Port Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{33}	ISCLK cycle time	54			nS
t_{34}	ISCLK HIGH time	15			nS
t_{35}	ISCLK LOW time	15			nS
t_{36}	IDATA setup time	12			nS
t_{37}	IDATA hold time	2			nS
t_{38}	ILR setup time	12			nS
t_{39}	ILR hold time	2			nS

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 20 Maestro-2 Mechanical Dimensions

APPENDIX A: SCHEMATIC EXAMPLES

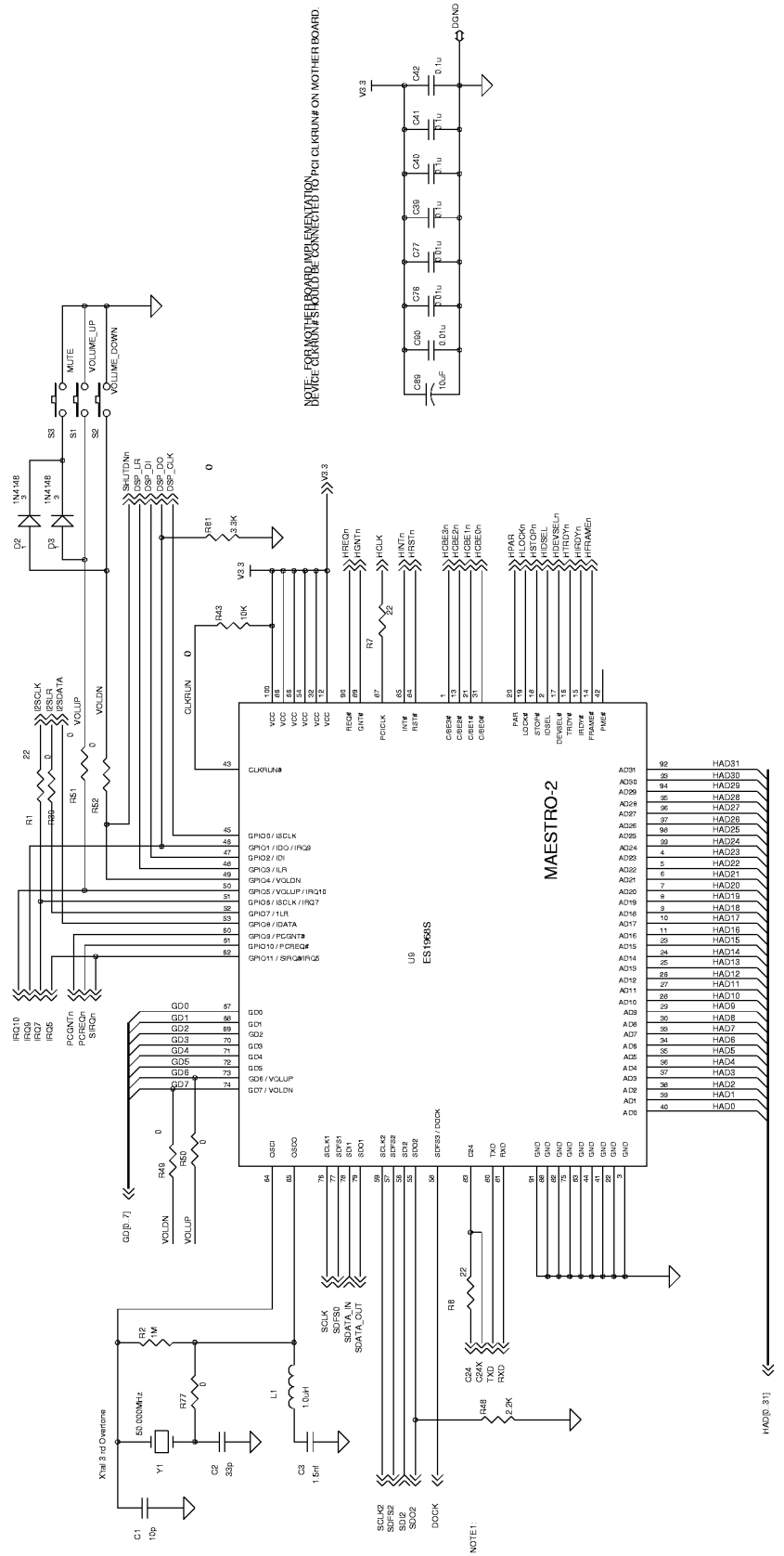


Figure 21 Maestro-2 Schematic

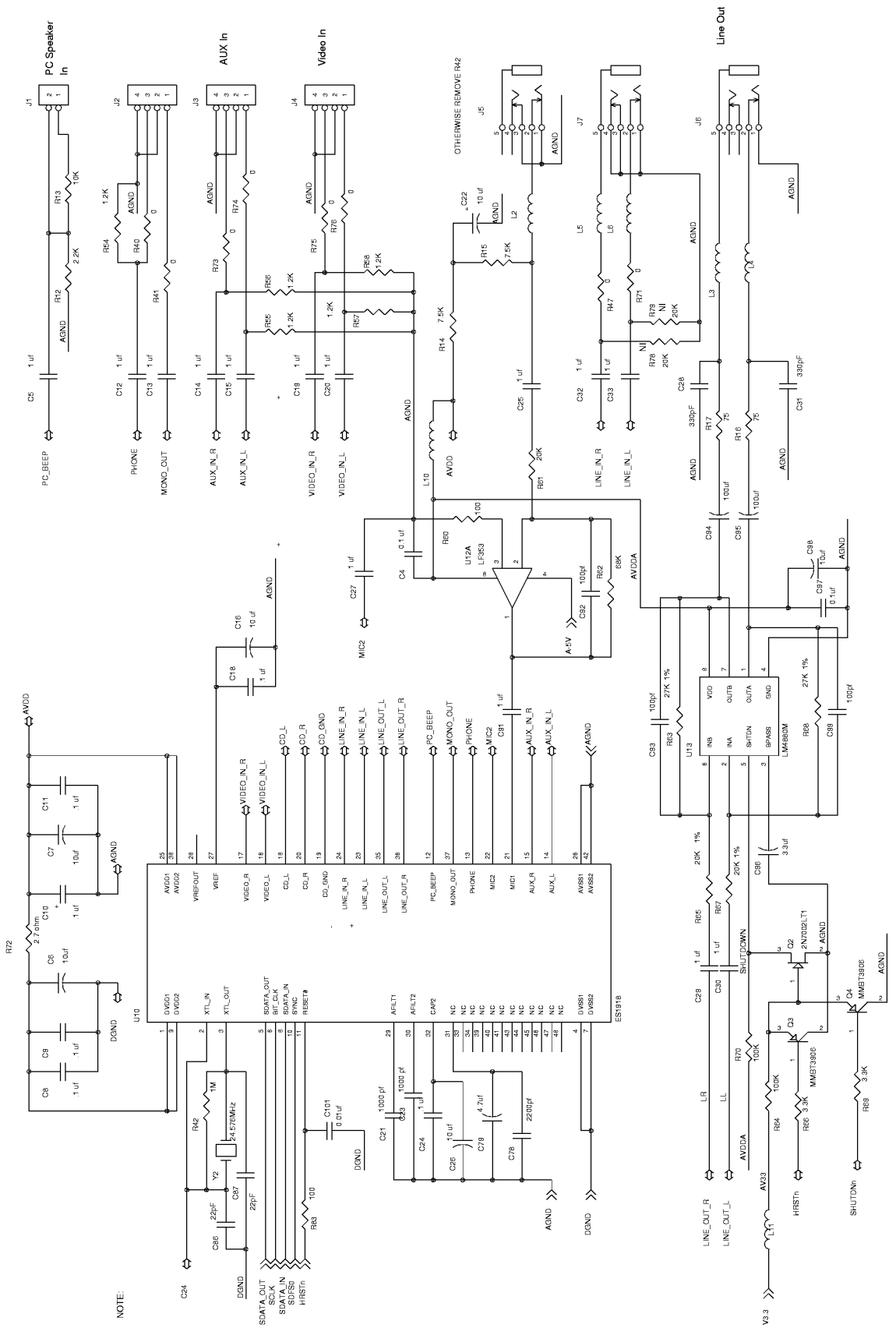


Figure 22 CODEC Interface

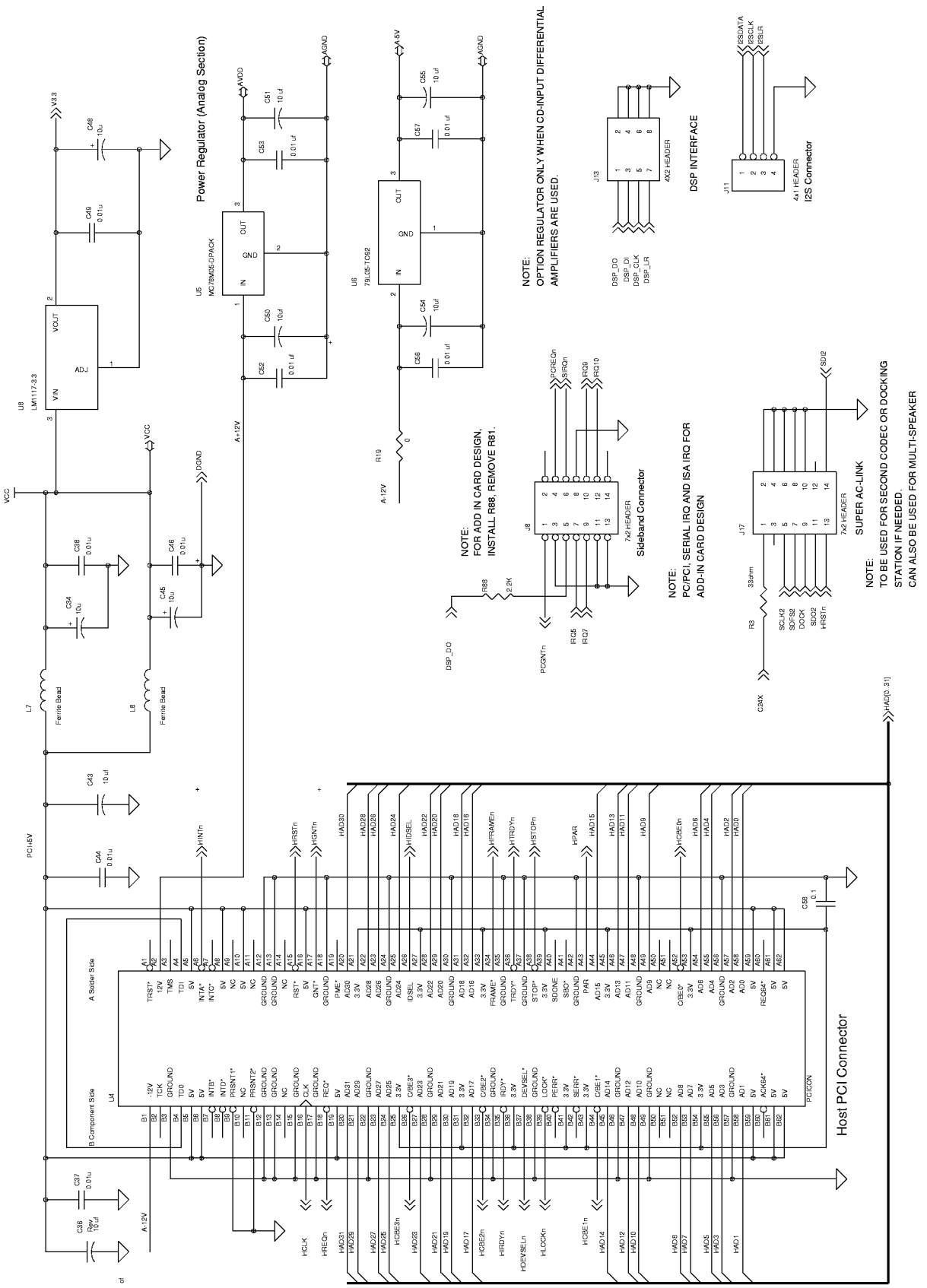


Figure 23 Host PCI Interface

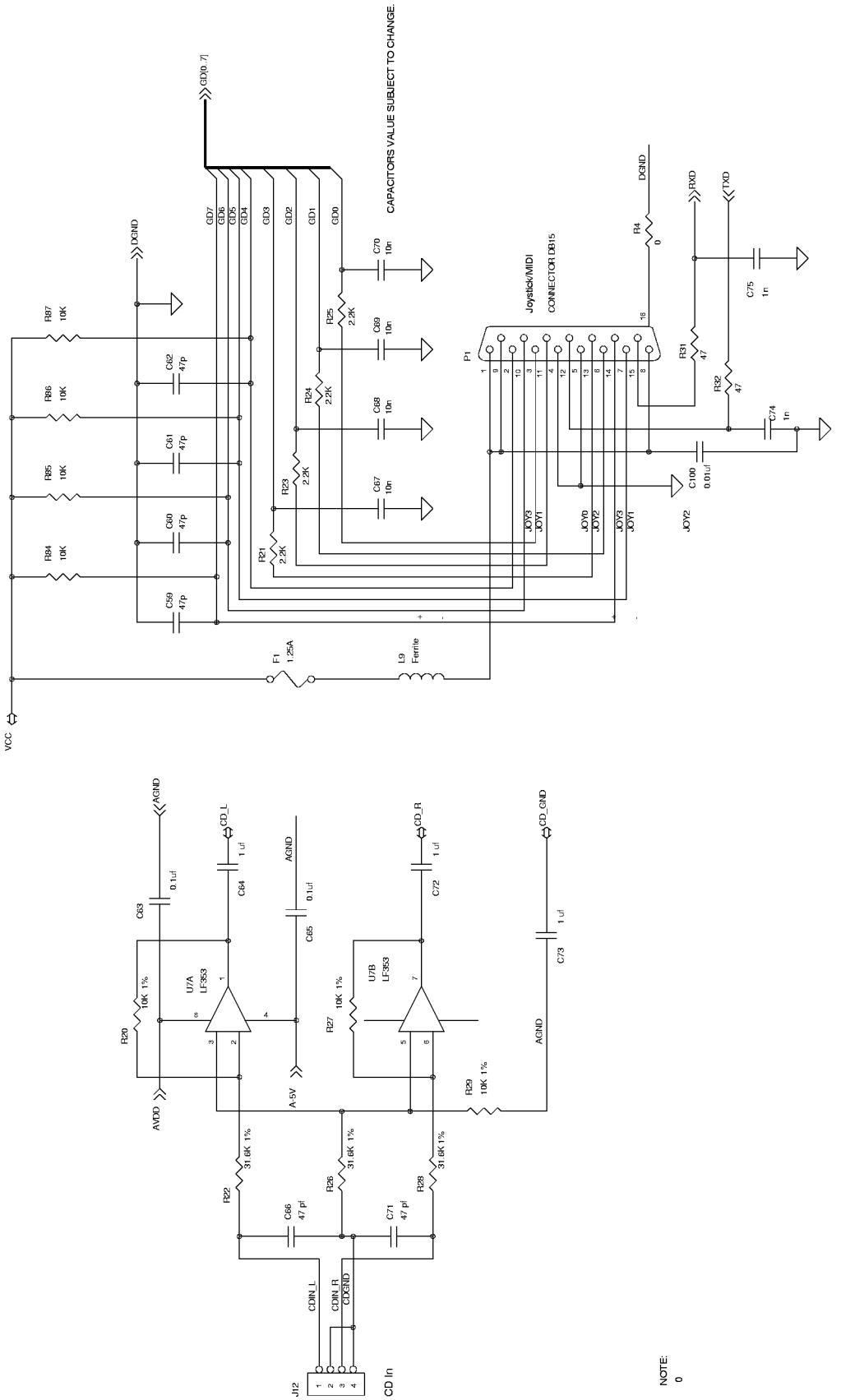


Figure 24 CD/MIDI Section

APPENDIX B: BILL OF MATERIALS

Table 17 Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	1	C1	CAP, SMT 0805, 5%, 10 p
2	1	C2	CAP, SMT 0805, 10%, 25 V, 33 p
3	1	C3	CAP, SMT 0805, 10%, 25 V, 1500 pf
4	17	C5,C12,C13,C14,C15,C19,C20,C25,C27, C29, C30,C32,C33,C64,C72,C73,C91	CAP, SMT 0805, 10%, 25 V, 1 µf
5	16	C6,C7,C50,C54,C89,C98,C16,C22,C26, C36,C43,C51,C55,C34,C45,C48	CAP, TANT B SIZE, 20%, 16 V, 10 µf
6	2	C21,C23	CAP, SMT 0805, 10%, 25 V, 1000 pf
7	2	C28,C31	CAP, SMT 0805, 10%, 330 pF
8	17	C37,C38,C44,C46,C49,C76,C67,C68, C69,C70,C100,C77,C90,C52,C53,C56, C57	CAP, SMT 0805, 10%, 25 V, 0.01 µf
9	15	C8,C9,C10,C11,C18,C24,C39,C40,C41, C42,C58,C63,C65,C97,C4 R8	CAP, SMT 0805, 10%, 25 V, 0.1 µf install R8 with 0.1 µf cap when using 5 V CODEC
10	6	C59,C60,C61,C62,C66,C71	CAP, SMT 0805, 10%, 25 V, 47 pf
11	2	C74,C75	CAP, SMT 0805, 10%, 25 V, 1000 pf
12	1	C78	CAP, SMT 0805, 10%, 25 V, 2200 pf
13	1	C79	CAP, TANT, B SIZE, 20%,10 V, 4.7 µf
14	3	C92,C93,C99	CAP, SMT 0805, 10%, 25 V, 100 pf
15	2	C94,C95	CAP, ELECT. 16 V, 20%, 100 µf
16	1	C96	CAP, TANT, B SIZE, 20%,10 V,3.3 µf
17	1	C101	CAP, SMT 0805, 10%, 25 V, 0.33 µf
18	2	D3,D2	DIODE, SOT-23, 1N4148
19	1	F1	FUSE, 1.25 A, SMD, 1210
20	1	J1	HEADER 2X1
21	4	J2,J3,J4,J12	CONNECTOR 4X1
22	3	J5,J6,J7	PHONEJACK STEREO, 3.5 mm
23	2	J8,J17	7x2 HEADER
24	1	J11	4x1 HEADER
25	1	J13	4X2 HEADER
26	1	L1	INDUCTOR, SMT, 1210, 1.0 µH
27	5	L2,L3,L4,L5,L6	FERRITE BEAD, SMT, 0805
28	5	L7,L8,L9,L10,L11	FERRITE BEAD, SMT, 1206
29	1	P1	CONNECTOR DB15
30	1	Q2	N CHANNEL FET, SOT-23, 2N7002LT1
31	3	Q3,Q4	TRANSISTOR, SOT-23, MMBT3906
32	4	R1,R3,R7,R8	RESISTOR, SMT, 0805, 5%, 1/10 W, 22 ohm; replace R8=22 ohm with 0.1 µf cap when using 5 V CODEC like AKM.
33	1	R2	RESISTOR, SMT, 0805, 5%, 1/10 W, 1 M
34	7	R12,R21,R23,R24,R25,R48,R88	RESISTOR, SMT, 0805, 5%, 1/10 W, 2.2 K
35	6	R13,R43,R84,R85,R86,R87	RESISTOR, SMT, 0805, 5%, 1/10 W, 10 K

Table 17 Bill of Materials (BOM) (Continued)

Item	Quantity	Reference	Part
36	2	R14,R15	RESISTOR, SMT, 0805, 5%, 1/10 W, 7.5 K
37	2	R17,R16	RESISTOR, SMT, 0805, 5%, 1/10 W, 75 ohm
38	14	R19,R39,R40,R41,R47,R51,R52,R71, R73,R74,R75,R76,R77,R4	RESISTOR, SMT, 0805, 5%, 1/10 W, 0 ohm
39	3	R20,R27,R29	RESISTOR, SMT, 0805, 1%, 1/10 W, 10 K
40	2	R65,R67	RESISTOR, SMT, 0805, 1%, 1/10 W, 20 K
41	3	R22,R26,R28	RESISTOR, SMT, 0805, 1%, 1/10 W, 31.6 K
42	2	R32,R31	RESISTOR, SMT, 0805, 5%, 1/10 W, 47 ohm
43	5	R54,R55,R56,R57,R58	RESISTOR, SMT, 0805, 5%, 1/10 W, 1.2 K
44	2	R60,R83	RESISTOR, SMT, 0805, 5%, 1/10 W, 100
45	3	R61,R78,R79	RESISTOR, SMT, 0805, 5%, 1/10 W, 20 K
46	1	R62	RESISTOR, SMT, 0805, 5%, 1/10 W, 68 K
47	2	R68,R63	RESISTOR, SMT, 0805, 1%, 1/10 W, 27 K
48	2	R64,R70	RESISTOR, SMT, 0805, 5%, 1/10 W, 100 K
49	4	R66,R69	RESISTOR, SMT, 0805, 5%, 1/10 W, 3.3 K
50	1	R72	RESISTOR, SMT, 1206, 5%, 1/10 W, 2.7 ohm
51	3	S1,S2,S3	PUSH BUTTON
52	1	U5	REGULATOR, MC78M05-DPACK
53	1	U6	REGULATOR, 79L05-TO92
54	2	U12,U7	AMPLIFIER, SO8, LF353
55	1	U8	REGULATOR, SOT-223, LT1117-3.3
56	1	U9	MAESTRO-2, TQFP, ES1968S
57	1	U10	AC'97 CODEC, TQFP, ES1918
58	1	U13	HEADPHONE DRIVE, SO8, LM4880M
59	1	Y1	XTAL, 50-100 ppm, 18 pf, 50.000 MHz