C-MEDIA ELECTRONICS INC.

PRELIMINARY
Ver. 0.1

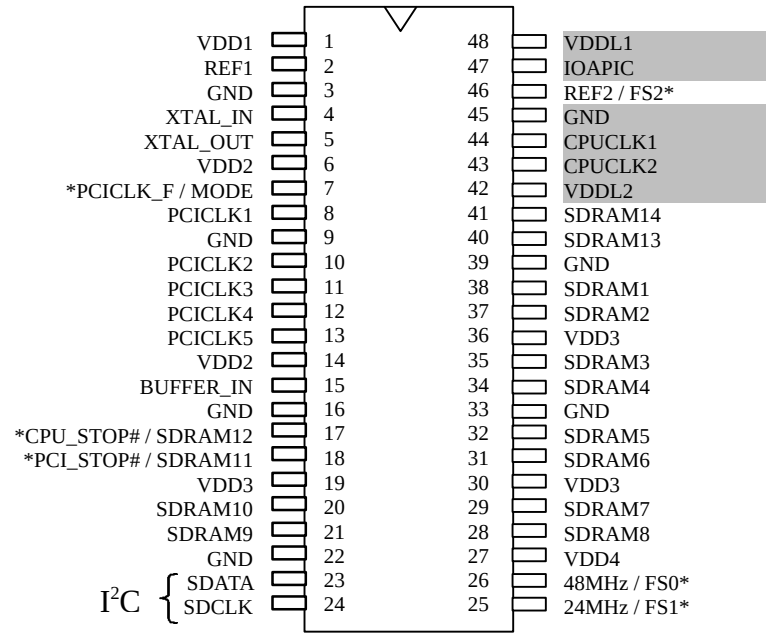
6F, No. 100, Sec. 4, Civil Boulevard, Taipei, Taiwan
TEL: (02)8773-1100 FAX: 886-2-8773-2211
www:http://cmedia.com.tw

CMA8864BF-26B (3 DIMM) — I²C, Mixed Voltage clock Synthesizer with Buffer for PENTIUM™ & II CPU/PCI, AGP system

FEATURES

- **Supports Pentium II/PRO CPUs, Intel BX motherboard chipset.**
- **Two (2) copies of CPUCLK clock powered with VDDL2.**
- **Fourteen (14) SDRAM clocks powered by VDD3. <5ns propagation delay from BUFFER_IN.**
- **Six (6) copies of PCI clock (1/2 CPU clock or asynchronous 2/5, 1/3 CPU clock).**
- **24/48 MHz outputs (3.3V TTL)**
- **Two Ref. Clock @ 14.318MHz (3.3V TTL), One IOAPIC powered by VDDL1.**
- **60mA buffer switching current @3.3V.**
- **CPU clocks lead PCI clocks 1-4 ns.**
- **Optional common or mixed power supply mode**
  - ✧ **VDD1, 2, 3 = 3.3V**
  - ✧ **VDDL1, 2 = 2.5V**
- **< 250ps skew between CPU/SDRAM buffers.**
- **<500ps skew between PCI buffers.**
- **Power management controlled by CPU_STOP#, PCI_STOP#.**
- **I²C Serial configuration interface.**
- **48 pins SSOP package.**

PIN CONFIGURATIONS



2.5V

I/O PINS

***Internal pull-up resistor 240Ω to 3.3V on indicated pins.**

POWER GROUPS

VDD1=REF, XTAL_IN, XTAL_OUT, PLL CORE

VDD2=PCICLK

VDD3=SDRAM

VDD4=24/48HMz

VDDL1=IOAPIC

VDDL2=CPUCLK

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PIN DESCRIPTION

NAME	TYPE	NO.	DESCRIPTION
VDD1	P	1	Analog 3.3V power supply for PLL core, REF, XTAL_IN/_OUT.
REF1	O	2	14.318MHz clock output.
GND	G	3, 9, 16, 22, 33, 39, 45	Ground.
XTAL_IN	I	4	Crystal input.
XTAL_OUT	O	5	Crystal output.
VDD2	P	6, 14	3.3V I/O power supply for PCICLK.
PCICLK_F / MODE	I/O	7	PCI clock output free-running, TTL compatible 3.3V. /Mode selection, latched input, internal pull-high.
			MODE=1 / PIN#17=SDRAM12 / PIN#18=SDRAM11
			MODE=0 / PIN#17=CPU_STOP# / PIN#18=SPCI_STOP#
PCICLK1-5	O	8, 10, 11, 12, 13	PCI clock output TTL compatible 3.3V.
BUFFER_IN	I	15	Input from fan-out buffers for SDRAM input.
SDRAM12 / CPU_STOP#	O	17	SDRAM clock output, powered by VDD3. / halts CPUCLK at logic 0 level when input low, MODE=0 (Mobil mode)
SDRAM11 /PCI_STOP#	O	18	SDRAM clock output, powered by VDD3. / halts PCICLK at logic 0 level when input low, MODE=0 (Mobil mode)
SDRAM13, 14, 10-1	O	20, 21, 28, 29, 31, 32, 34, 35, 37, 38, 40, 41	SDRAM clock output, powered by VDD3.
VDD3	P	19, 30, 36	3.3V I/O power supply for SDRAM.
SDATA	I	23	Data input pin for I^2C bus.
SDCLK	I	24	Clock input pin for I^2C bus.
24MHz / FS1	I/O	25	24MHz clock output 3.3V. / Frequency select pin, latched input, internal pull-High.
48MHz / FS0	I/O	26	48MHz clock output 3.3V. / Frequency select pin, latched input, internal pull-High.
VDD4	P	27	3.3V I/O power supply for 24/48MHz.
VDDL2	P	42	2.5V I/O power supply for CPUCLK.
CPUCLK1, 2	O	43, 44	CPU and Host clock output, powered by VDDL2.
REF2 / FS2	I/O	46	14.318MHz clock output. / Frequency select pin, latched input, internal pull-High.
IOAPIC	O	47	14.318MHz clock output 2.5V, powered by VDDL1
VDDL1	P	48	2.5V I/O power supply for IOAPIC.

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CPU CLOCK FREQUENCY TABLE (in MHz)

SEL2	SEL1	SEL0	CPUCLK	PCICLK	REF, IOAPIC
1	1	1	100.2	33.4 (1/3 CPU)	14.318
1	1	0	133	33.3 (1/4 CPU)	14.318
1	0	1	112	37.3 (1/3 CPU)	14.318
1	0	0	103	34.3 (1/3 CPU)	14.318
0	1	1	66.8	33.4 (1/2 CPU)	14.318
0	1	0	83.3	33.3 (2/5 CPU)	14.318
0	0	1	75	37.5 (1/2 CPU)	14.318
0	0	0	50	25 (1/2 CPU)	14.318

IC SERIAL CONTROL

IC Specification

Address assignment	7 bit									
Transfer type	Slaver / Receiver									
Transfer rate	100kbits/s (standard mode)									
Data byte format	8 bits									
Address format	A6	A5	A4	A3	A2	A1	A0	R/Ws	+8 bits dummy Command Code	+8 bits dummy Command Code
	1	1	0	1	0	0	1	0		
General call	No respond									

SERIAL CONTROL REGISTERS

A) The serial bits will be read in the following order :

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

B) The PIN# column lists the affected pin number where application. The values in the @Pup column gives the state at true power up. Registers are set to the values shown only on the true power up.

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Byte 0 : Function and Frequency Select Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description					
7	--	0	Must be 0 for normal operation.					
			0 -- ¡ Ó5% frequency modulation.					
			1 -- ¡ Ó5% frequency modulation.					
6	--	0	Bit6	Bit5	Bit4	CPU	PCI	REF, IOAPIC
5	--	0	1	1	1	100.2	33.4	14.318
4	--	0	1	1	0	133	33.3	14.318
			1	0	1	112	37.3	14.318
			1	0	0	103	34.3	14.318
			0	1	1	66.8	33.4	14.318
			0	1	0	83.3	33.3	14.318
			0	0	1	75	37.5	14.318
			0	0	0	50	25	14.318
3	--	0	0 -- Frequency is selected by hardware select, latched inputs.					
			1 -- Frequency is selected by Bit 6 : 4.					
2	--	0	Must be 0 for normal operation.					
			0 -- Frequency modulation center spread type.					
			1 -- Frequency modulation down spread type.					
1	--	0	0 -- Normal.					
			1 -- Frequency modulation enabled type.					
0	--	0	0 -- Normal.					
			1 -- Tristate all outputs.					

Byte 1 : CPU Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	26	1	48MHz
6	25	1	24MHz
5		X	Reserved
4		X	Reserved
3	40	1	SDRAM13 (Active/Inactive)
2	41	1	SDRAM14 (Active/Inactive)
1	43	1	CPUCLK2 (Active/Inactive)
0	44	1	CPUCLK1 (Active/Inactive)

Byte 2 : PCI Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	7	1	PCICLK_F (Active/Inactive)
5	--	X	Reserved
4	13	1	PCICLK5 (Active/Inactive)
3	12	1	PCICLK4 (Active/Inactive)
2	11	1	PCICLK3 (Active/Inactive)
1	10	1	PCICLK2 (Active/Inactive)
0	8	1	PCICLK1 (Active/Inactive)

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Byte 3 : SDRAM Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	--	X	Reserved
3	--	X	Reserved
2	21, 20, 18, 17	1	SDRAM(9-12) (Active/Inactive)
1	32, 31, 29, 28	1	SDRAM(5-8) (Active/Inactive)
0	38, 37, 35, 34	1	SDRAM(1-4) (Active/Inactive)

Byte 4 : Additional SDRAM Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	--	X	Reserved
3	--	1	Reserved
2	--	X	Reserved
1	--	X	Reserved
0	--	X	Reserved

Byte 5 : Peripheral Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	47	1	IOAPIC (Active/Inactive)
3	--	X	Reserved
2	--	X	Reserved
1	46	1	REF2 (Active/Inactive)
0	2	1	REF1(Active/Inactive)

Byte 6 : Reserved Optional Register for Future Requirements

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	--	X	Reserved
3	--	X	Reserved
2	--	X	Reserved
1	--	X	Reserved
0	--	X	Reserved

Notes :
1. Inactive means outputs are held LOW and are disable from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

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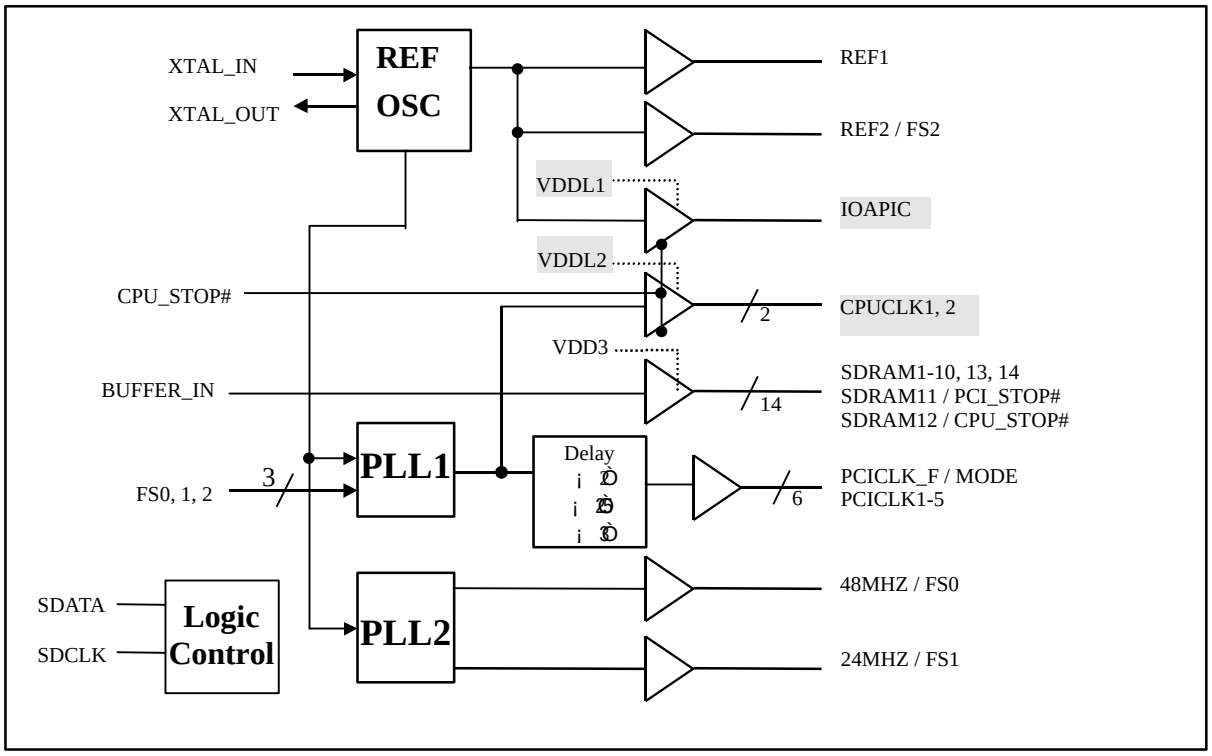
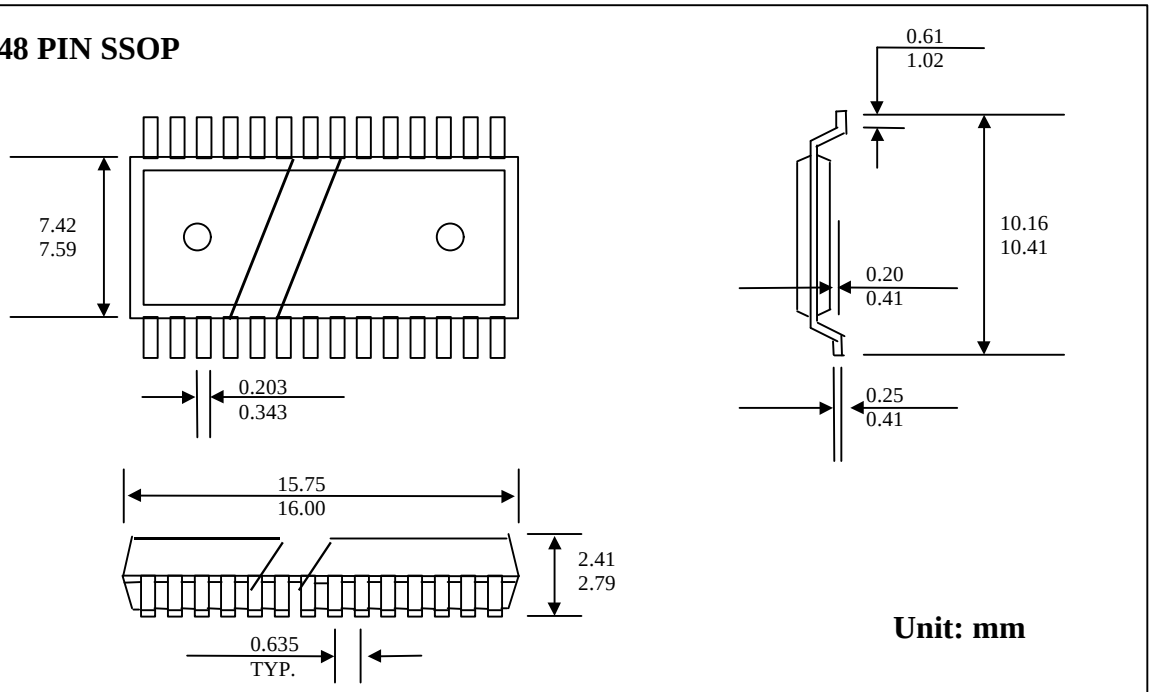
BLOCK DIAGRAM



PACKAGE DIMENSION

48 PIN SSOP



Unit: mm