PRELIMINARY

Am78C201/202

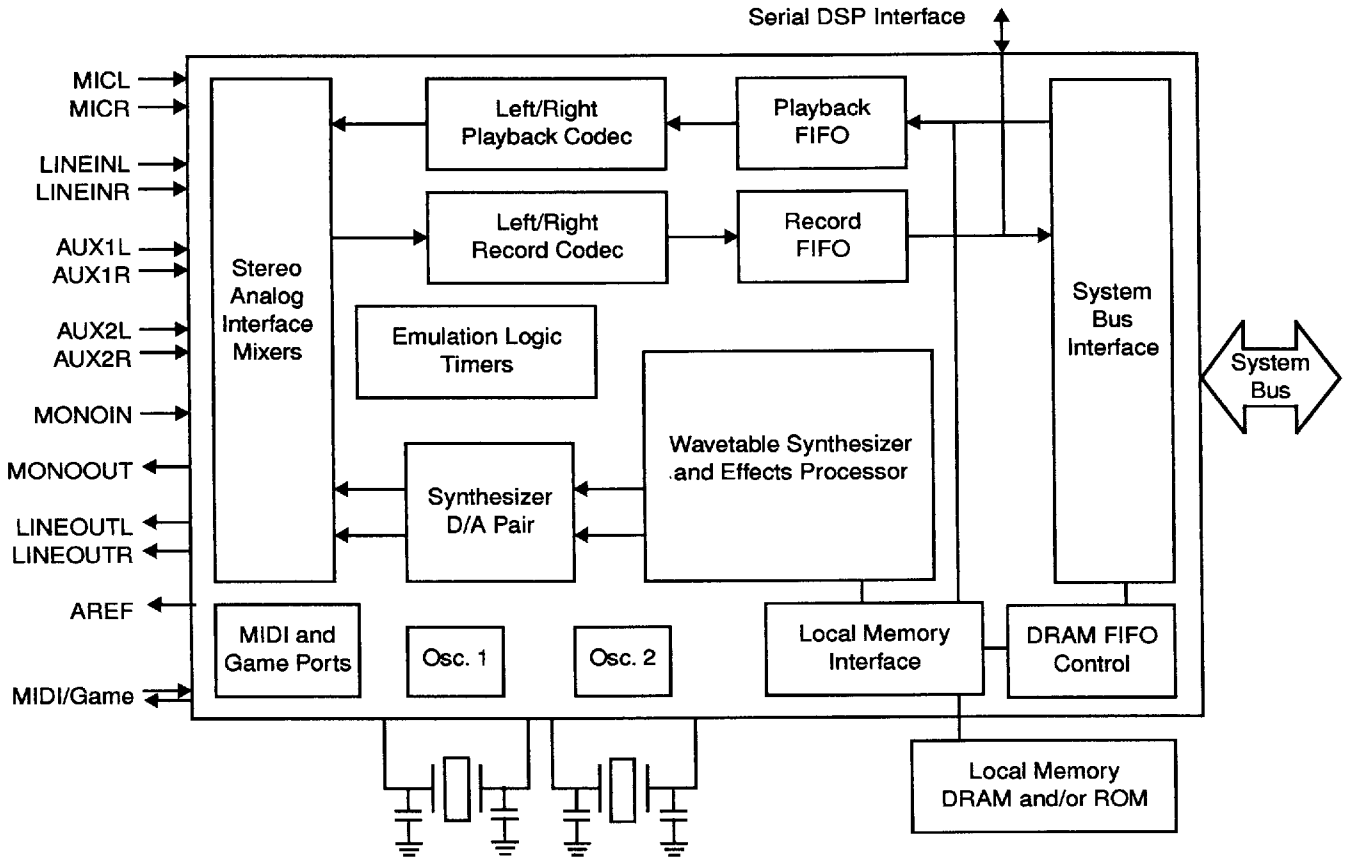
InterWave™ Interactive Audio and Wavetable Solution

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **32-voice stereo wavetable synthesizer**
- **Integrated effects processor**
- **Up to 32 channels of digital mixing**
- **Stereo 16-bit audiophile codec with IMA ADPCM 4:1 compression/decompression**
- **MPC-compliant analog mixer**
- **ISA plug and play (Am78C201)**
- **ISA non-plug and play (Am78C202)**
- **MIDI and game ports**
- **Power management, 3.3 V and 5 V**
- **System expansion through a serial DSP interface**
- **Supports multiple standards:**
  - — Microsoft® Windows®95, DirectSound™
  - — Sound Blaster compatible applications
  - — Windows® Sound System
  - — MPU-401
  - — Windows 3.x API, Win32 API
  - — MT32
  - — General MIDI
  - — Miles AIL API
  - — HMI SOS API
  - — MPC2, MPC3
  - — UltraSound

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The InterWave audio IC provides a complete audio subsystem that meets all major business and entertainment audio standards. The Am78C201 and Am78C202 devices integrate a 32-voice stereo wavetable synthesizer, a 16-bit stereo audiophile codec and audio mixer, both MIDI and game ports, and legacy FM sound card emulation hardware into a single device.

The InterWave IC is available in two versions: The 160-pin Am78C201 device has an ISA Plug and Play interface, while the Am78C202 device is packaged in a 144-pin TQFP, suitable for mounting on a PCMCIA card or a laptop motherboard where Plug and Play is not required.

Analog Interface, Mixers

The Am78C201 device includes stereo analog inputs provided for microphone, line, and, on the Am78C201 device, two auxiliary inputs. These signals are combined with the outputs of the left and right playback codecs to produce the stereo and monaural outputs. The gain of each of these channels is controlled by internal registers, which are loaded through the system bus interface. (The Am78C202 device has only one auxiliary input.)

Playback and Record Codec

The full duplex 16-bit audiophile stereo codec is a register compatible super-set of the CS4231 and AD1848. The codec provides: independently programmable sample rates for the playback and record paths; a variety of data types and compression schemes; on board 16-sample playback and record FIFOs; and a serial port that allows an external DSP engine to connect directly to the record and playback paths.

Wavetable Synthesizer

The wavetable synthesizer offers 32 16-bit stereo voices, all running at a 44.1-kHz frame rate. Each voice supports address generation, envelope generation, tremolo, vibrato, panning, and volume control. Any combination of the 32 synthesizer voices can be used to play or mix digital audio files. Additionally, all of the voice processing power can be used to modify the signals, including volume, pan, frequency shift, reverb, chorus, flanging, echo, tremolo, and vibrato.

The synthesizer includes an on-chip effects processor that provides up to eight channels of reverb, echo, chorus, and flanging capability. Effects can be assigned to individual voices or to any combinations of voices.

The wavetable memory can be either DRAM or ROM, or a combination of the two. When DRAM is used, musical instrument "patches" can be swapped in and out as needed. This swapping allows for a smaller, lower-cost wavetable memory. The IC supports up to 16 Mbytes each of DRAM and ROM. Wavetable patches can be 8-bit, 16-bit, or 8-bit μ-law compressed.

The stereo digital output of the synthesizer is converted into analog form by two on-chip 16-bit digital-to-analog converters (DACs).

Bus Interface

The bus interface of the Am78C201 device is fully compliant with the Plug and Play standard with no external logic. The Plug and Play interface can be either an 8-bit or a 16-bit ISA interface. The IC supports connecting an external device, such as a CD-ROM drive, to the ISA bus through the Plug and Play interface. On the Am78C202 device, the Plug and Play feature is eliminated.

Local Memory Interface

The local memory control module (LMC) transfers data between local memory and the synthesizer, the system bus interface, and the codec. Local memory can include up to four banks of DRAM and up to four banks of ROM. The IC contains support for implementing external FIFOs using DRAM, and for a serial EEPROM that in turn supports the Plug and Play interface.

MIDI and Game Ports

The MIDI (Musical Instrument Digital Interface) port provides data to a user-supplied external interface between the InterWave IC and a MIDI-compatible Local Area Network (LAN). The MIDI port is built around a UART with a 16-byte receive FIFO.

The game port of the InterWave IC provides the functions found in standard game ports in PCs. The Am78C201 device supports connection of up to two joysticks with a total of four buttons, while the Am78C202 device supports one joystick with four buttons. Trim DACs are provided to adjust the offset voltage for calibration.

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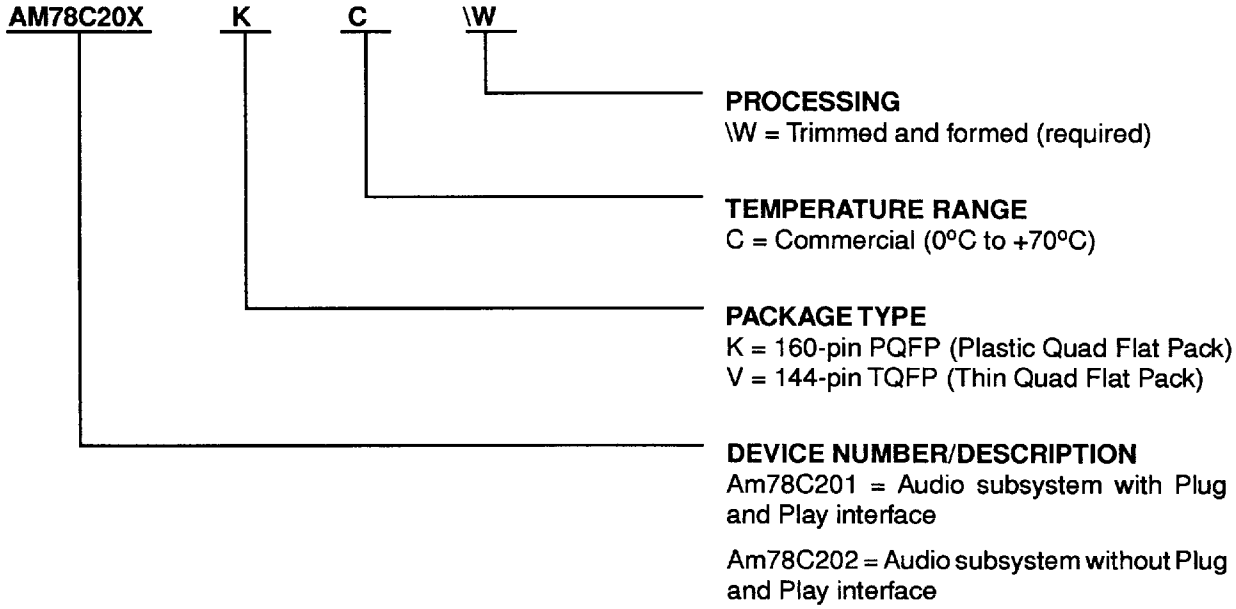
ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order numbers (Valid Combination) are formed by a combination of the elements below.



Valid Combinations	
Am78C201	KC\W
Am78C202	VC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN ASSIGNMENTS AND CONNECTION DIAGRAMS

The InterWave audio IC is packaged in a 160-pin plastic quad flat pack (PQFP) (Am78C201) or a 144-pin thin quad flat pack (TQFP) (Am78C202). Figure 1 shows the package layout and Table 1 lists the pin assignments for both the 144-pin and 160-pin versions. AVCC and AVSS are analog power and ground pins; VCC and VSS are digital power and ground pins.

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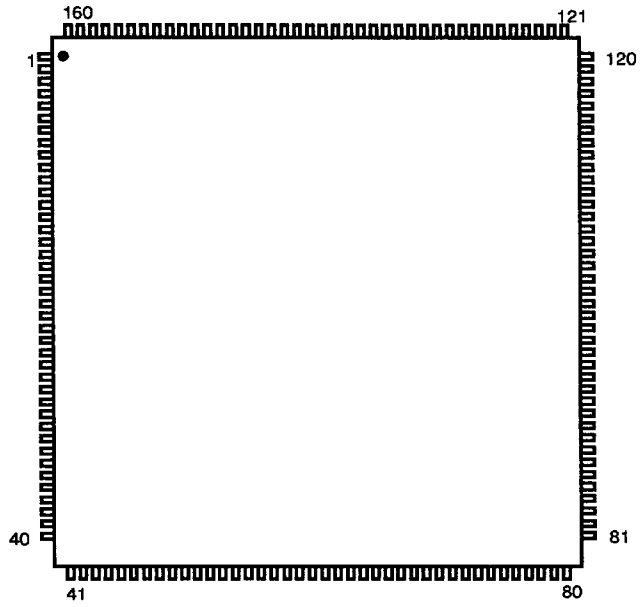
CONNECTION DIAGRAM

160 Pin Top View



CONNECTION DIAGRAM

144 Pin Top View

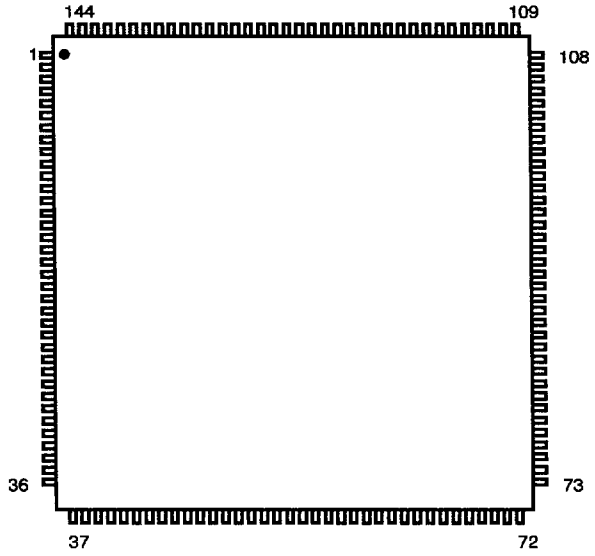


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Table 1. Pin Assignments

144 Pin	160 Pin	Signal Name	144 Pin	160 Pin	Signal Name	144 Pin	160 Pin	Signal Name	144 Pin	160 Pin	Signal Name
	1	SA7	37	41	EX_DRQ	74	81	MD7	109	121	SD11
	2	SA8	38	42	GAMIN3	75	82	VCC	110	122	SD10
1	3	GPOUT0	39	43	GAMIN2		83	DRQ7	111	123	SD9
2	4	RESET	40	44	GAMIN1		84	$\overline{\text{DAK7}}$	112	124	SD8
3	5	GPOUT1	41	45	GAMIN0	76	85	$\overline{\text{ROMCS}}$	113	125	TC
4	6	VCC	42	46	GAMIO3	77	86	$\overline{\text{RAHLD}}$	114	126	DRQ1
5	7	AVSS	43	47	GAMIO2	78	87	$\overline{\text{RAS}}$	115	127	$\overline{\text{DAK1}}$
6	8	AVSS	44	48	GAMIO1	79	88	$\overline{\text{MWE}}$	116	128	AEN
7	9	IREF	45	49	GAMIO0	80	89	RA20	117	129	IOCHRDY
8	10	CFILT	46	50	VSS	81	90	RA21	118	130	IRQ2/9
9	11	AVSS	47	51	VSS	82	91	VCC	119	131	IRQ3
10	12	AVCC	48	52	MA0		92	IRQ15	120	132	$\overline{\text{IOR}}$
11	13	AREF	49	53	MA1		93	IRQ12	121	133	VSS
12	14	AUX1L	50	54	$\overline{\text{EX\_DAK}}$	83	94	$\overline{\text{BKSEL0}}$	122	134	VCC
13	15	MICL	51	55	VCC	84	95	$\overline{\text{BKSEL1}}$	123	135	$\overline{\text{IOW}}$
14	16	AVSS	52	56	MA2	85	96	VSS	124	136	$\overline{\text{IOCS16}}$
15	17	AVCC	53	57	MA3	86	97	$\overline{\text{BKSEL2}}$	125	137	SD0
16	18	AVSS	54	58	MA4	87	98	$\overline{\text{BKSEL3}}$	126	138	SD1
17	19	AUX1R	55	59	MA5		99	IRQ11	127	139	SD2
18	20	MICR	56	60	EX_IRQ	88	100	XTAL1I	128	140	SD3
19	21	AUX2R	57	61	$\overline{\text{EX\_CS}}$	89	101	XTAL1O	129	141	VSS
20	22	LINEINR	58	62	VSS	90	102	VSS	130	142	SD4
21	23	AVSS	59	63	MA6	91	103	XTAL2O	131	143	SD5
22	24	LINEINL	60	64	MA7	92	104	XTAL2I	132	144	SD6
23	25	AUX2L	61	65	MA8	93	105	VCC	133	145	SD7
24	26	AVCC	62	66	MA9	94	106	MIDIRX	134	146	VCC
25	27	LINEOUTR	63	67	MA10	95	107	MIDITX	135	147	VSS
26	28	AVSS		68	$\overline{\text{DAK5}}$	96	108	C32KHZ		148	IRQ5
27	29	LINEOUTL	64	69	MD0	97	109	$\overline{\text{SUSPEND}}$		149	IRQ7
28	30	MONOOUT	65	70	MD1	98	110	VSS	136	150	$\overline{\text{IOCHK}}$
29	31	MONOIN	66	71	MD2	99	111	$\overline{\text{SBHE}}$	137	151	SA0
30	32	AVSS	67	72	MD3	100	112	DRQ0	138	152	SA1
31	33	AVCC	68	73	VSS	101	113	$\overline{\text{DAK0}}$	139	153	SA2
32	34	AVSS		74	DRQ5	102	114	VCC	140	154	SA3
33	35	PNPCS	69	75	VCC	103	115	VCC	141	155	SA4
	36	SA9		76	$\overline{\text{DAK6}}$	104	116	SD15	142	156	SA5
	37	SA10		77	DRQ6	105	117	SD14	143	157	VSS
	38	SA11	70	78	MD4	106	118	SD13		158	DRQ3
34	39	VCC	71	79	MD5	107	119	SD12		159	$\overline{\text{DAK3}}$
35	40	VSS	72	80	MD6	108	120	VSS		160	SA6

Note:
In the 144-pin package, pins 36, 73, and 144 are no connects.

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PIN SUMMARY

Table 2. Am78C201 Pin Designations

System Control		Codec		Local Memory		Ports, Crystals	
Pin Name	**# Pins**	**Pin Name**	**# Pins**	**Pin Name**	**# Pins**	**Pin Name**	**# Pins**
SD15–SD0	16	MIC[L,R]	2	MA10–MA0	11	XTAL1I	1
SA11–SA0*	12	AUX1[L,R]	2	MD7–MD0	8	XTAL1O	1
→SCS[1,0], SA[3–0]		AUX2[L,R]	2	$\overline{\text{BKSEL}}$[3–0]	4	XTAL2I	1
$\overline{\text{SBHE}}$	1	LINEIN[L,R]	2	$\overline{\text{ROMCS}}$	1	XTAL2O	1
DRQ[7,6,5,3,1,0]	6	LINEOUT[L,R]	2	$\overline{\text{RAHLD}}$	1	MIDIRX	1
$\overline{\text{DAK}}$[7,6,5,3,1,0]	6	MONOIN	1	RA21–RA20	2	MIDITX	1
TC	1	MONOOUT	1	$\overline{\text{MWE}}$	1	GAMIN[3–0]	4
IRQ[15,12,11]	3	IREF	1	$\overline{\text{RAS}}$	1	GAMIO[3–0]	4
IRQ[7,5,3,2/9]	4	CFILT	1				
IRQ10, IRQ4*	2→	GPOUT[1–0]	–				
$\overline{\text{IOCHK}}$	1	AREF	1				
$\overline{\text{IOR}}$	1						
$\overline{\text{IOW}}$	1						
$\overline{\text{IOCS16}}$	1						
IOCHRDY	1						
AEN	1						
EX_IRQ*	1→	ESPCLK	–				
EX_DRQ*	1→	ESPDIN	–				
$\overline{\text{EX\_DAK}}$*	1→	ESPSYNC	–				
$\overline{\text{EX\_CS}}$*	1→	ESPDOUT	–				
RESET	1						
$\overline{\text{SUSPEND}}$*	1→			$\overline{\text{FRSYNC}}$	–		
C32KHZ*	1→			$\overline{\text{EFFECT}}$	–		
PNPCS	1						
Power & Ground	37						

Note:
** These pins have multiple functions as indicated.*

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PIN DESCRIPTIONS BY FUNCTIONAL GROUP

Table 3 through Table 8 list pins by function and describes each pin.

Table 3. System Bus Interface Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
AEN	128	116	I, T	**Address Enable** from the ISA bus, used to distinguish between DMA and I/O cycles. This signal must be driven Low when the bus performs an I/O access to the IC.
$\overline{DAK0}$, $\overline{DAK1}$, $\overline{DAK3}$, $\overline{DAK5}$, $\overline{DAK6}$, $\overline{DAK7}$	113, 127, 159, 68, 76, 84	101, 115, N/A	I, T	The selectable **DMA Acknowledge** lines from the ISA bus. $\overline{DAK0}$, $\overline{DAK1}$, and $\overline{DAK3}$ are used for 8-bit DMA transfers and $\overline{DAK5}$, $\overline{DAK6}$, and $\overline{DAK7}$ are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
DRQ0, DRQ1, DRQ3, DRQ5, DRQ6, DRQ7	112, 126, 158, 74, 77, 83	100, 114, N/A	3S, T	The selectable **DMA Request** lines to the ISA bus. DRQ0, DRQ1, and DRQ3 are used for 8-bit DMA transfers and DRQ5, DRQ6, and DRQ7 are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
IOCHRDY	129	117	OD, T	**I/O Channel Ready** to the ISA bus is used to extend the I/O bus cycle when deasserted. IOCHRDY High indicates that the device is ready to complete the current I/O bus cycle.
$\overline{IOCS16}$	136	124	OD, T	**I/O Chip Select 16** is asserted Low by the device during an I/O Read or Write operation to indicate that a 16-bit port is supported at the current address.
$\overline{IOR}$	132	120	I, T	**I/O Read** on the ISA bus is driven Low by the host to indicate that an input/output Read operation is taking place. $\overline{IOR}$ is valid only if the AEN signal is also Low.
$\overline{IOW}$	135	123	I, T	**I/O Write** on the ISA bus is driven Low by the host to indicate that an input/output Write operation is taking place. $\overline{IOW}$ is valid only if the AEN signal is also Low.
IRQ2/9, IRQ3, IRQ5, IRQ7, IRQ11, IRQ12, IRQ15	130, 131, 148, 149, 99, 93, 92	118, 119, N/A	3S, T	The selectable **Interrupt Requests** to the ISA bus. The device can select up to three of the nine supported interrupts; the allocation of interrupt signals is fully programmable using the Plug and Play registers. Internally, interrupt sources can be assigned to the available interrupt request signals as required by software.
IRQ4, IRQ10	3, 5	1, 3	3S, C	See description for **Interrupt Requests**. These pins are multiplexed with GPOUT0 and GPOUT1. IRQ4 and IRQ10 are selected by IEIRQI[7] = 0 ($\overline{EX\_DAK}$ = 0 at reset). See the *InterWave Programmer's Guide*.
$\overline{IOCHK}$	150	136	OD, T	**I/O Check**. Channel or I/O channel check on the ISA bus. $\overline{IOCHK}$ is asserted Low by the device to generate an NMI (non-maskable interrupt).
PNPCS	35	33	B, T	**Plug and Play Serial EEPROM Chip Select**. Active High output used as chip select for the Plug and Play serial EEPROM. This is an input during reset; its state is latched by the trailing edge of reset to determine whether the IC is in PNP-compliant mode (Low) or PNP-system mode (High).
RESET	4	2	I, T	**Reset** from the ISA bus. When RESET is asserted High on the ISA bus, the device performs an internal system reset. The RESET pin must be asserted for at least 10 ms before being deasserted. While in the reset state, the device ignores all ISA bus activity and no local memory cycles take place. On the trailing edge of RESET, the state of some I/O pins are latched to determine the configuration of certain multifunction pins.
$\overline{SBHE}$	111	99	I, T	The **System Byte High Enable** signal indicates the High byte of the system data bus is to be used. When connecting to an 8-bit ISA bus, this pin must be disconnected.

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Table 3. System Bus Interface Pins (continued)

Pin Name	Pin (201)	Pin (202)	Type	Description
SD15–SD0	116–119, 121–124, 145–142, 140–137	104–107, 109–112, 133–130, 128–125	B, T	The ISA **System Data Bus** is used to transfer data to and from the device. The entire data bus, SD15–SD0, is active during 16-bit I/O access. During 8-bit I/O accesses, the lower data bus, SD7–SD0, is active when accessing an even byte, and the upper data bus, SD15–SD8, is active when accessing an odd byte.
TC	125	113	I, T	**Transfer Complete** or **Terminal Count** is driven active High by the master or slave DMAC when the word or byte transfer count for a DMA channel is complete.

Note:
Pin Type: A = analog signal, B = digital bi-directional, C = CMOS compatible, I = digital input, O = digital output, OD = digital open drain output, P = power or ground, T = TTL compatible, 3S = digital 3-state output

Table 4. Codec/Mixer Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
AREF	13	11	A	The **Analog Reference** pin provides a reference voltage which can be used by external amplifier circuitry. When VCC is at +5 V, the value of this output pin is 0.376 times VCC, nominal. When VCC is at +3.3 V, the value of AREF is 0.303 times VCC, nominal. AREF is capable of sinking up to 250 µA without degradation and can be placed into High-impedance mode, as controlled by the Mono Input and Output Control (CMONOI) register. See the *InterWave Programmer's Guide*.
AUX1L, AUX1R	14, 19	12, 17	A	The **Stereo Auxiliary 1 Inputs** provide an alternative input path and are multiplexed with the synthesizer DAC outputs. Only one of these sources can be mixed and supplied to LINEOUT as selected in Configuration Register 3 (CFIG3I). See the *InterWave Programmer's Guide*. Either of these sources can be selected for analog-to-digital conversion through the Record Multiplexer. The AUX1 input impedance is at least 20 kΩ.
AUX2L, AUX2R	25, 21	23, 19	A	The **Stereo Auxiliary 2 Inputs** can always be independently mixed or muted. Typically, these inputs are used for mixing analog CD stereo audio. The AUX2 input impedance is at least 20 kΩ.
CFILT	10	8	A	The **Capacitor Filter** input must be connected to analog ground through a 0.1-µF capacitor and a 10-µF capacitor.
GPOUT0, GPOUT1	3, 5	1, 3	3S, T	The **General Purpose Digital Outputs** are two general purpose digital outputs controlled by bits located in the External Control (CEXTI) register. These pins are multiplexed with IRQ4 and IRQ10. GPOUT0 and GPOUT1 are selected by IEIRQI[7] = 1 ($\overline{\text{EX\_DAK}}$ = 1 at reset). See the *InterWave Programmer's Guide*.
IREF	9	7	A	The Current Reference input pin must be connected to analog ground through a 61.9-kΩ 1% tolerance resistor.
LINEINL, LINEINR	24, 22	22, 20	A	The **Stereo Line Inputs** can always be independently mixed or muted. These inputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these inputs are used for mixing or recording analog stereo audio from a variety of external stereo audio sources. The LINEIN input impedance is at least 20 kΩ.
LINEOUTL, LINEOUTR	29, 27	27, 25	A	The **Stereo Line Outputs** are stereo single-ended line drivers which can drive 5-kΩ loads. These outputs are the sum of the left and right mixer channels respectively. The LINEOUTs can be independently attenuated or muted and these mixer outputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these outputs are used for driving powered speakers or connected to speaker or headphone drivers.

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Table 4. Codec/Mixer Pins (continued)

Pin Name	Pin (201)	Pin (202)	Type	Description
MICL, MICR	15, 20	13, 18	A	The **Stereo Microphone Inputs** can be independently mixed or muted. These inputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these inputs are used for mixing or recording a preamplified signal from a stereo microphone. The MIC input impedance is at least 20 kΩ.
MONOIN	31	29	A	The **Mono Input** can always be independently mixed or muted and feeds both the left and right mixer output paths. Typically, this input is used for mixing PC speaker audio. The MONOIN input impedance is at least 20 kΩ.
MONOOUT	30	28	A	The **Mono Output** is a single-ended line driver which can drive a 5 kΩ load. It provides the sum of the left and right LINEOUT signals and is independently mutable. Typically, this output is connected to a speaker driver for a PC speaker.

Table 5. Local Memory Controller Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
$\overline{\text{BKSEL0}}$–$\overline{\text{BKSEL3}}$	94, 95, 97, 98	83, 84, 86, 87	O, C	The **Bank Select** signals are used to control the $\overline{\text{CAS}}$ input of each DRAM bank or the Output Enable input of each ROM bank.
MA3–MA10	57–59, 63–67	53–55, 59–63	B, C	The **Memory Address** signals are multiplexed row-column address lines for DRAM cycles. For ROM access cycles, they are time multiplexed ROM Latched Address[10:3] outputs and ROM High Byte Data Bus[15:8] inputs. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal.
MA0–MA2	52, 53, 56	48, 49, 52	O, C	**Memory address**. The multiplexed row-column address bits for DRAM cycles, and the RLA[2,1,19] outputs for ROM access cycles.
MD7–MD0	69–72, 78–81	64–67, 70–72, 74	B, C	The **Memory Data Bus** for DRAM cycles. For ROM access cycles, they are time-multiplexed ROM Latched Address[18:11] outputs and ROM Low Byte Data Bus[7:0]. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal. For Plug and Play Serial EEPROM accesses, MD[2] is the Serial Data Clock (SK), MD[1] is the Serial Data Input (DI), and MD[0] is the Serial Data Output (DO).
$\overline{\text{MWE}}$	88	79	B, C	The **Memory Write Enable** output controls the $\overline{\text{WE}}$ pin of all the DRAM banks and determines whether a DRAM cycle is a Read or Write. This pin remains High during all refresh cycles.
RA20–RA21	89, 90	80, 81	B, C	The High **ROM Address** lines during ROM accesses. At the trailing edge of RESET, these signals become inputs that are used to determine the operation mode of certain multiplexed function pins.
$\overline{\text{RAHLD}}$	86	77	O, C	The **ROM Address Hold** output is used to latch the state of ROM Latched Address lines, MD[7:0] (RLA[18:11]), and MA[10:3] (RLA[10:3]), in external latches during ROM accesses.
$\overline{\text{RAS}}$	87	78	O, C	The **Row Address Strobe** is asserted Low during DRAM accesses and is connected directly to the $\overline{\text{RAS}}$ input of each DRAM in all of the DRAM banks.
$\overline{\text{ROMCS}}$	85	76	O, C	The **ROM Chip Select** output is asserted Low during ROM accesses and is connected directly to the Chip Select/Enable input of each ROM in all of the ROM banks.

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Table 6. Additional Multiplexed Function Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
C32KHZ / $\overline{\text{EFFECT}}$	108	96	I, C O, C	The **Suspend Mode Refresh Clock** input (C32 kHz) is used for refreshing local memory DRAM when the InterWave IC is in Suspend mode. This pin can also be the **Synthesizer Effect Local Memory Writes** output ($\overline{\text{EFFECT}}$), which is asserted Low during writes to local memory DRAM involving synthesizer delay-based effects. The operation mode of this pin is determined by the state of RA[21] at the trailing edge of RESET. If RA[21] is High at the trailing edge of RESET, the C32-kHz pin function is selected; if RA[21] is Low, the $\overline{\text{EFFECT}}$ signal is selected.
$\overline{\text{EX\_CS}}$ / ESPDOUT	61	57	B, T O, T	The **External Device Chip Select** consisting of the decode of AEN deasserted (Low) and the address specified in the PNP CD-ROM Address High/Low (PRAHI and PRALI) registers. Optionally, this pin can be configured as the **External Serial Port Data Out** signal (ESPDOUT) through the Compatibility (ICMPTI) register.
$\overline{\text{EX\_DAK}}$ / ESPSYNC	54	50	B, T O, T	The **External Device DMA Acknowledge** output to the external device. Optionally, this pin can be configured as the **External Serial Port Sync** signal (ESPSYNC) through the Compatibility (ICMPTI) register.
EX_DRQ / ESPDIN	41	37	I, T I, T	**External Device DMA Request**. Optionally, this pin can be configured as the **External Serial Port Data In** signal (ESPDIN) through the Compatibility (ICMPTI) register.
EX_IRQ / ESPCLK	60	56	I, T O, T	**External Device Interrupt Request**. Optionally, this pin can be configured as the 2.1168-MHz **External Serial Port Clock** output signal (ESPCLK) through the Compatibility (ICMPTI) register.
SA11–SA6 SA5–SA0/ SCS1–SCS0, SA3–SA0	38–36, 2, 1, 160 156–151	N/A 142–137	I, T I, T	**System Address Bus**. During Internal Decoding mode, these inputs are the 12 lower lines of the ISA System Address Bus which are used along with AEN to generate decodes for internal device resources. During External Decoding mode, the System Address Bus is redefined as follows: SA[11:6] are not used, SA[5:4] are redefined as **System Chip Selects** (SCS[1:0]), and the lower address lines SA[3:0] are unchanged. The decoding mode is determined by the state of RA[20] at the trailing edge of the RESET signal. If RA[20] is Low at the trailing edge of RESET, Internal Decoding mode is selected; if RA[20] is High, External Decoding mode is selected.
$\overline{\text{SUSPEND}}$ / $\overline{\text{FRSYNC}}$	109	97	I, C O, C	When the **Suspend** input is asserted Low, all chip activity becomes frozen, the oscillators are turned off, the C32-kHz input clock is used to refresh local memory DRAM, and most of the ISA bus inputs and outputs are isolated from the IC. This pin can also be used as the **Frame Sync** output, which is asserted Low at the start of each synthesizer data frame. The operation mode of this pin is determined by the state of RA[21] at the trailing edge of the RESET signal. If RA[21] is High at the trailing edge of RESET, the $\overline{\text{SUSPEND}}$ input function is selected; if RA[21] is Low, the $\overline{\text{FRSYNC}}$ output signal is selected.

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Table 7. Game and MIDI Port Pins, Crystal Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
GAMIN3–GAMIN0	42–45	38–41	I, C	The **Game Inputs** are used to monitor the state of buttons on external joystick(s). The state of these inputs can be read from the Game Control (GGCR) register. These pins are internally pulled up through a nominal 6-kΩ resistance.
GAMIO3–GAMIO0	46–49	42–45	A	The **Game I/O** pins are used to determine the state of potentiometers on an external joystick to obtain the joystick's X-Y position.
MIDITX	107	95	B	The **MIDI Transmit** output is used to send serial digital data from the internal Motorola MC6850-compatible UART.
MIDIRX	106	94	I	The **MIDI Receive** input is used to receive serial digital data into the internal Motorola MC6850-compatible UART.
XTAL1I	100	88		**Crystal 1 Input**. Input from the 24.576-MHz crystal. The clock used by the codec module to support select sampling rates is derived from the 24.576-MHz crystal attached to the XTAL1 pins. An external 24.576-MHz CMOS-compatible clock is not supported.
XTAL1O	101	89		**Crystal 1 Output**. Output from the 24.576-MHz crystal.
XTAL2I	104	92		**Crystal 2 Input**. Input from the 16.9344-MHz crystal. The main clocks used throughout the IC are derived from the 16.9344-MHz crystal attached to the XTAL2 pins. An external 16.9344-MHz CMOS-compatible clock is not supported.
XTAL2O	103	91		**Crystal 2 Output**. Output from the 16.9344-MHz crystal.

Table 8. Power Supply Pins

Pin Name	Pin (201)	Pin (202)	Type	Description
AVCC	12, 17, 26, 33	10, 15, 24, 31	P	**Analog Power**. Supplies power to analog portions of the InterWave IC.
VCC	6, 39, 55, 75, 82, 91, 105, 114, 115, 134, 146	4, 34, 51, 69, 75, 82, 93, 102, 103, 122, 134	P	**Digital Power**. Supplies power to digital portions of the InterWave IC.
AVSS	7, 8, 11, 16, 18, 23, 28, 32, 34	5, 6, 9, 14, 16, 21, 26, 30, 32	P	**Analog Ground**. Supplies ground reference to analog portions of the InterWave IC.
VSS	40, 50, 51, 62, 73, 96, 102, 110, 120, 133, 141, 147, 157	35, 46, 47, 58, 68, 85, 90, 98, 108, 121, 129, 135, 143	P	**Digital Ground**. Supplies ground reference to digital portions of the InterWave IC.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature Under Bias . –65°C to +125°C

Supply Voltage VCC to VSS . . . . . –0.5 V to +7 V

All digital inputs within the range . . . . . –0.5 V to VCC +0.5 V

All analog inputs within the range . . . . . –0.5 V to AVCC +0.5 V

Supply voltage . . . . . AVCC to AVSS –0.5 V to +7 V

Supply voltage . . . . . VCC to AVCC ±0.5 V

Supply voltage . . . . . VSS to AVSS ±0.5 V

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature. . . . . 0°C to +70°C

VCC . . . . . 4.75 V to 5.25 V or 3.0 V to 3.6 V

AVCC . . . . . 4.75 V to 5.25 V or 3.0 V to 3.6 V

ELECTRICAL CHARACTERISTICS over COMMERCIAL operating ranges

Table 9. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
TTL-Compatible Input Voltage (VCC = 4.75 V to 5.25 V) All Digital Inputs (VCC = 3.0 V to 3.6 V)						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.0		VCC +0.5	V
CMOS-Compatible Input Voltage (VCC = 4.75 V to 5.25 V)						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		3.7		VCC +0.5	V
Digital Output Voltage						
VOL	Output Low Voltage				0.5	V
VOH	Output High Voltage		2.4			V
Digital Leakage Current						
IIX	Input Leakage Current		–10		10	µA
IOZL	Output Low Leakage Current		–10			µA
IOZH	Output High Leakage Current				10	µA
Crystal Input						
FCK1	Crystal 1 Frequency			24.576		MHz
FCK2	Crystal 2 Frequency			16.9344		MHz
Power Supply Current						
	Total Operating Current (Digital and Analog)	Note 2		140	TBD	mA
	Analog Operating Current	Note 1		TBD	TBD	mA
	Digital, Suspend			TBD	TBD	µA

Notes:

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

2. All applicable output pins are three-stated.

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Table 10. Maximum Drive Table For VOL and VOH Specifications, VCC = 5 V

Signals	Load Cap. (pF)	IOL (mA)	IOH (mA)	Notes
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$, $\overline{\text{IOCHK}}$	240	24	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$, $\overline{\text{IOCHK}}$	120	12	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$, $\overline{\text{IOCHK}}$	60	3	-3	1, 2
DRQ[7:5,3,1:0], IRQ[15,12,11,7,5,3,2], GPOUT[1:0]	120	5	-3	2
PNPCS, $\overline{\text{CD\_CS}}$, $\overline{\text{CD\_DAK}}$, CD_IRQ, MIDITX, $\overline{\text{RAHLD}}$, $\overline{\text{EFFECT}}$, $\overline{\text{FRSYNC}}$	50	3	-3	3
MA[10:0], MD[7:0], $\overline{\text{BKSEL}}$[3:0], $\overline{\text{ROMCS}}$, RA[21:20], $\overline{\text{MWE}}$, $\overline{\text{RAS}}$	120	3	-3	

Notes:

1. *The maximum drive capability for these signals is selectable via programmable register. See the InterWave Programmer's Guide.*
2. *There is no IOH value for the open collector outputs.*
3. *$\overline{\text{EFFECT}}$ and $\overline{\text{FRSYNC}}$ are multiplexed with the $\overline{\text{SUSPEND}}$ and C32-kHz inputs. Also, CD_IRQ can be selected as the output ESPCLK.*

Table 11. Maximum Drive Table For VOL, VOH Specifications, VCC = 3.3 V

Signals	Load Cap. (pF)	IOL (mA)	IOH (mA)	Notes
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$, $\overline{\text{IOCHK}}$	60	TBD	TBD	2
DRQ[7:5,3,1:0], IRQ[15,12,11,7,5,3,2], GPOUT[1:0]	60	TBD	TBD	2
PNPCS, $\overline{\text{CD\_CS}}$, $\overline{\text{CD\_DAK}}$, CD_IRQ, MIDITX, $\overline{\text{RAHLD}}$, $\overline{\text{EFFECT}}$, $\overline{\text{FRSYNC}}$	50	TBD	TBD	3
MA[10:0], MD[7:0], $\overline{\text{BKSEL}}$[3:0], $\overline{\text{ROMCS}}$, RA[21:20], $\overline{\text{MWE}}$, $\overline{\text{RAS}}$	80	TBD	TBD	

Notes:

1. *The maximum drive capability for these signals is selectable via programmable register. See the InterWave Programmer's Guide.*
2. *There is no IOH value for the open collector outputs.*
3. *$\overline{\text{EFFECT}}$ and $\overline{\text{FRSYNC}}$ are multiplexed with the $\overline{\text{SUSPEND}}$ and C32-kHz inputs. Also, CD_IRQ can be selected as the output ESPCLK.*

Table 12. Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
A/D							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range		80	85		dB	
THD	Total Harmonic Distortion				0.02	%	
	Signal-to-Intermodulation Distortion			90			1
	Offset Error			TBD	TBD	bits	1
	Gain Error				TBD	%	
Mixer Inputs							
	Full Scale Input Voltage			2.9		Vp-p	
	Input Resistance		20			kΩ	1
	Input Capacitance				15	pF	1

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Table 12. Electrical Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
	Interchannel Isolation						
	Line-Line		75	80		dB	
	Line-Mic		75	80		dB	
	Line-Aux1		75	80		dB	
	Line-Aux2		75	80		dB	
	Interchannel Gain Mismatch				0.5	dB	
	Programmable Gain Range (CLICI)		21.5		23.5	dB	3
	Programmable Gain Step Size (CLICI)		1.3		1.7	dB	3
	Programmable Gain Range (CLOAI)		45.5		47.5	dB	3
	Programmable Gain Step Size (CLOAI)		1.3		1.7	dB	3
	Programmable Gain Range (CMONOI)		44.0		46.0	dB	3
	Programmable Gain Step Size (CMONOI)		1.3		1.7	dB	3
Mixer Outputs							
	Full Scale Output Voltage, OFVS = 1	measured at LINEOUT		2.9		Vp-p	
	Full Scale Output Voltage, OFVS = 0	measured at LINEOUT		2.0		Vp-p	
	External Load Impedance	LINEOUT, MONOOUT	5			kΩ	2
	External Load Capacitance				100	pF	
	Audible Out-of-Band Energy 0.6 Fs to 20 kHz	measured at Fs = 8 kHz		-70		dB	1
	Mute Attenuation		80			dB	
	AREF Drive		-0.25		1.0	mA	
	AREF Level			0.376 VCC		V	
	Programmable Gain Range (CLCI, CLDACI)		93.5		95.5	dB	3
	Programmable Gain Step Size			1.5		dB	
	Line-to-Line Interchannel Isolation	measured at LINEOUT	75	80		dB	
	Interchannel Gain Mismatch				±0.5	dB	
Synthesizer D/A							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range			85		dB	1
THD	Total Harmonic Distortion			0.01	0.02	%	1
	Signal-to-Intermodulation Distortion			85			1
	Gain Error			-0.5		dB	1
Codec D/A							
	Resolution			16		bits	
IDR	Instantaneous Dynamic Range		80	85		dB	

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Table 12. Electrical Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
THD	Total Harmonic Distortion			0.01	0.02	%	
	Signal-to-Intermodulation Distortion			85			1
	Gain Error		−0.5		0.5	dB	
	Deviation from Linear Phase			1	Degree		1
Game Port							
	Joystick Trim DAC Threshold				TBD	V	
	Joystick Trim DAC Step Size				TBD	V	

Notes:
VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. *This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.*
2. *Outputs AC coupled.*
3. *See InterWave Programmer's Guide.*

Table 13. Digital Filter Characteristics—Playback

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		±0.1	dB	1
	Transition Band		.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		−107	dB	1

Notes:
VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. *This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.*

Table 14. End-To-End Frequency Characteristics—Playback (Measured at LINEOUT)

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	±0.2	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1

Notes:
VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. *This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.*

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Table 15. Digital Filter Characteristics—Record

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		0.1	dB	1
	Transition Band		0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		−100	dB	1

Notes:
VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. *This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.*

Table 16. End-To-End Frequency Characteristics—Record

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	±0.2	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1

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Table 17. Switching Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit	Notes
System Control						
t_{AS}	Address Setup		88		ns	
t_{AH}	Address Hold		32		ns	
t_{AR}	Address Recovery		152		ns	
t_{SW}	Read or Write Strobe Width		TBD		ns	
t_{DDW}	Data Delay (Write)			61	ns	
t_{DHW}	Data Hold (Write)			25	ns	
t_{DDR}	Data Delay (Read)			103	ns	
t_{DHR}	Data Hold (Read)		0		ns	
t_{RD}	Ready Delay			76	ns	
t_{ID}	I/O Delay			116	ns	
t_{IDD}	I/O Delay (Read)			59	ns	
Serial Interface						
f_{SF}	Serial Clock Frequency			2.1168	MHz	
t_{SC}	Serial Clock Period			472	ns	
t_{SH}	Serial Clock High		t_{SC}/2-15		ns	
t_{SK}	Serial Clock Low		t_{SC}/2-15		ns	
t_{SSS}	Serial Sync Setup		10		ns	
t_{SSH}	Serial Sync Hold		10		ns	
t_{SDS}	Serial Data In Setup		TBD		ns	
t_{SDD}	Serial Data Out Delay		TBD		ns	
Local Memory Control						
t_{RAS}	$\overline{RAS}$ Pulse Width		177		ns	2
t_{RC}	Read or Write Cycle Time		236		ns	2
t_{RP}	$\overline{RAS}$ Precharge Time		59		ns	2
t_{RCD}	$\overline{RAS}$ to $\overline{BKSEL}$ Delay Time			58	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time			119	ns	2
t_{ASR}	Row Address Setup Time		31		ns	2
t_{CAS8}	$\overline{BKSEL}$ Pulse Width		146		ns	2
t_{RAH}	Row Address Hold Time		29		ns	2
t_{ASC}	Column Address Setup Time		30		ns	2
t_{CAH}	Column Address Hold Time		147		ns	2
t_{RAL}	Column Address To $\overline{RAS}$ Rising Edge		149		ns	2
t_{RCS}	Read Command Setup Time		83		ns	2
t_{RCH}	Read Command Hold Time from $\overline{BKSEL}$		59		ns	2
t_{CRP}	$\overline{BKSEL}$ to $\overline{RAS}$ Precharge Time		32		ns	2
t_{DCS}	Read Data Setup Time		37		ns	
t_{DCH}	Read Data Hold Time		50		ns	
t_{WP}	Write Pulse Width		179		ns	2
t_{WCS8}	Write Command Setup Time		26		ns	2
t_{WS8}	Write Data Setup Time		88		ns	
t_{WH}	Write Data Hold Time		118		ns	
t_{CAS16}	$\overline{BKSEL}$ Pulse Width		60		ns	2
t_{WCS16}	Write Command Setup		26		ns	2
t_{WS16}	Write Data Setup		88		ns	2

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Table 17. Switching Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit	Notes
DRAM Refresh						
t_{RPC}	$\overline{RAS}$ Precharge $\overline{BKSEL}$ Hold Time		61		ns	2
t_{CP}	$\overline{BKSEL}$ Recharge Time		32		ns	2
t_{CSR}	$\overline{BKSEL}$ Setup Time (Refresh)		50		ns	2
t_{CHR}	$\overline{BKSEL}$ Hold Time (Refresh)		60		ns	2
DRAM Suspend Mode Refresh						
t_{SCD}	Suspend to $\overline{BKSEL}$ Delay		160		ns	1, 2
t_{CRD}	$\overline{BKSEL}$ to $\overline{RAS}$ Delay		31.25		µs	2
t_{RW125}	$\overline{RAS}$ Pulse Width		31.25		µs	2
t_{RI125}	$\overline{RAS}$ Pulse Interval		124.8		µs	2
t_{RW62}	$\overline{RAS}$ Pulse Width		31.2		µs	
t_{RI62}	$\overline{RAS}$ Pulse Interval		62.4		µs	
ROM Read						
t_{AS1}	Address Setup Time (bits 19, 2, 1)		24		ns	2
t_{AS2}	Address Setup Time (bits 10–3)		55		ns	2
t_{AS3}	Address Setup Time (bits 18–11)		24		ns	2
t_{AS4}	Address Setup Time (bits 21–20)		24		ns	2
t_{AH1}	Address Hold Time (bits 19, 2, 1)		237		ns	2
$t_{AH2, 3}$	Address Hold Time (bits 18–3)		80		ns	2
t_{RC}	Read Cycle Time		102		ns	2
t_{DF}	Output Disable Time		29		ns	2
t_{ACE}	Chip Enable Access Time			239	ns	
t_{OE}	Output Enable Access Time			161	ns	
t_{RDS}	Read Data Setup Time		58		ns	
t_{RDH}	Read Data Hold Time			70	ns	

VCC = 5.0 V; Ambient temperature = 25°C.

1. *This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.*
2. *XTAL2 frequency = 16.9344 MHz.*

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FILTER RESPONSE

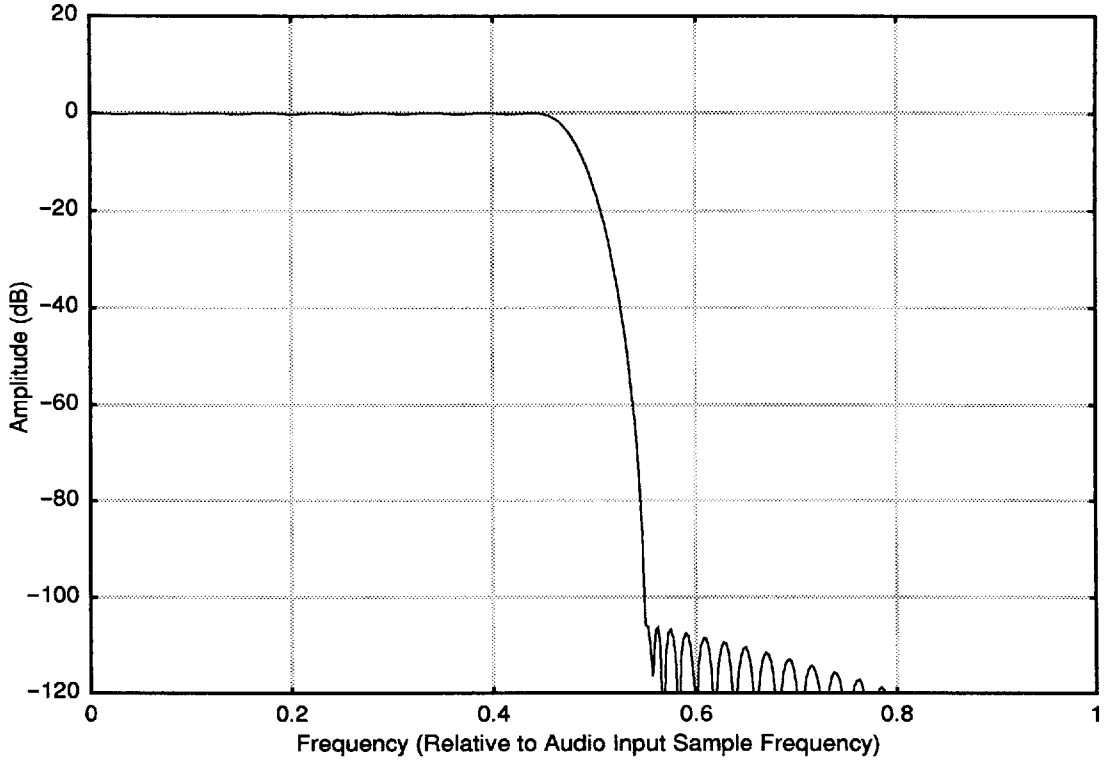

Figure 1. DAC Filter Response

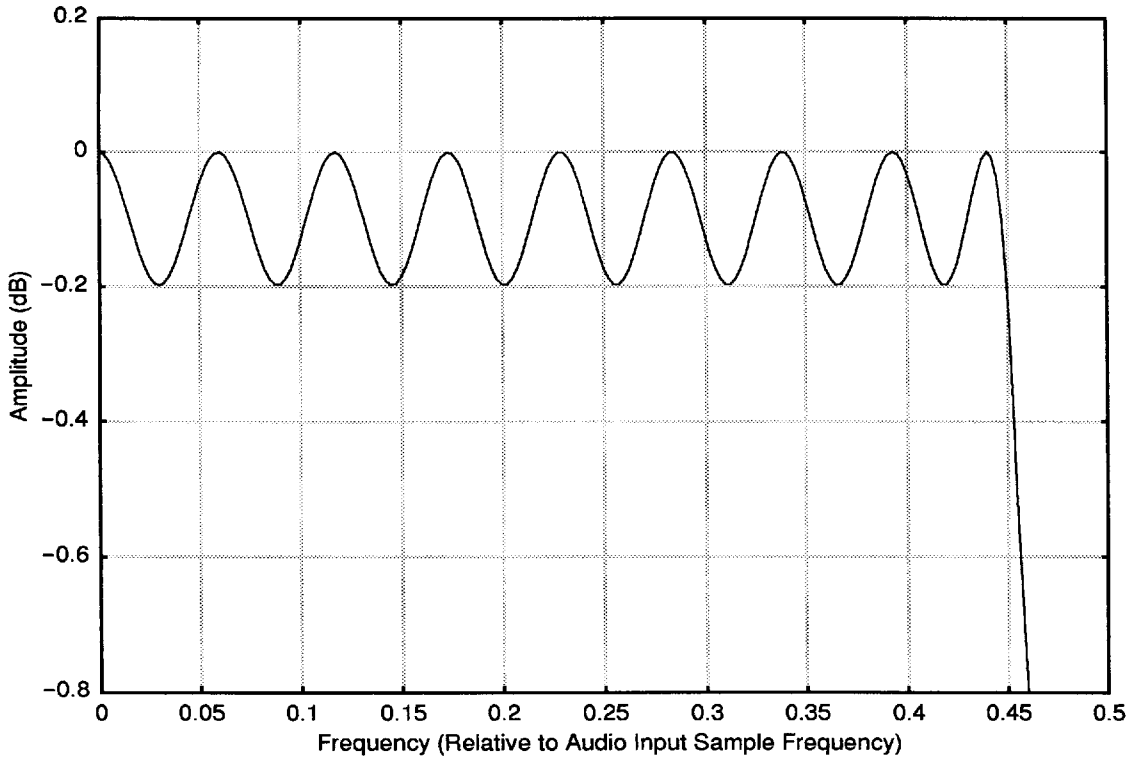

Figure 2. DAC Filter In Band Response

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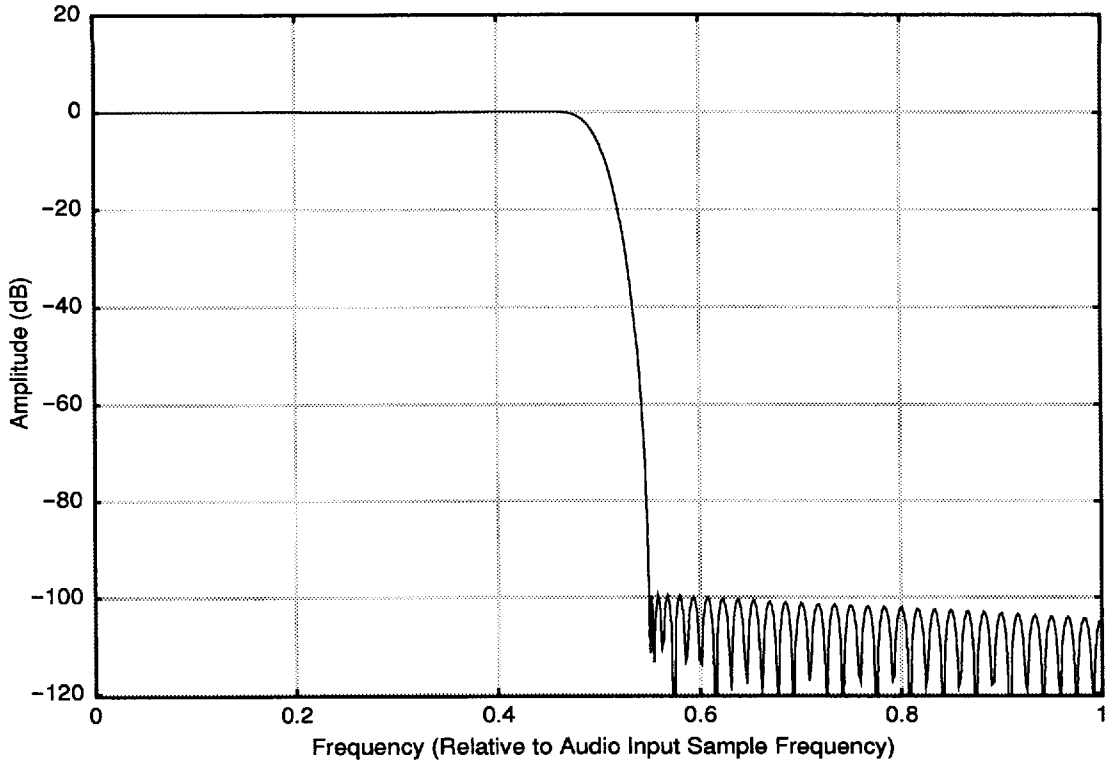

Figure 3. ADC Filter Response

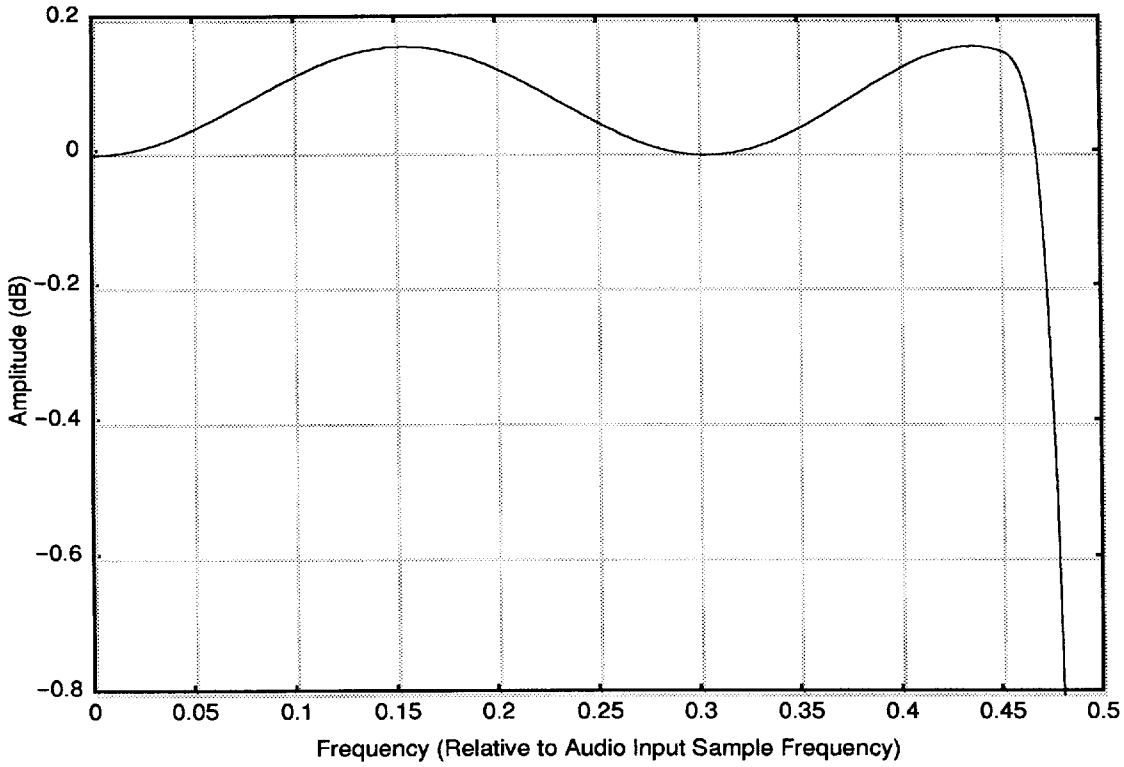

Figure 4. ADC Filter In Band Response

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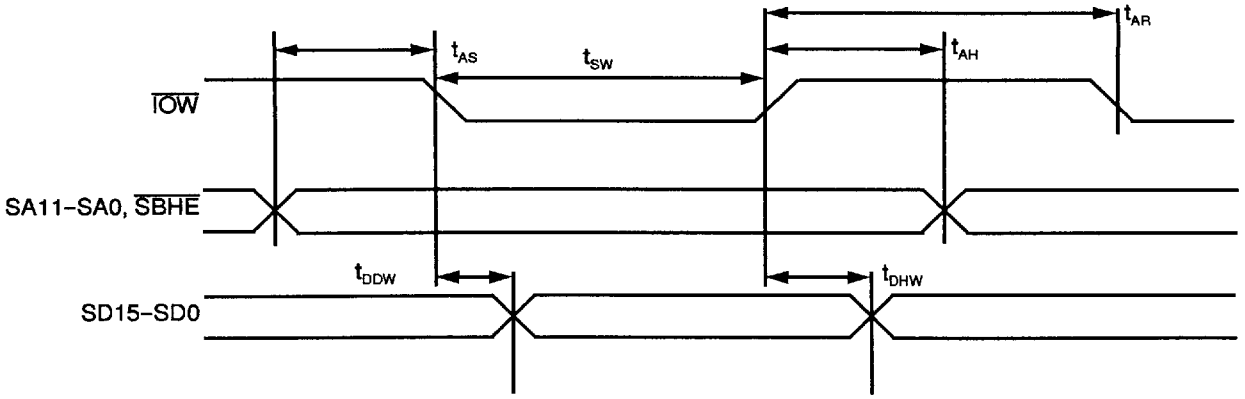
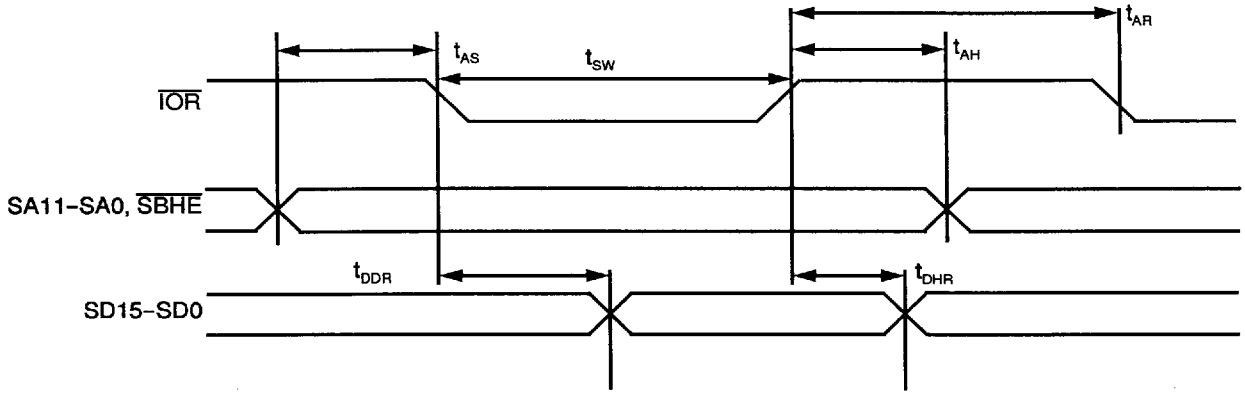


ISA Bus Write Cycle Timing



ISA Bus Read Cycle Timing

Figure 5. ISA Bus Cycle Timing

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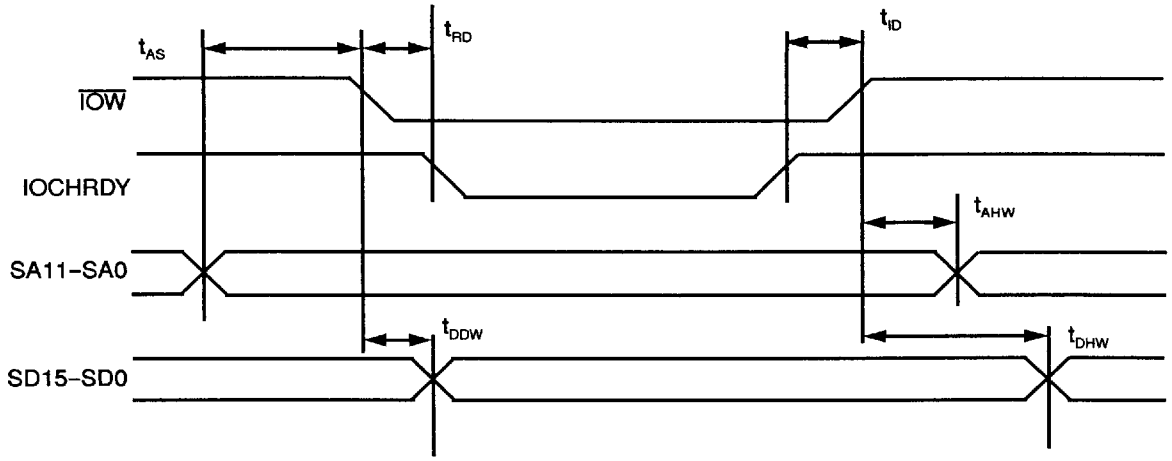
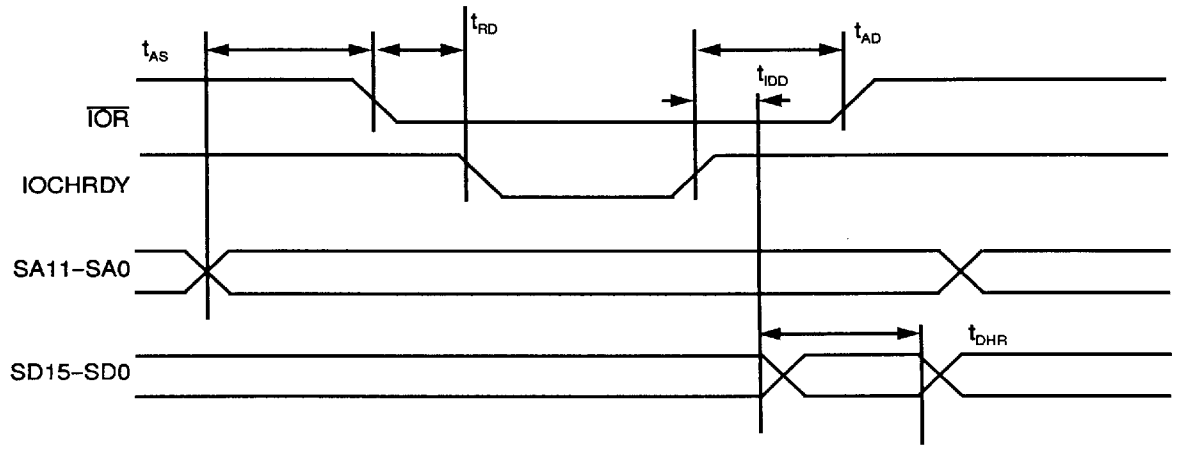


ISA Bus Extended Write Cycle Timing



ISA Bus Extended Read Cycle Timing

Figure 6. ISA Bus Extended Cycle Timing

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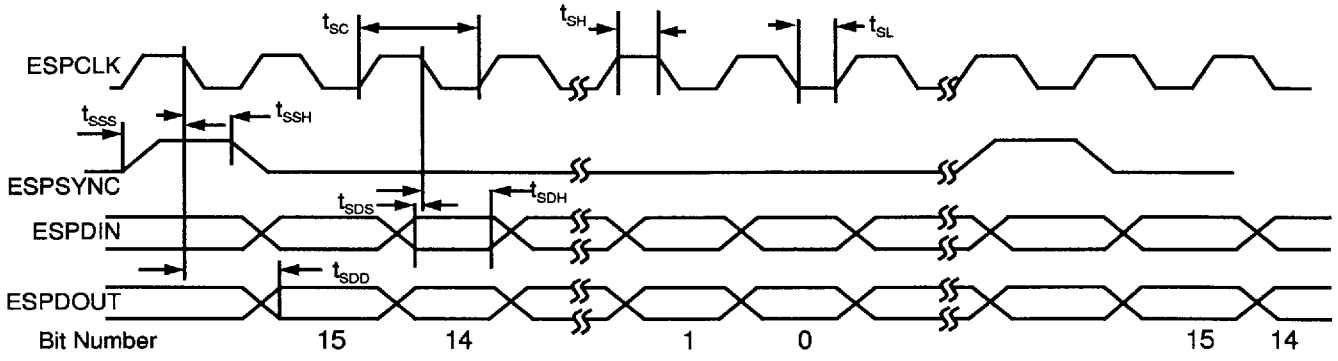

Figure 7. Serial Port Timing: Record FIFO Output, Playback FIFO Input

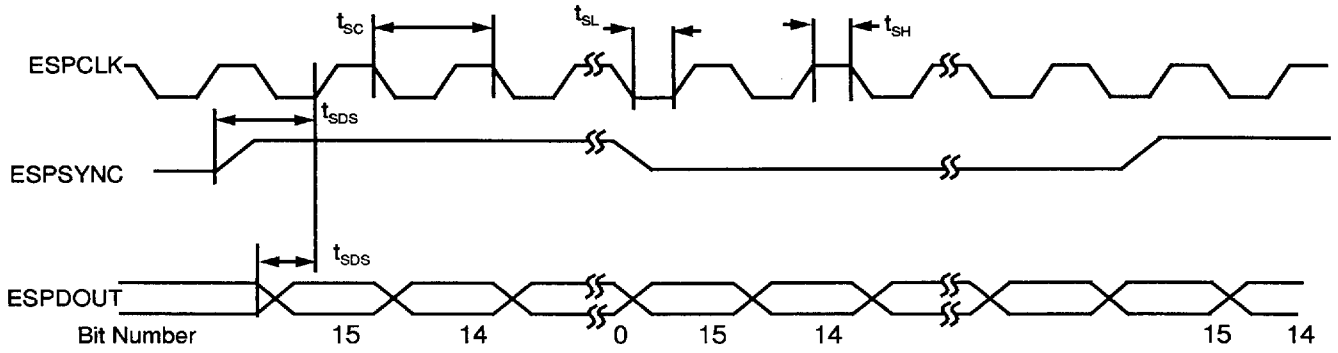

Figure 8. Serial Port Timing: Synthesizer Output

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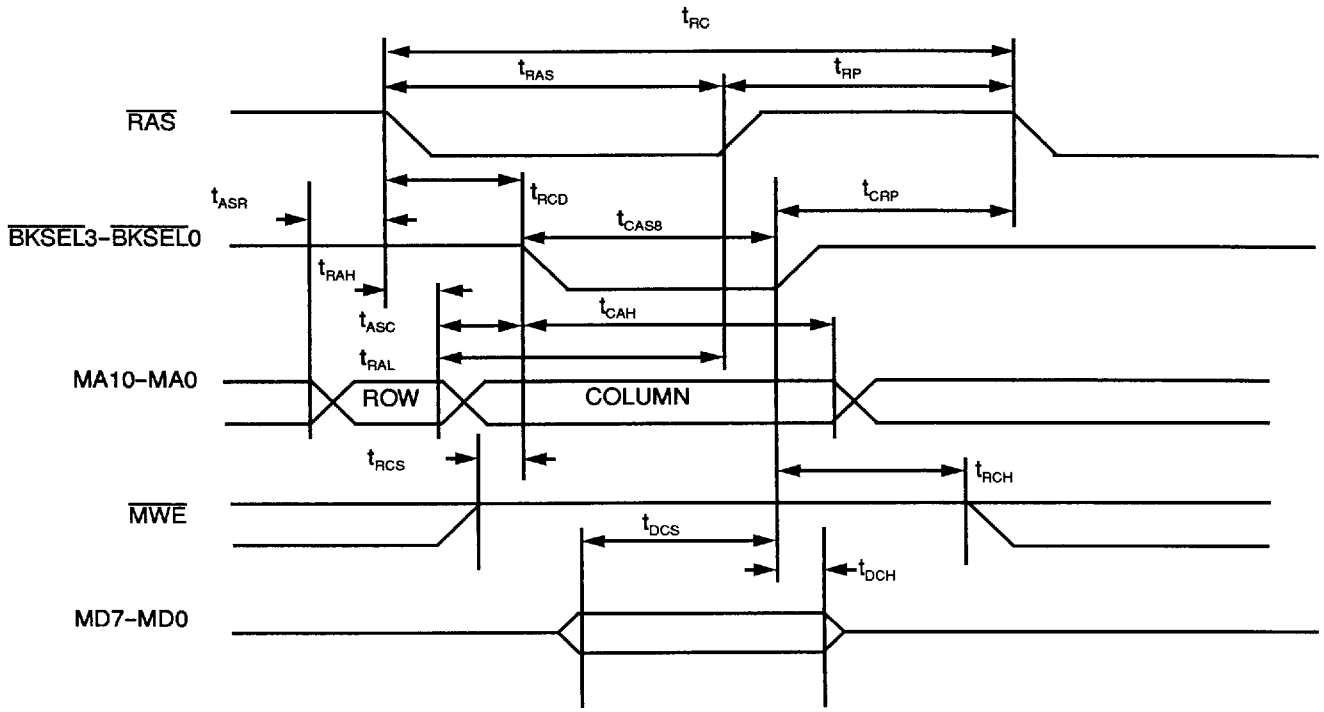

Figure 9. Local Memory: DRAM Read—8 bit

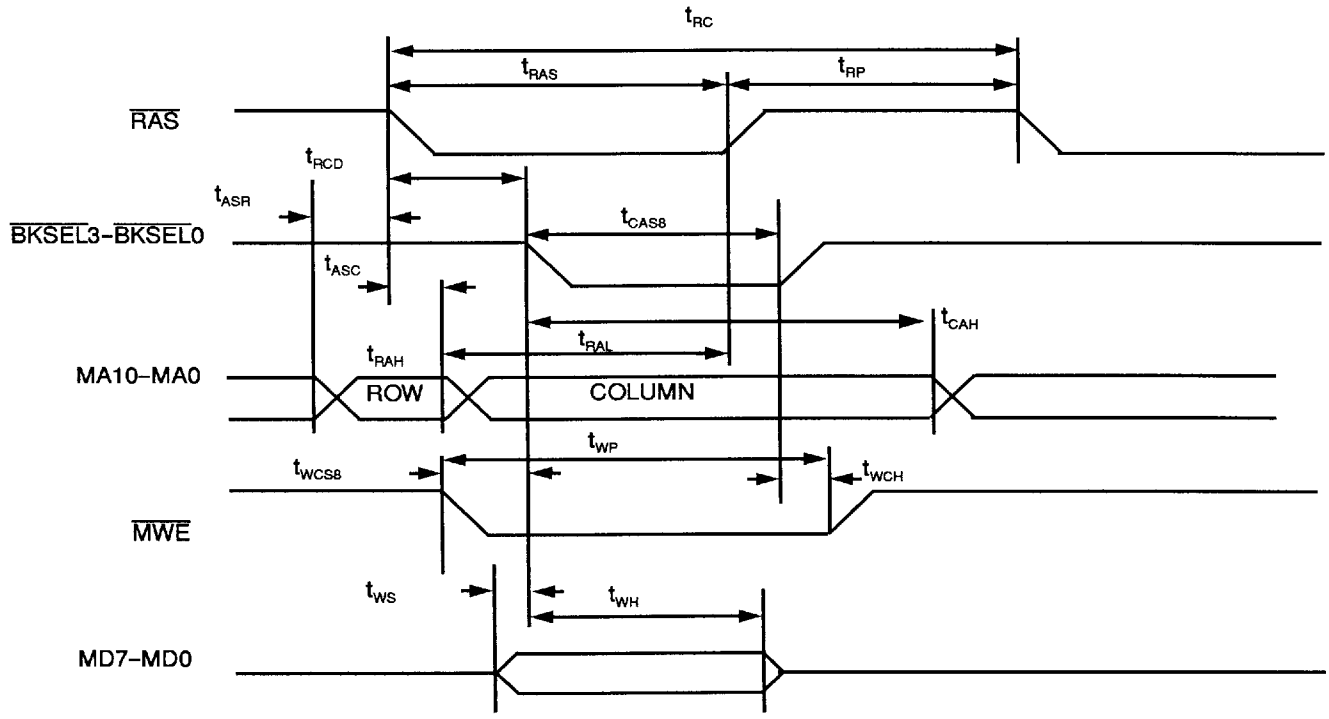

Figure 10. Local Memory: DRAM Write—8 bit

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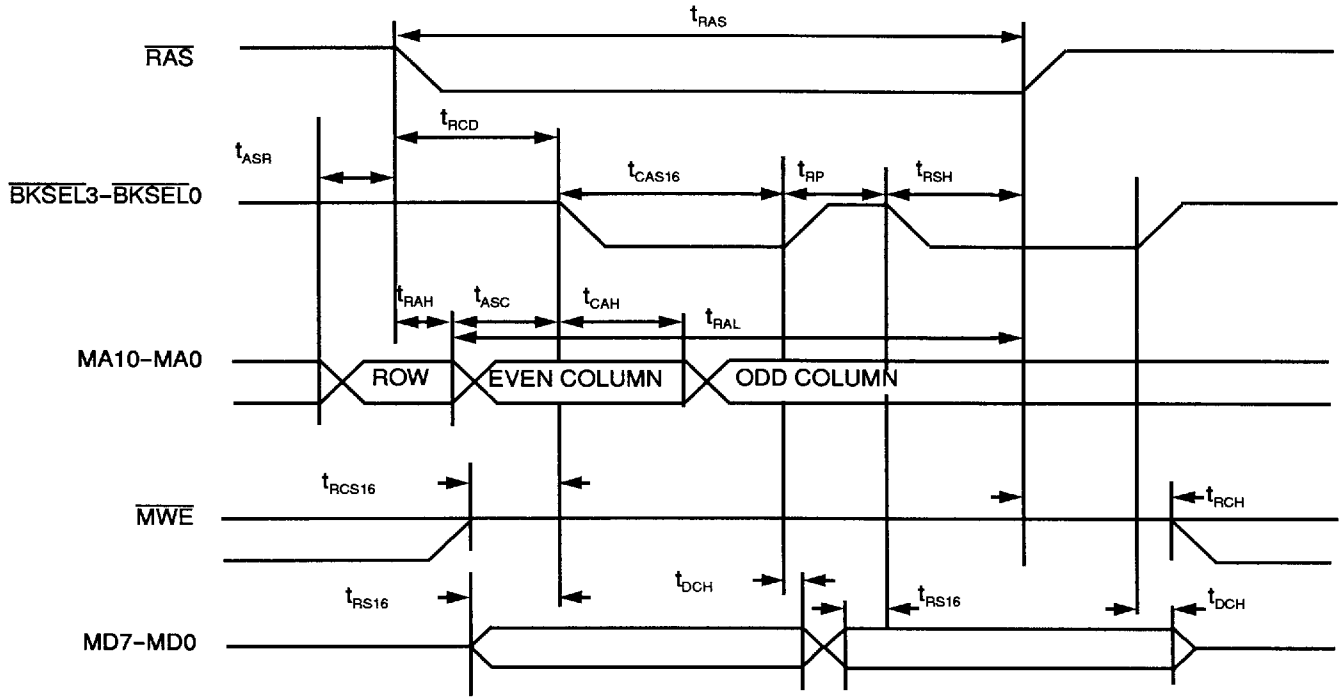

Figure 11. Local Memory: DRAM Read—16 bit

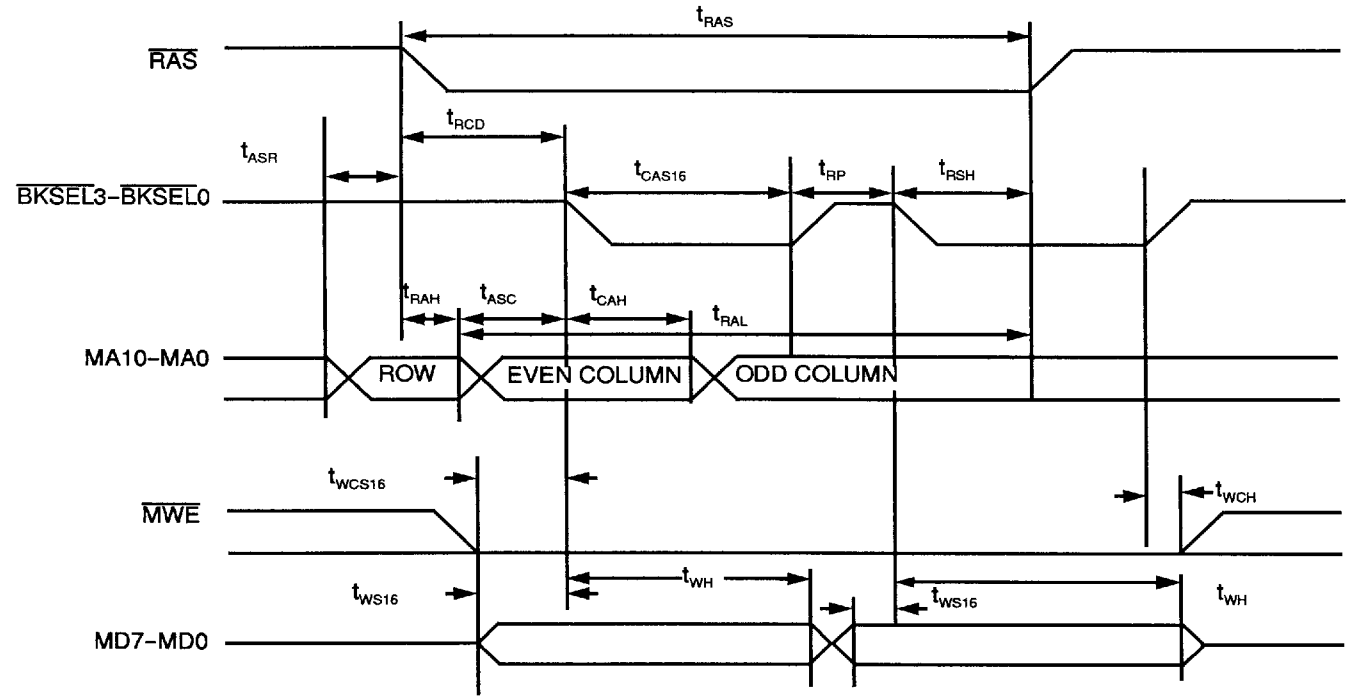

Figure 12. Local Memory: DRAM Write—16 bit

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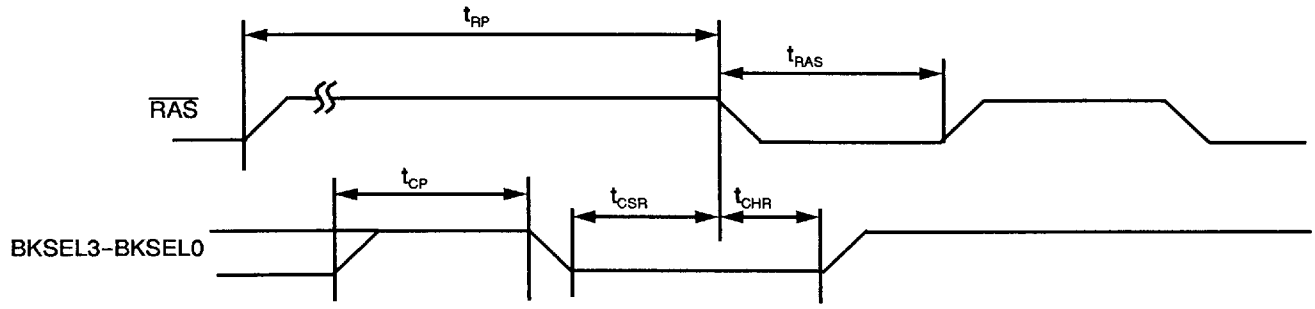

Figure 13. Local Memory: DRAM Refresh ($\overline{CAS}$ Before $\overline{RAS}$)

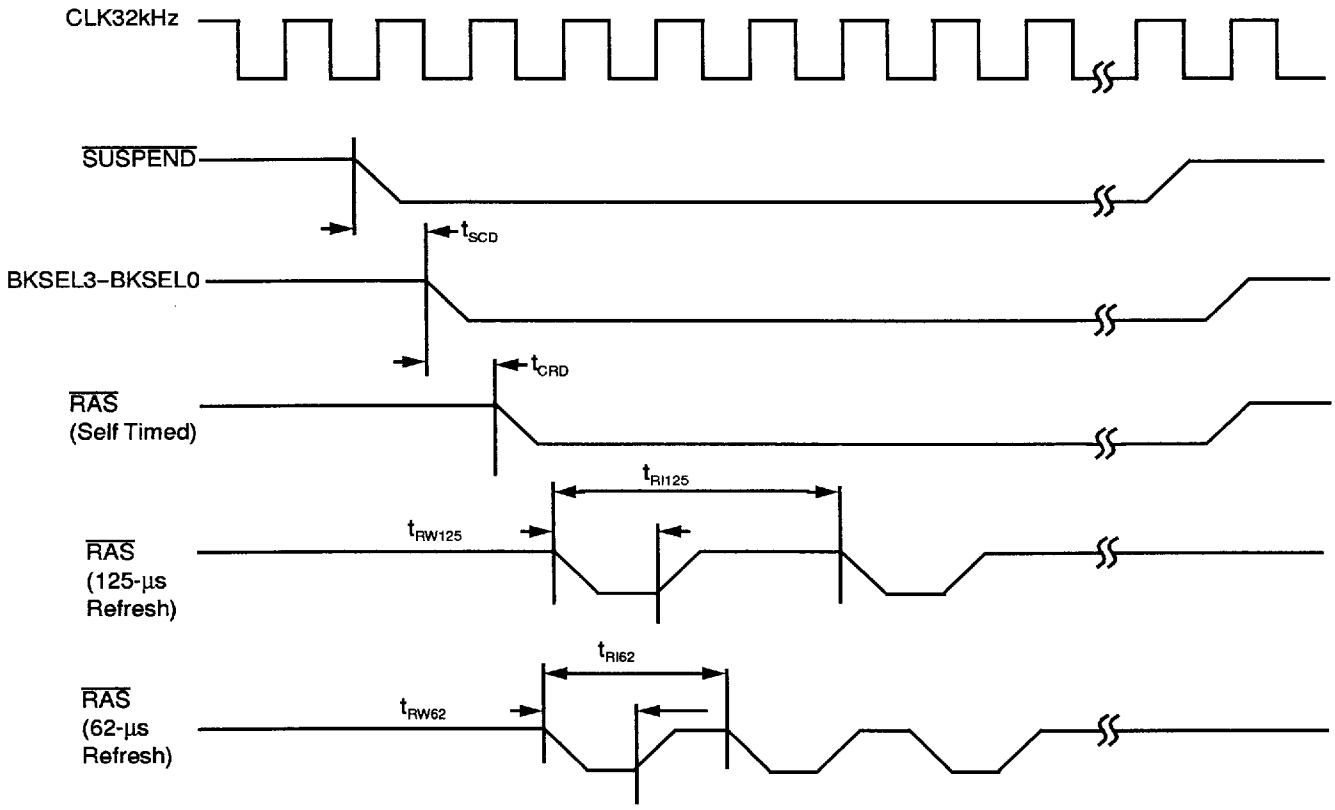

Figure 14. Local Memory: DRAM Refresh (Suspend and Shut Down Modes)

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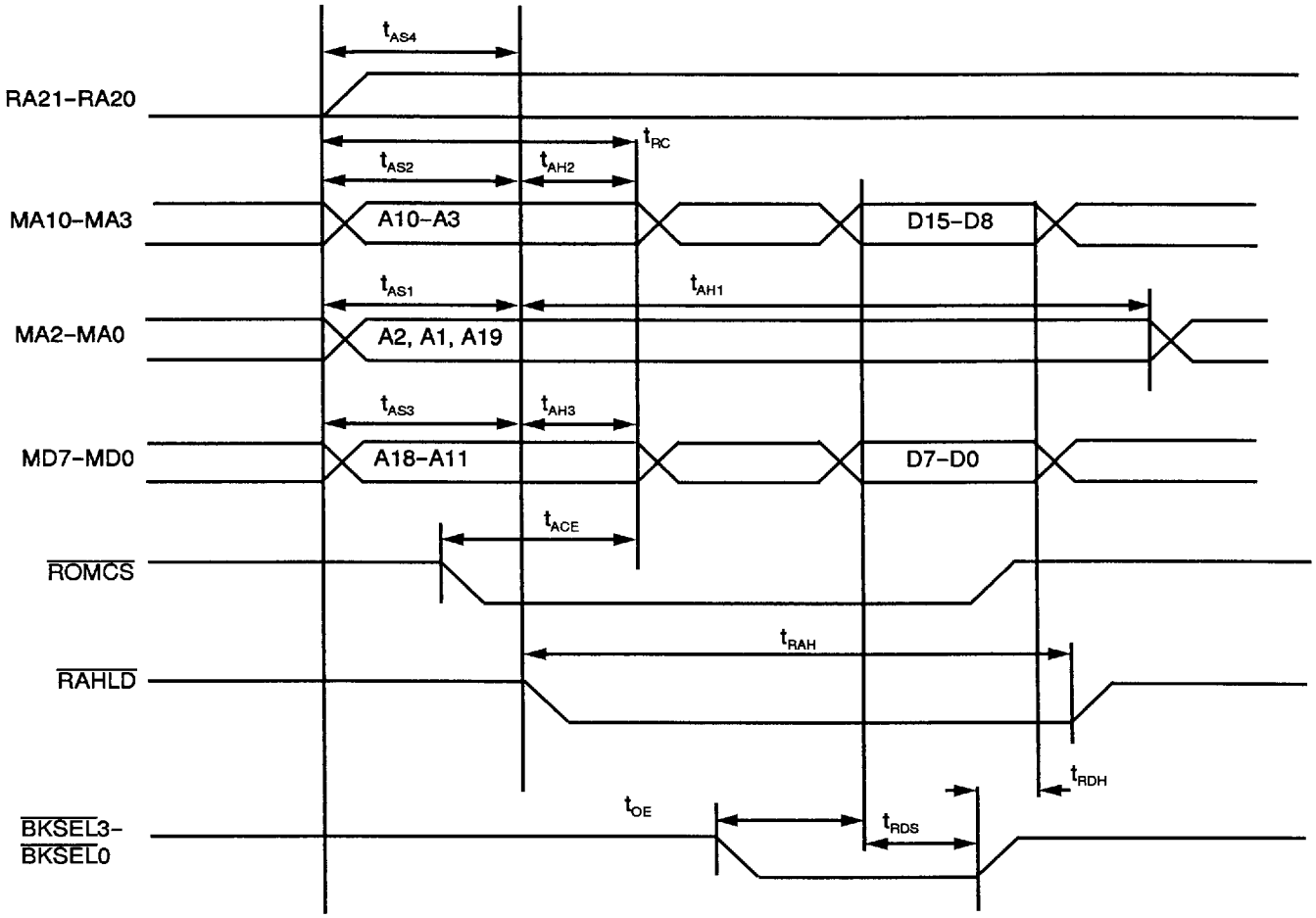

Figure 15. Local Memory: ROM Access

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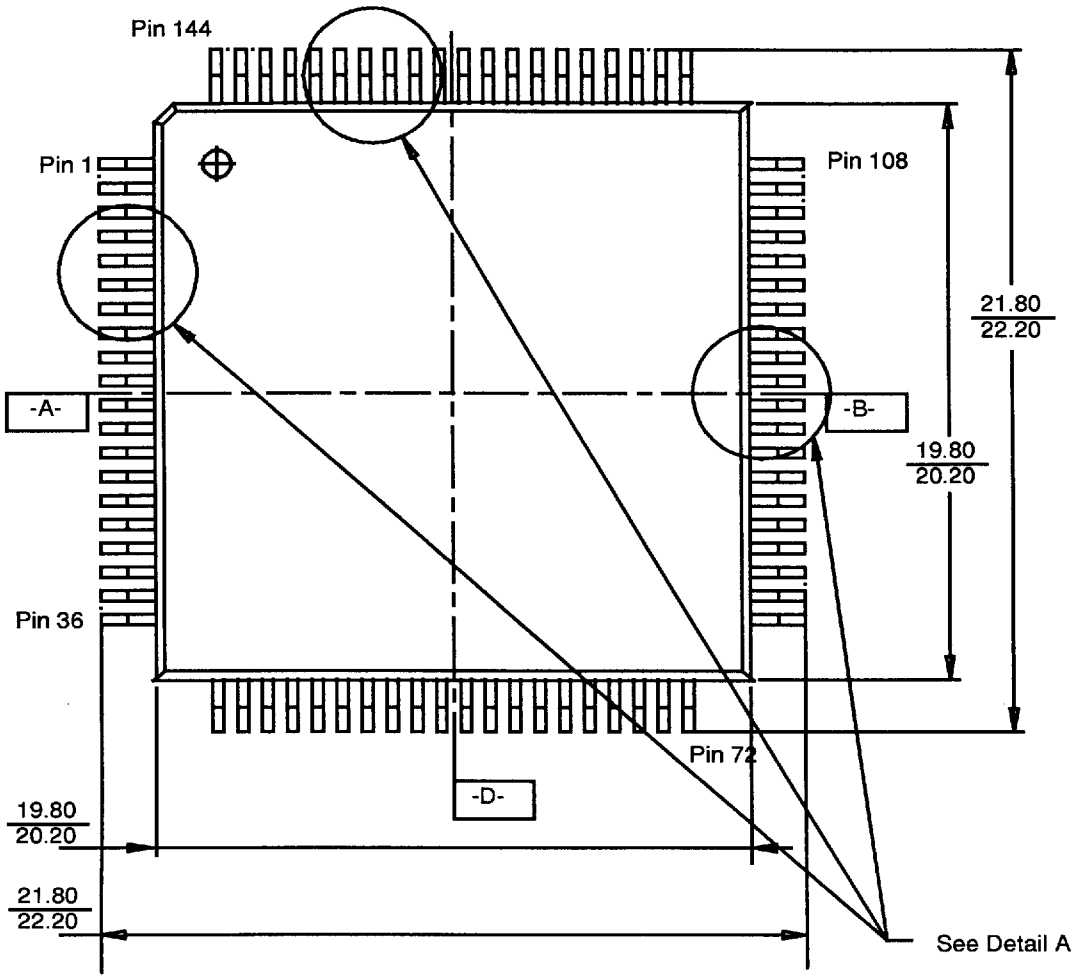
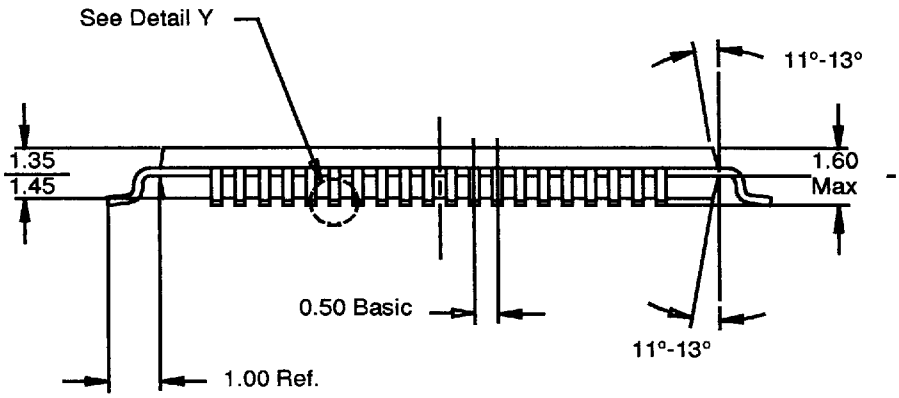
PHYSICAL DIMENSIONS
TQFP 144





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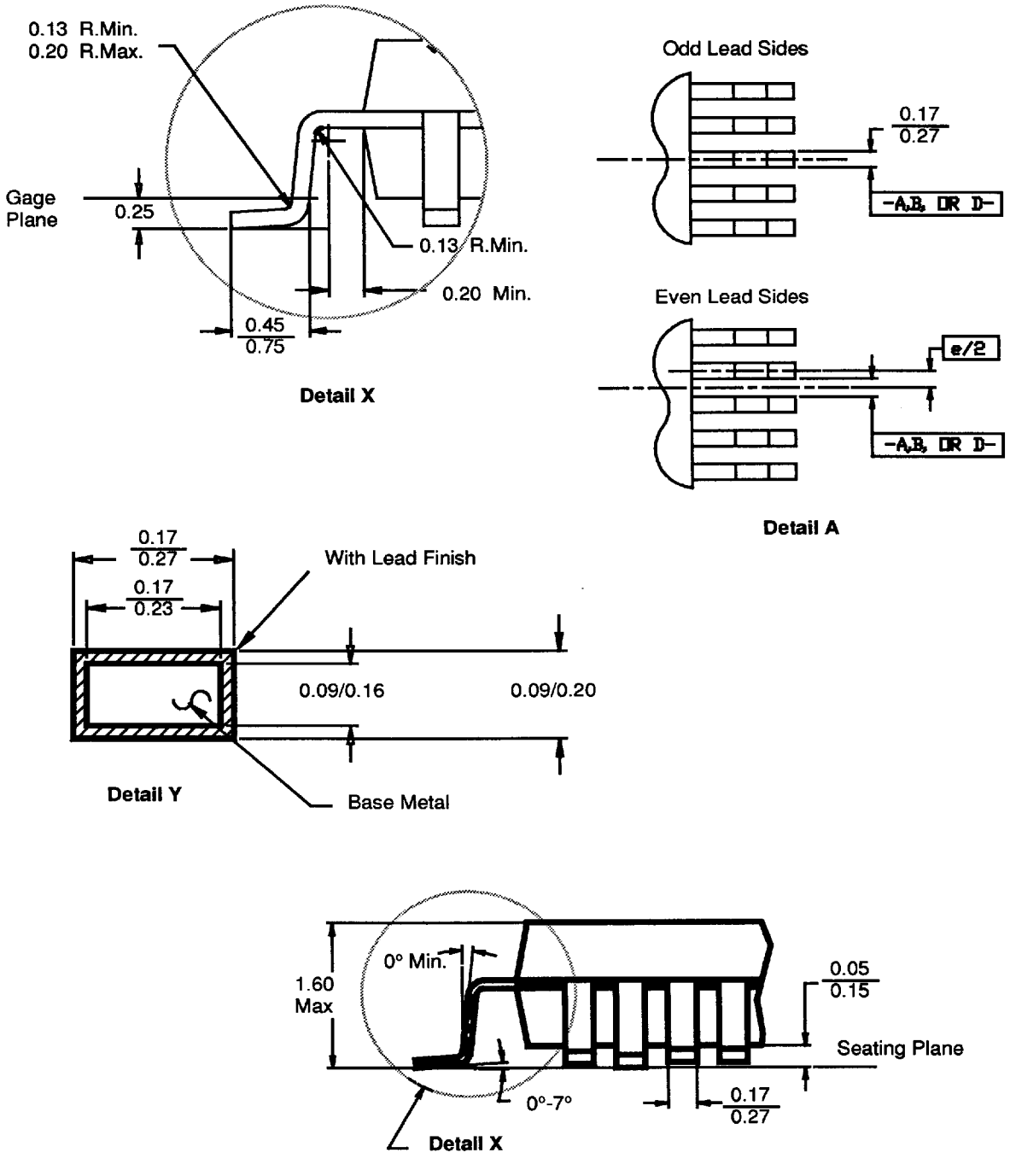
PHYSICAL DIMENSIONS
TQFP 144



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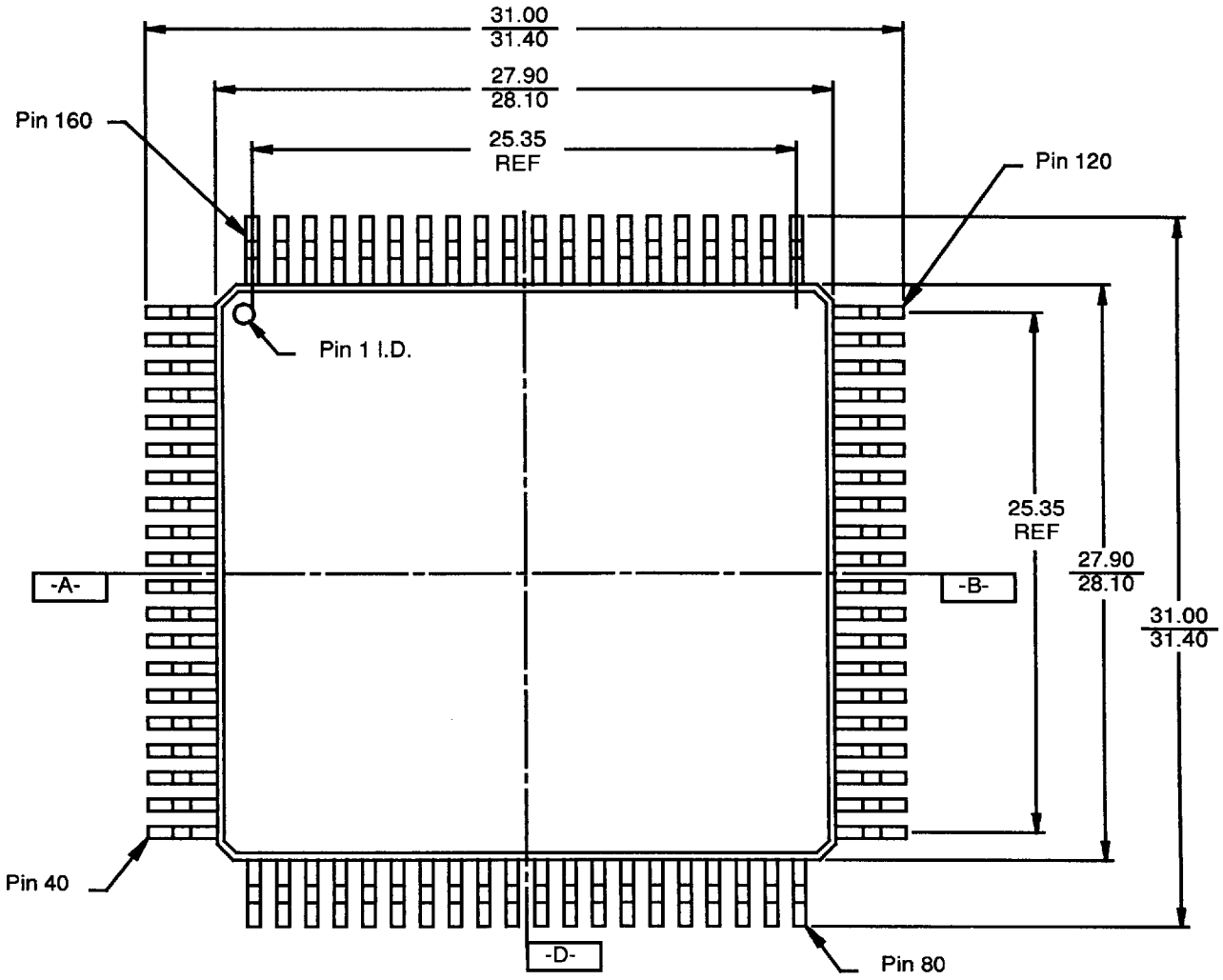
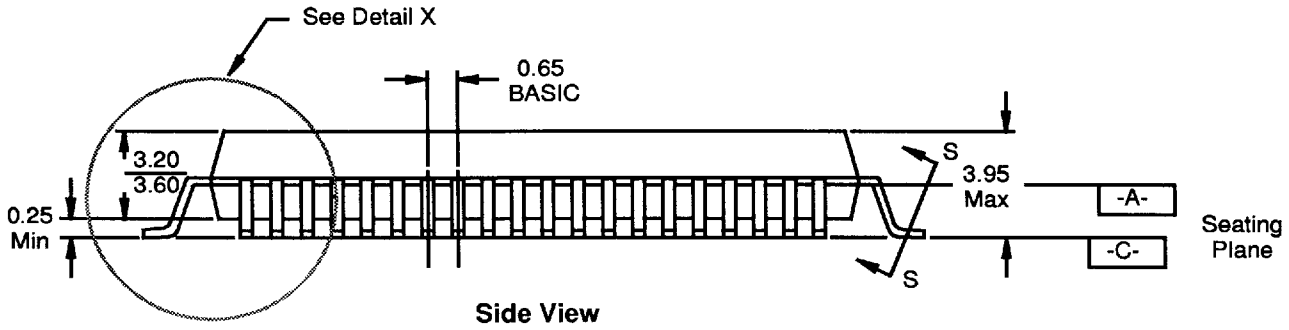
PQR 160, Trimmed and Formed
Plastic Quad Flat Pack



Top View



Side View

Notes:

1. *All measurements are in millimeters unless otherwise noted.*
2. *Not to scale; for reference only.*

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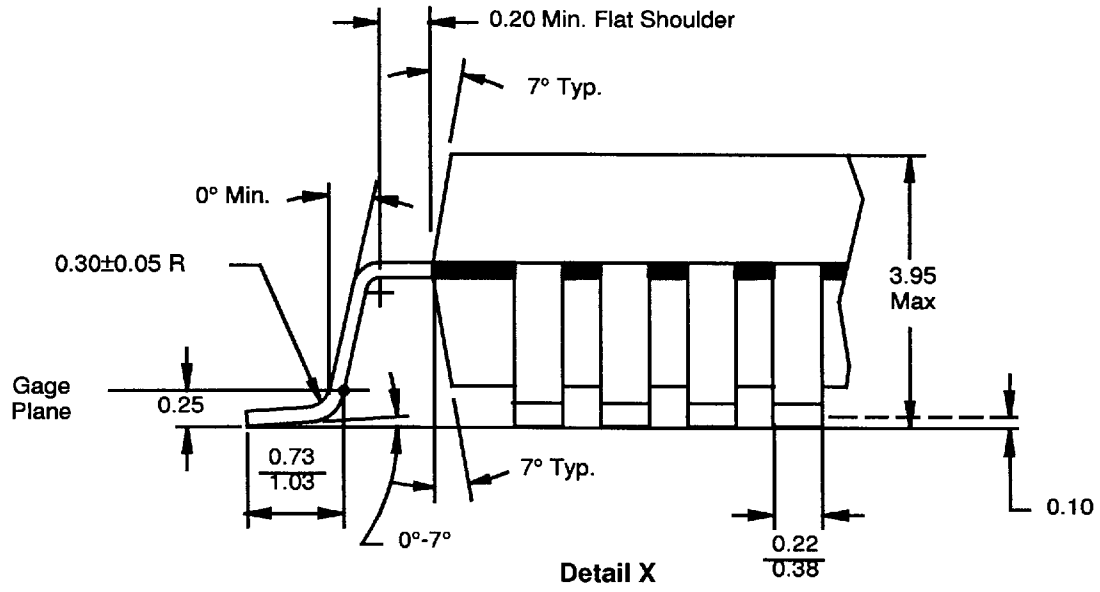
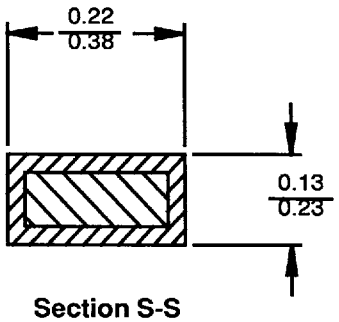
PQR 160 (continued)



Detail X



Section S-S

Note:

1. Not to scale; for reference only.

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