GND_RT VINGND GND_TPVSS GND_A2VSSN GND_AVSSN GND_A2VSSQ GND_AVSSQ GND_MPVSS GND_PVSS GND_R2SET GND_RSET

The following grounds should be routed back to their respective regulators and then tied directly to the ground plane with one via: GND_PVSS, GND_MPVSS, GND_TPVSS, and GND_A2VSSN. The other ground pins (GND_AVSSN, GND_A2VSSQ, GND_RSET, GND_R2SET) should be tied to the ground plane directly through one via as close to the pins as possible without connecting to anything else. If space is an issue it is possible to use one via for two adjacent pins.

+VDDQ_BUS

C2 100uF_6.3V
Biggest footprint

Use 47uF Tant. 16V 20% D size (P/N 4230047600), 800mR Max. ESR and Max. ripple 430mA @ 100kHz
or
100uF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mR Max. ESR and Max. ripple 230mA @ 100kHz
or
47uF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mR Max. ESR and Max. ripple 150mA @ 100kHz

+5V_BUS

C5 DNI/47uF_6.3V >=6.3V

+3.3V_BUS

C8 47uF_6.3V >=6.3V

+12V_BUS

C10 place at the AGP connector
C10 DNI/10uF_20V

MAGP1

	A1	12V	OVRCNT#	B1	
AGP_TYPEDET#	A2	TYPEDET#	5.0V	B2	
AGP_GC_8X_DET#	A3	GC_DET#/RESEVED	5.0V	B3	
	A4	USB-	USB+	B4	
	A5	GND	GND	B5	
	A6	INTA#	INTB#	B6	
	A7	RST#	CLK	B7	
	A8	GNT#	REQ#	B8	AGP_AGP/PCICLK 2, AGP_REQ# 2
	A9	VCC3.3	VCC3.3	B9	
AGP_ST1	A10	ST1	ST0	B10	AGP_ST0, AGP_ST2
	A11	MB_DET#/RESERVED	ST2	B11	
	A12	DBI_HI/PIPE#	RBF#	B12	AGP_RBF# 2
	A13	GND	GND	B13	AGP_DBI_LO 2
	A14	WBF#	DBI_LO/RESERVED	B14	
AGP_SBA1	A15	SBA1	SBA0	B15	AGP_SBA0
	A16	VCC3.3	VCC3.3	B16	
AGP_SBA3	A17	SBA3	SBA2	B17	AGP_SBA2
	A18	SB_STB#	SB_STB	B18	AGP_SB_STB 2
	A19	GND	GND	B19	
AGP_SBA5	A20	SBA5	SBA4	B20	AGP_SBA4
AGP_SBA7	A21	SBA7	SBA6	B21	AGP_SBA6
	A22	KEY	KEY	B22	
	A23	KEY	KEY	B23	
	A24	KEY	KEY	B24	
	A25	KEY	KEY	B25	
	A26	KEY	KEY	B26	
AGP_AD30	A27	AD30	AD31	B27	AGP_AD31, AGP_AD29
AGP_AD28	A28	AD28	AD29	B28	
	A29	VCC3.3	VCC3.3	B29	
AGP_AD26	A30	AD26	AD27	B30	AGP_AD27, AGP_AD25
AGP_AD24	A31	AD24	AD25	B31	
	A32	GND	GND	B32	AGP_AD_STB1 2
AGP_C/BE#3	A33	AD_STB1#	AD_STB1	B33	
	A34	C/BE3#	AD23	B34	AGP_AD23
	A35	VDDQ	VDDQ	B35	
AGP_AD22	A36	AD22	AD21	B36	AGP_AD21
AGP_AD20	A37	AD20	AD19	B37	AGP_AD19
	A38	GND	GND	B38	
AGP_AD18	A39	AD18	AD17	B39	AGP_AD17
AGP_AD16	A40	AD16	C/BE2#	B40	AGP_C/BE#2
	A41	VDDQ	VDDQ	B41	
	A42	FRAME#	IRDY#	B42	AGP_IRDY# 2
	A43	KEY	KEY	B43	
	A44	KEY	KEY	B44	
	A45	KEY	KEY	B45	
	A46	KEY	KEY	B46	
	A47	TRDY#	DEVSEL#	B47	AGP_DEVSEL# 2
	A48	STOP#	VDDQ	B48	
	A49	PME#	PERR#	B49	
	A50	GND	GND	B50	
AGP_AD15	A51	PAR	SERR#	B51	
	A52	AD15	C/BE1#	B52	AGP_C/BE#1
AGP_AD13	A53	VDDQ	VDDQ	B53	
AGP_AD11	A54	AD13	AD14	B54	AGP_AD14, AGP_AD12
	A55	AD11	AD12	B55	
AGP_AD9	A56	GND	GND	B56	AGP_AD10
AGP_C/BE#0	A57	AD9	AD10	B57	AGP_AD8
	A58	C/BE0#	AD8	B58	
	A59	VDDQ	VDDQ	B59	
AGP_AD6	A60	AD_STB0#	AD_STB0	B60	
	A61	AD6	AD7	B61	AGP_AD7
AGP_AD4	A62	GND	GND	B62	AGP_AD5
AGP_AD2	A63	AD4	AD5	B63	AGP_AD3
	A64	AD2	AD3	B64	
AGP_AD0	A65	VDDQ	VDDQ	B65	AGP_AD1
	A66	AD0	AD1	B66	AGP_AGPREF
		VREFGC	VREFCG		

UNIVERSAL_AGP_BUS

AGP_SBA[7..0] AGP_ST[2..0] AGP_C/BE#[3..0] AGP_AD[31..0]

2 AGP_INTR#
2 AGP_GNT#
2 AGP_WBF#
2 AGP_SB_STB#
2 AGP_MB_8X_DET#
2 AGP_DBI_HI

R83 0R

+5V_BUS
C11 100nF X7R

2,12 AGP_RESET#
R3 100R
R4 180R
U6A SN74ACT86D
COMMON

2 AGP_AD_STB1#
2 AGP_FRAME#
2 AGP_TRDY#
2 AGP_STOP#
2 AGP_PAR
2 AGP_AD_STB0#

R86 0R

AGP_VREFGC

AGP_TYPEDET#
R19 0R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET#
R81 0R

+12V_BUS
J1
1
2
WAFER 2-PIN

+3.3V_BUS
R90 47K
U6D SN74ACT86D
AGP_MB_8X_DET#
TEST
R91 1K

R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

+VDDQ_BUS
2N7002E Q10
R92 147R_1%
R_AGP8X
R93 332R_1%
R94 100R_1%
C19 10nF

+VDDQ_BUS
R88 169R_1%
Q9 2N7002E
TEST
R89 71.5R_1%
AGP_AGPTEST
AGP_AGPTEST 2

AGP_AGPREF
AGP_VREFGC
R84 DNI/0R
R85 DNI/0R
Keep stubs short

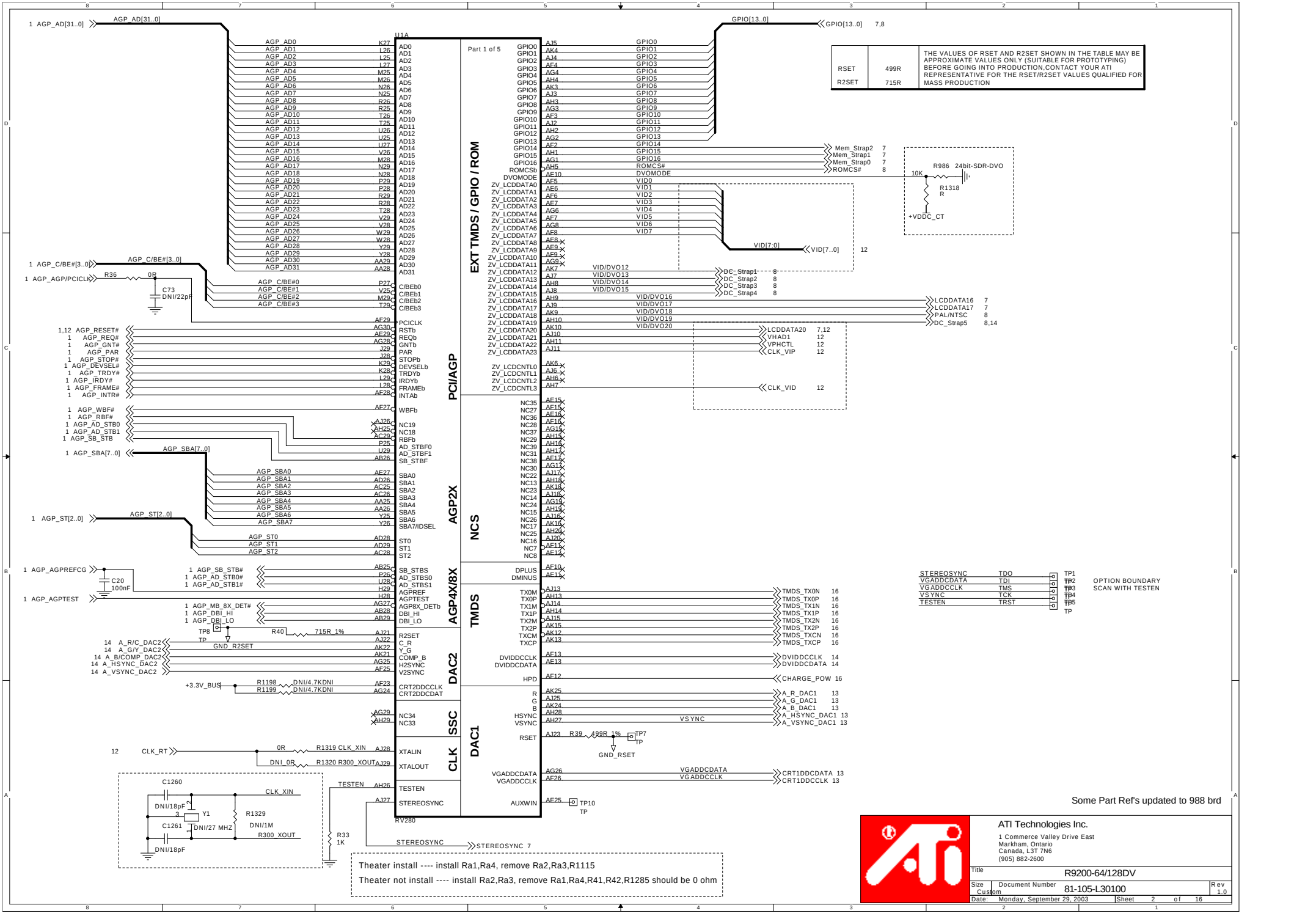
R_AGP8X must be 1% resistor to provide 350mV +/- 5% on Vref

+VDDQ_BUS
2N7002E Q11
TEST
R95 147R_1%
R_AGP8X
R96 332R_1%
R97 100R_1%
C21 10nF
AGP_AGPREFCG 2

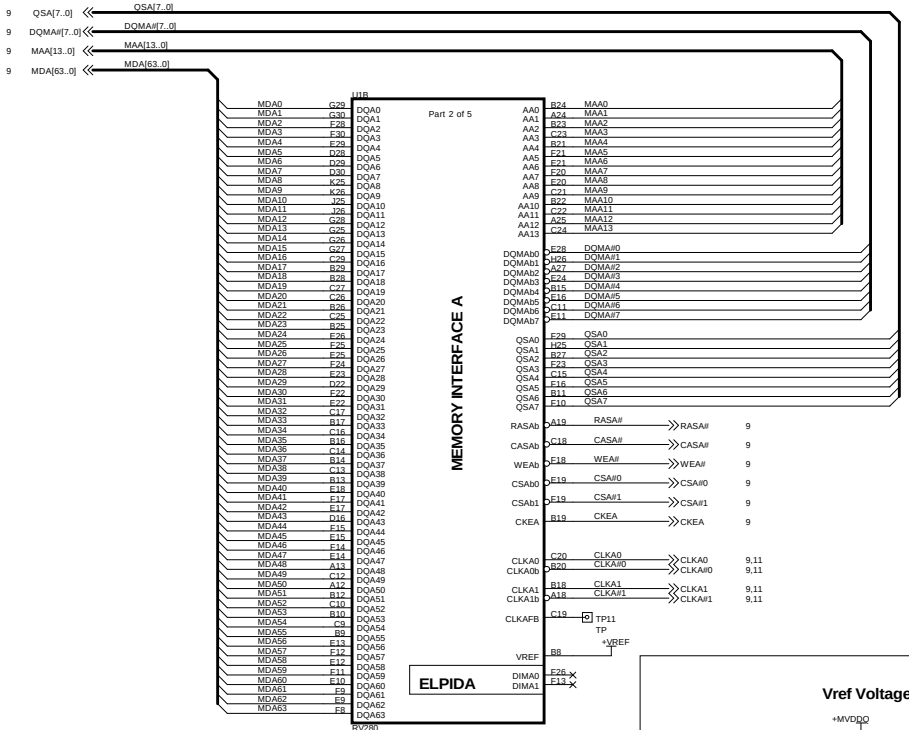
UNIVERSAL VREFGC CIRCUIT (2X, 4X, 8X)

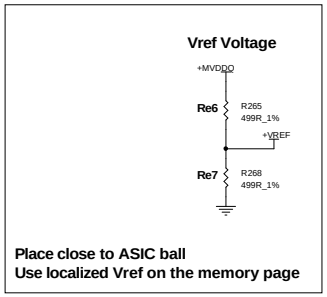
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV		
Size	Document Number		Rev
Custom	81-105-L30100		1.0
Date:	Monday, September 29, 2003	Sheet 1 of 16	

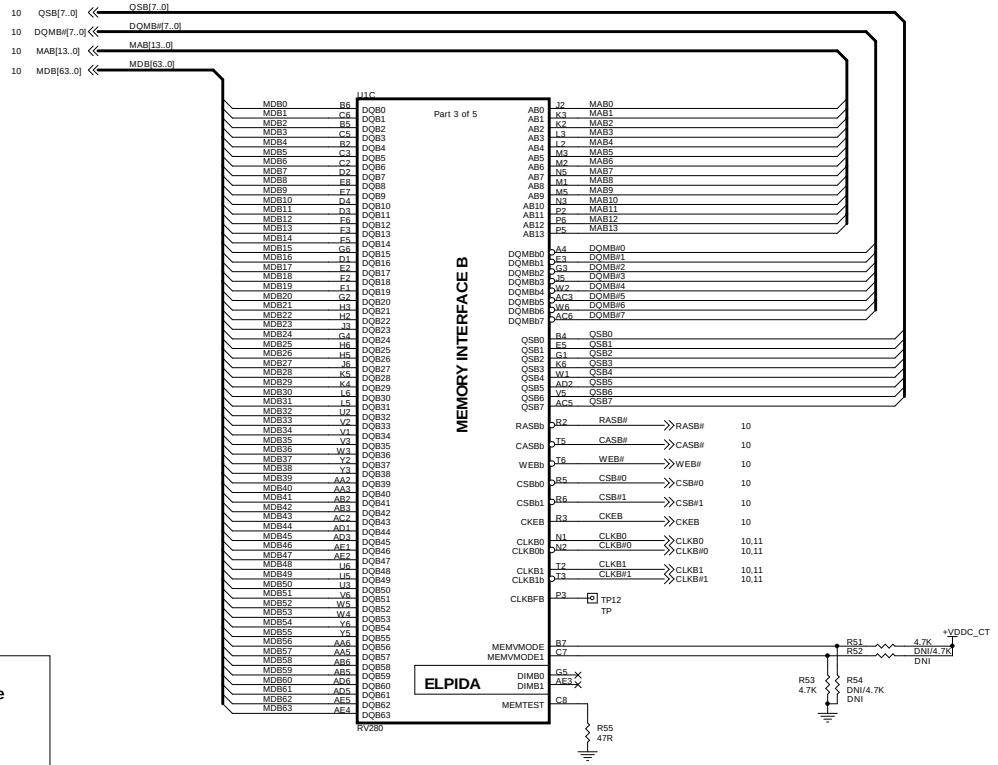

U1A
Part 1 of 5
RV280
PCI/AGP
AGP2X
NCS
AGP4X/8X
TMDS
DAC2
SSC
CLK
DAC1
EXT TMDS / GPIO / ROM
AGP_AD[31..0]
AGP_C/BE#[3..0]
AGP_SBA[7..0]
AGP_ST[2..0]
GPIO[13..0]
VID[7..0]
R36 0R
C73 DNI/22pF
C20 100nF
R40 715R 1%
R1198 DNI/4.7KDNI
R1199 DNI/4.7KDNI
R39 499R 1%
R1319 CLK_XIN
R1320 R300_XOUT
C1260 DNI/18pF
C1261 DNI/18pF
Y1 DNI/27 MHZ
R1329 DNI/1M
R33 1K
R986 24bit-SDR-DVO
10K
R1318 R
+VDDC_CT
+3.3V_BUS
GND_R2SET
GND_RSET
TP8
TP7
TP10
TP
RSET 499R
R2SET 715R
THE VALUES OF RSET AND R2SET SHOWN IN THE TABLE MAY BE APPROXIMATE VALUES ONLY (SUITABLE FOR PROTOTYPING) BEFORE GOING INTO PRODUCTION,CONTACT YOUR ATI REPRESENTATIVE FOR THE RSET/R2SET VALUES QUALIFIED FOR MASS PRODUCTION
STEREOSYNC TDO TP1
VGADDCDATA TDI TP2
VGADDCCLK TMS TP3
VSYNC TCK TP4
TESTEN TRST TP5
OPTION BOUNDARY SCAN WITH TESTEN
Theater install ---- install Ra1,Ra4, remove Ra2,Ra3,R1115
Theater not install ---- install Ra2,Ra3, remove Ra1,Ra4,R41,R42,R1285 should be 0 ohm
Some Part Ref's updated to 988 brd
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600
Title R9200-64/128DV
Size Custom
Document Number 81-105-L30100
Rev 1.0
Date: Monday, September 29, 2003
Sheet 2 of 16

MEMORY CHANNEL A





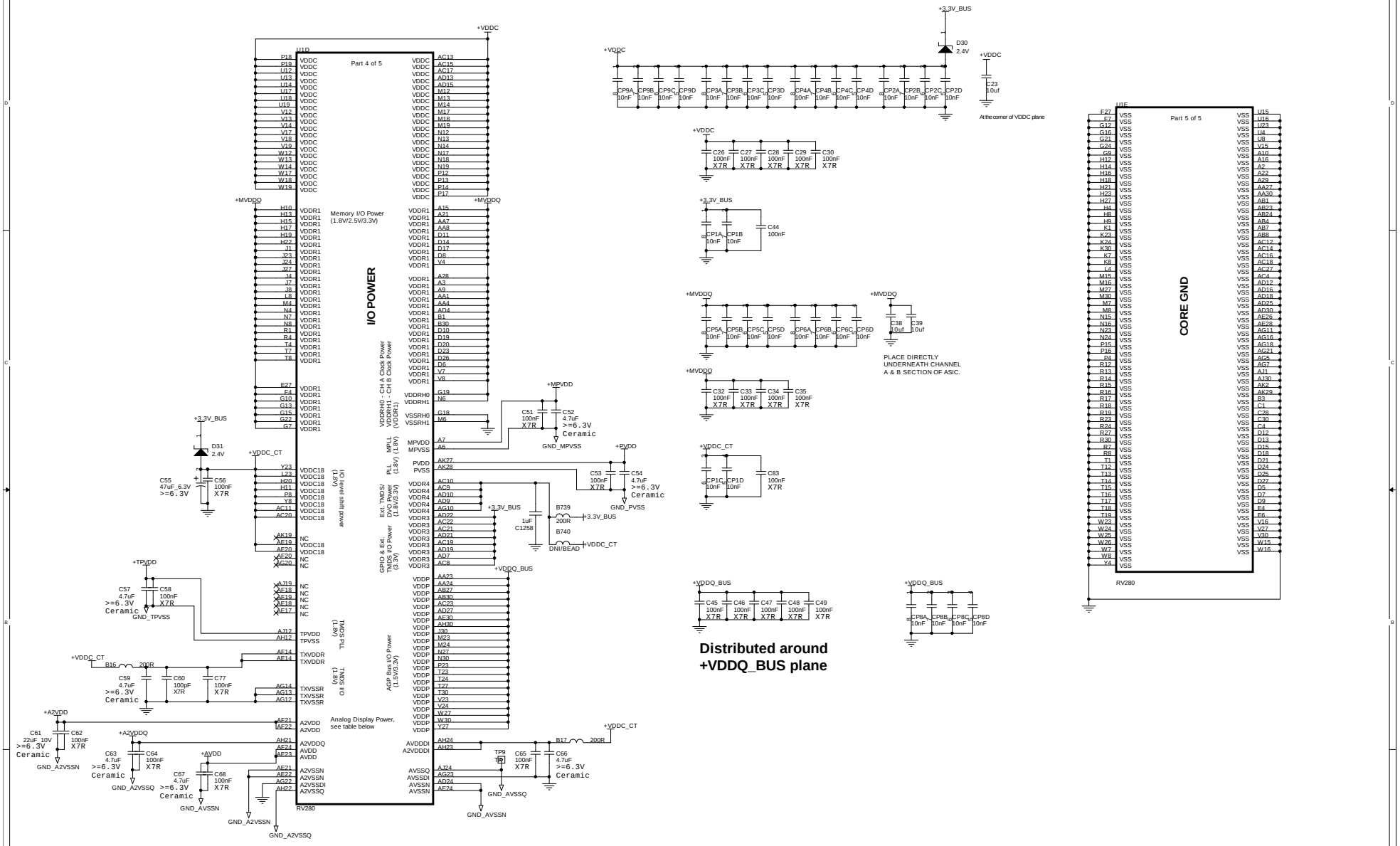
MEMORY CHANNEL B



MEMVMODE[1:0]	MEMORY IO VOLTAGE	
01	2.5V (DDR)	Default
1 0	1.8V (DDR)	
11	3.3V (SDR)	

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV	
Size: Custom	Document Number: 81-105-L30100	Rev: 1.0
Date: Monday, September 29, 2003	Sheet 3 of 16	



Pin Names	+AVDD	Matching Ground	+A2VDD	Matching Ground	+A2VDDQ	Matching Ground	+AVDDDI +A2VDDDI	Matching Ground
Voltage	1.8V		2.5V		1.8V		1.8V	
Usage	DAC1 VDD (80mA)	AVSSN (Noisy)	DAC2 VDD (120mA)	A2VSSN (Noisy)	DAC2 Band Gap Ref	A2VSSQ (Quiet)	Digital Power for DAC1 and DAC2	AVSSDI A2VSSDI (Digital)
	DAC1 Band Gap Ref	AVSSQ (Quiet)						
Board power and ground option(s)	AVDD sourced from VDDC_CT thru bead at least 15 mil trace and not longer than 1.5 inch. AVSSN and AVSSQ with single via to GND close to the pin.		(1) A2VDD regulated source and A2VSSN return path routed with at least 15 mil trace and not longer than 1.5 inch. AVSSN with single via to GND at the regulator. (2) Sourced from VDD thru bead instead of the regulator		Source from AVDD thru bead. A2VSSQ with sigle via to GND close to the pin.		Source from VDDC_CT thru bead	

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

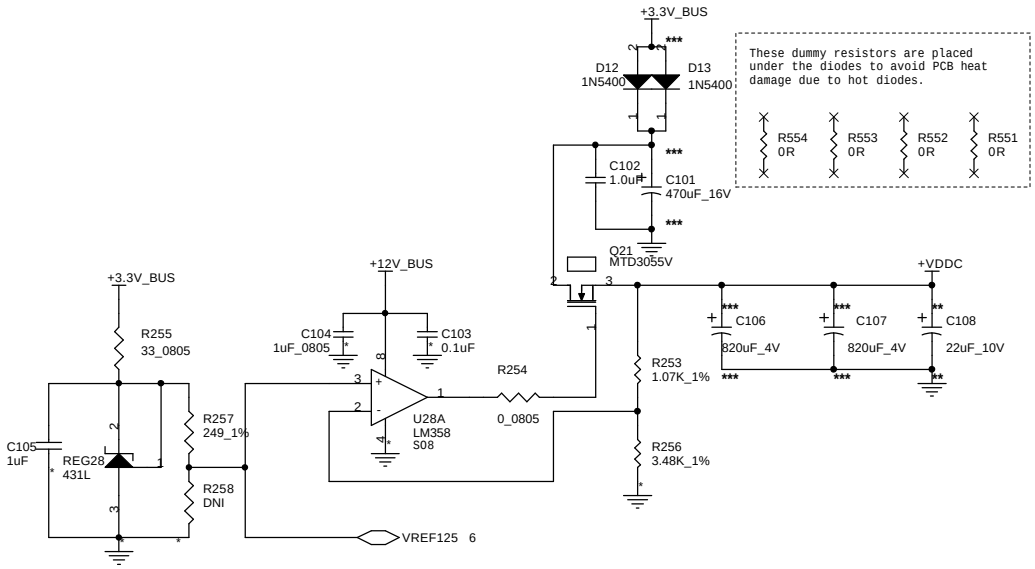
Title	R9200-64/128DV		
Size: Custom	Document Number: 81-105-L30100		Rev: 1.0
Date: Monday, September 29, 2003	Sheet 4 of 16		

Regulator for VDDC (ASIC Core)

Vin = 3.3V AGP
Vout = 1.5V ~ 1.62V
Iout = 4A MAX (load consumption)
Iout = 2.5A MAX (Power rail consumption)

Cout1 470uF thru hole capacitor (P/N 4051047700) has 30mR ESR where as 470uF SMT (P/N 4262047700) capacitor has 150mR ESR. For current below 4.5A, 1 thru 470uF is enough.

*** Indicate number of via required for the connection



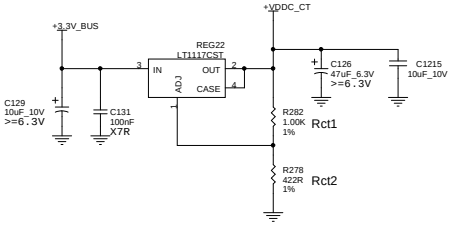
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128TD	
Size B	Document Number 81-105-L30100	Rev 1.0
Date: Monday, September 29, 2003	Sheet 5 of 16	

Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD

Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

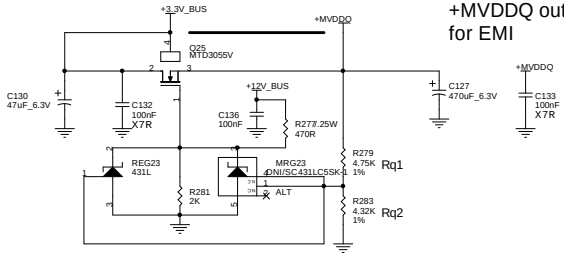
	Rct1		Rct2		
1.8V	1K	3240100100 603	422R	3240422000	603
1.9V			499R	3240499000	603



Regulator for MVDDQ (MEM IO) and VDDR1

Vin = 3.3V AGP
Vout = 2.5V (TSOP)
Iout = 1200mA MAX
Iout = 1000mA Est. MAX

Q25 Pin2/4 should be soldered to board for heat dissipation and a GND fill area.

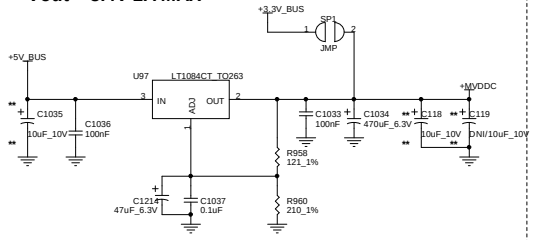


Placed close to +MVDDQ output for EMI

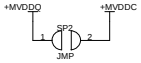
Regulator for MVDDC

Vin = 5V

Vout = 3.4V 2A MAX

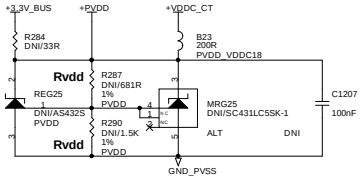


Placed close to +VDDC output for EMI



Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 30mA MAX (PVDD + TPVDD)



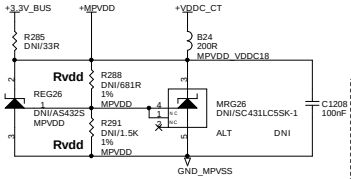
The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX

(Optional)

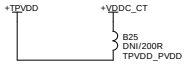


Regulator For TPVDD (TMDS PLLs)

Vin = +3.3V AGP
Vout = 1.8V
Iout = 15mA MAX

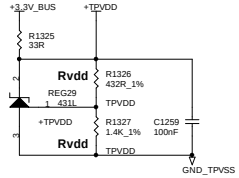
TPVDD might not be needed if PVDD can provide stable 1.8V

(Optional)



Regulator for TPVDD (TMDS PLLs)

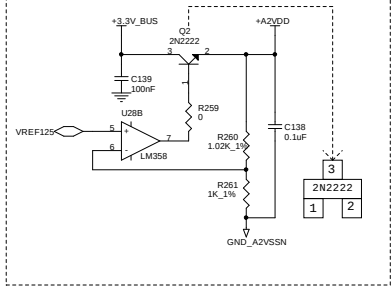
Vin = 3.3V AGP
Vout = +1.62V
Iout = 10mA MAX
15mA Estimeatd MAX



Regulator For A2VDD (2nd DACs)

Vin = +3.3V AGP
Vout = 2.5V
Iout = 150mA MAX

A2VDD might not be needed if VDD can provide stable 2.5V



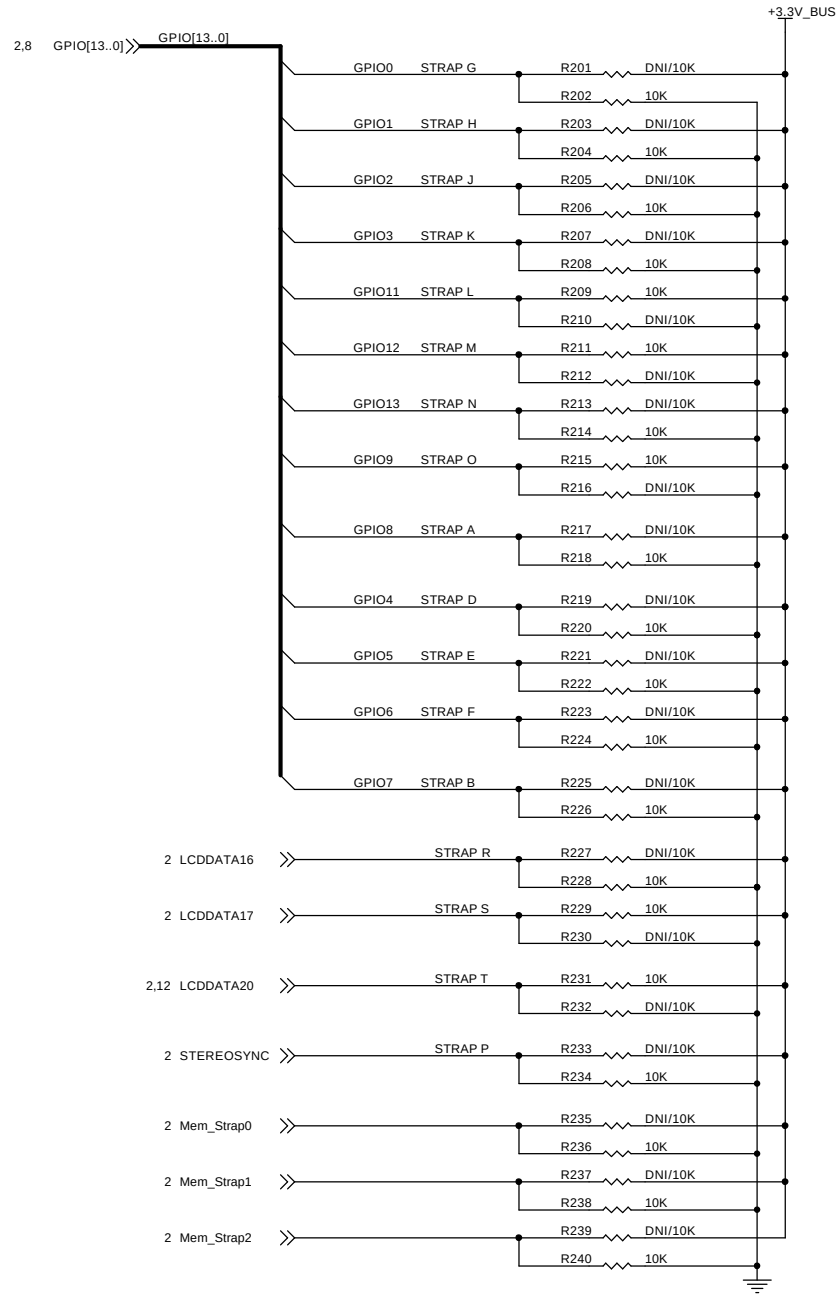
A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signle via to GND at the regulator

AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)

Some Part Ref's updated to 988 brd

<Variant Name>
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV
Size: Custom	Document Number: 81-105-L30100 Rev 1.0
Date: Monday, September 29, 2003	Sheet 6 of 16



OPTION STRAPS

STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) **00 - refclk slightly earlier then feedback** 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM **1011 - Serial M25P05/10 ROM (ST), chip IDis from ROM** 1100 - Reserved 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1100
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
VGA_DISABLE	GPIO(7)	**0 - VGA controller capabillity enabled.** 1 - The device will not be recognized as the systemis VGA controller.	0
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function **10 - two function device. AGP only in function 0** 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	10
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. **0 - Slave VIP host port devices present** 1 - No slave VIP host port devices reporting presence during reset	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

<Variant Name>

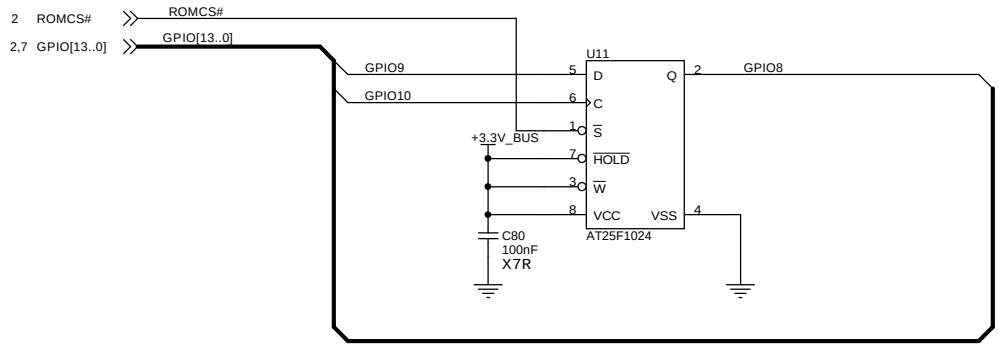
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title: R9200-64/128DV

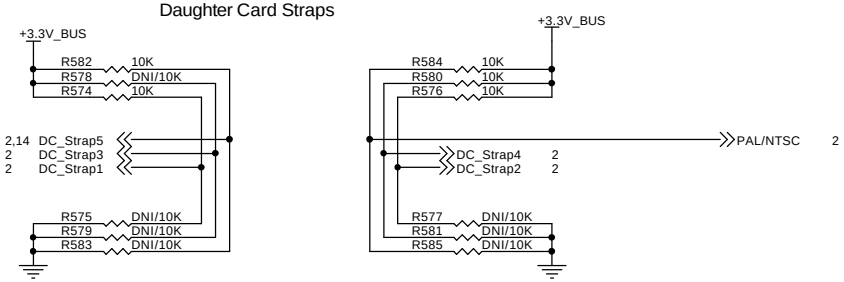
Size: B | Document Number: 81-105-L30100 | Rev: 1.0

Date: Monday, September 29, 2003 | Sheet 7 of 16

SERIAL EEPROM BIOS



Daughter Card Straps

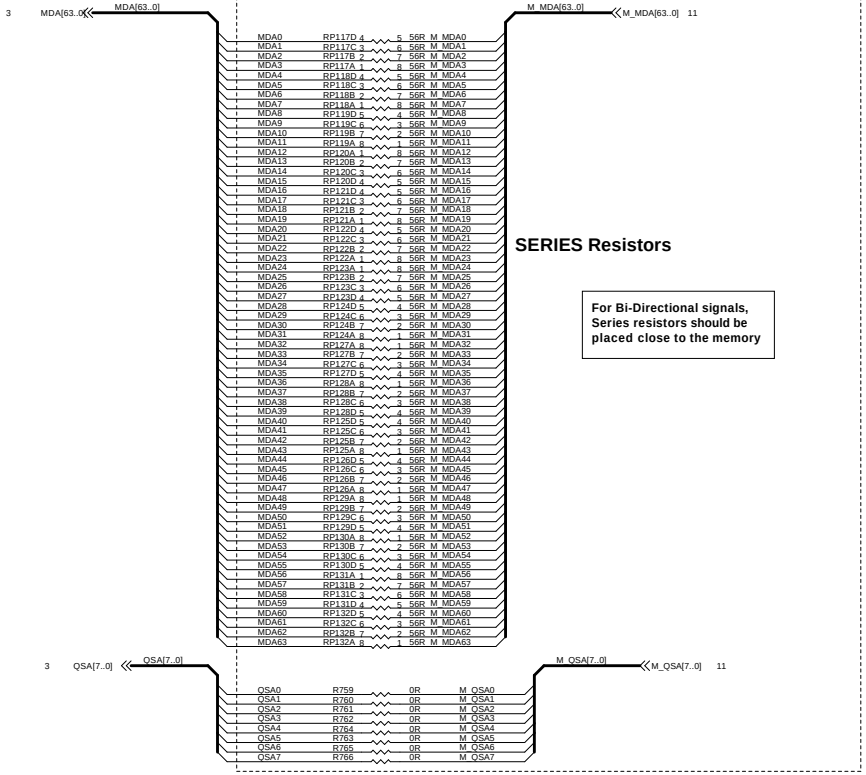


STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)

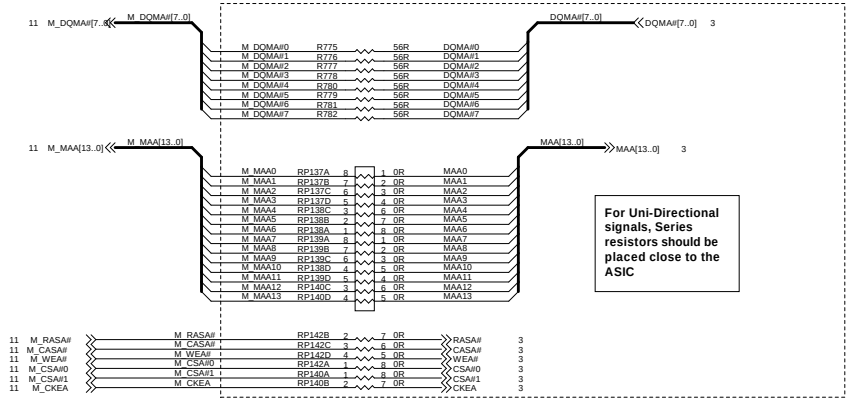
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV	
Size B	Document Number 81-105-L30100	Rev 1.0
Date: Monday, September 29, 2003	Sheet 8 of 16	

TERMINATION FOR MEMORY CHANNEL A



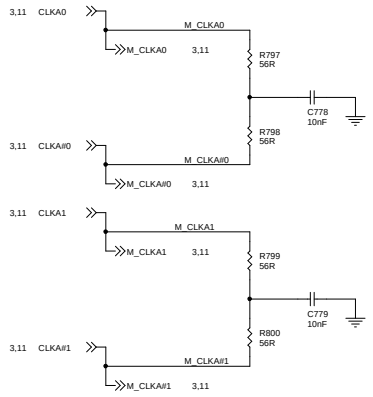
Proper Termination of QSA?



CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



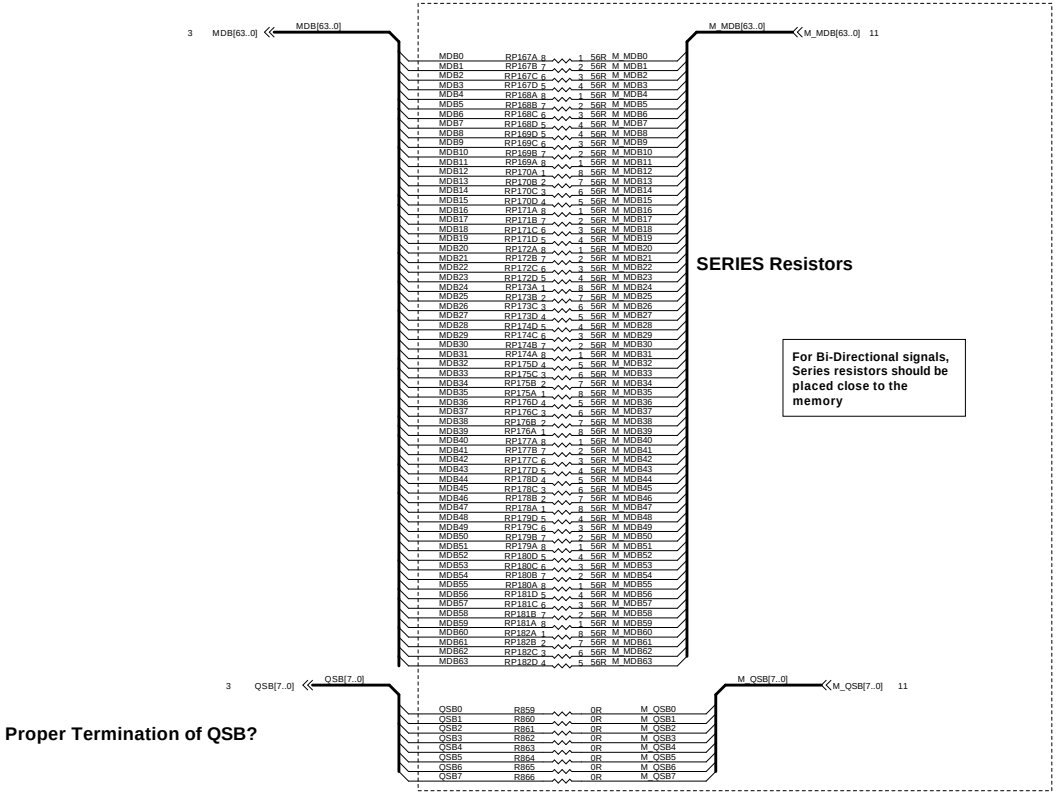
<Variant Name>

ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV		
Size: Custom	Document Number: 81-105-L30100		Rev: 1.0
Date: Monday, September 29, 2003	Sheet 9 of 16		

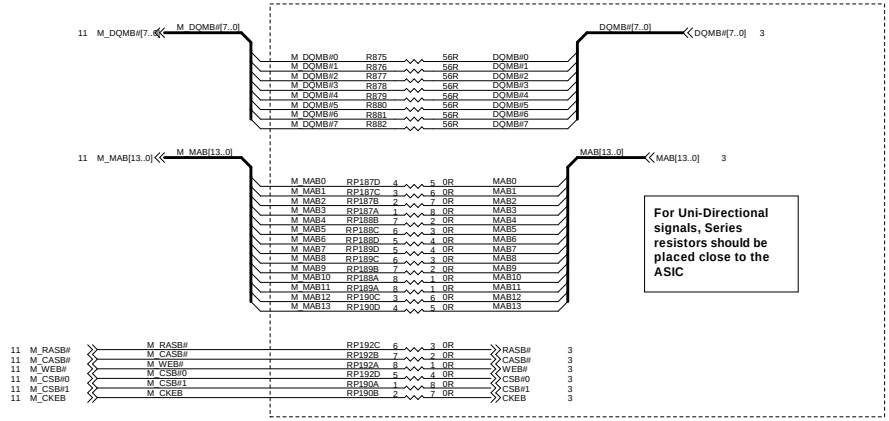
TERMINATION FOR MEMORY CHANNEL B



SERIES Resistors

For Bi-Directional signals, Series resistors should be placed close to the memory

Proper Termination of QSB?

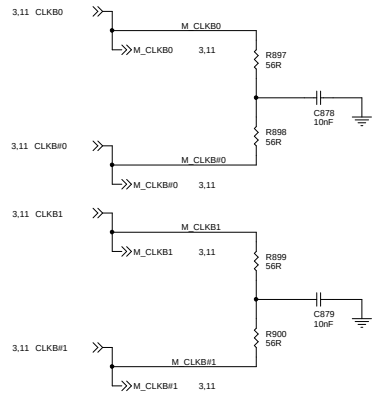


For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory

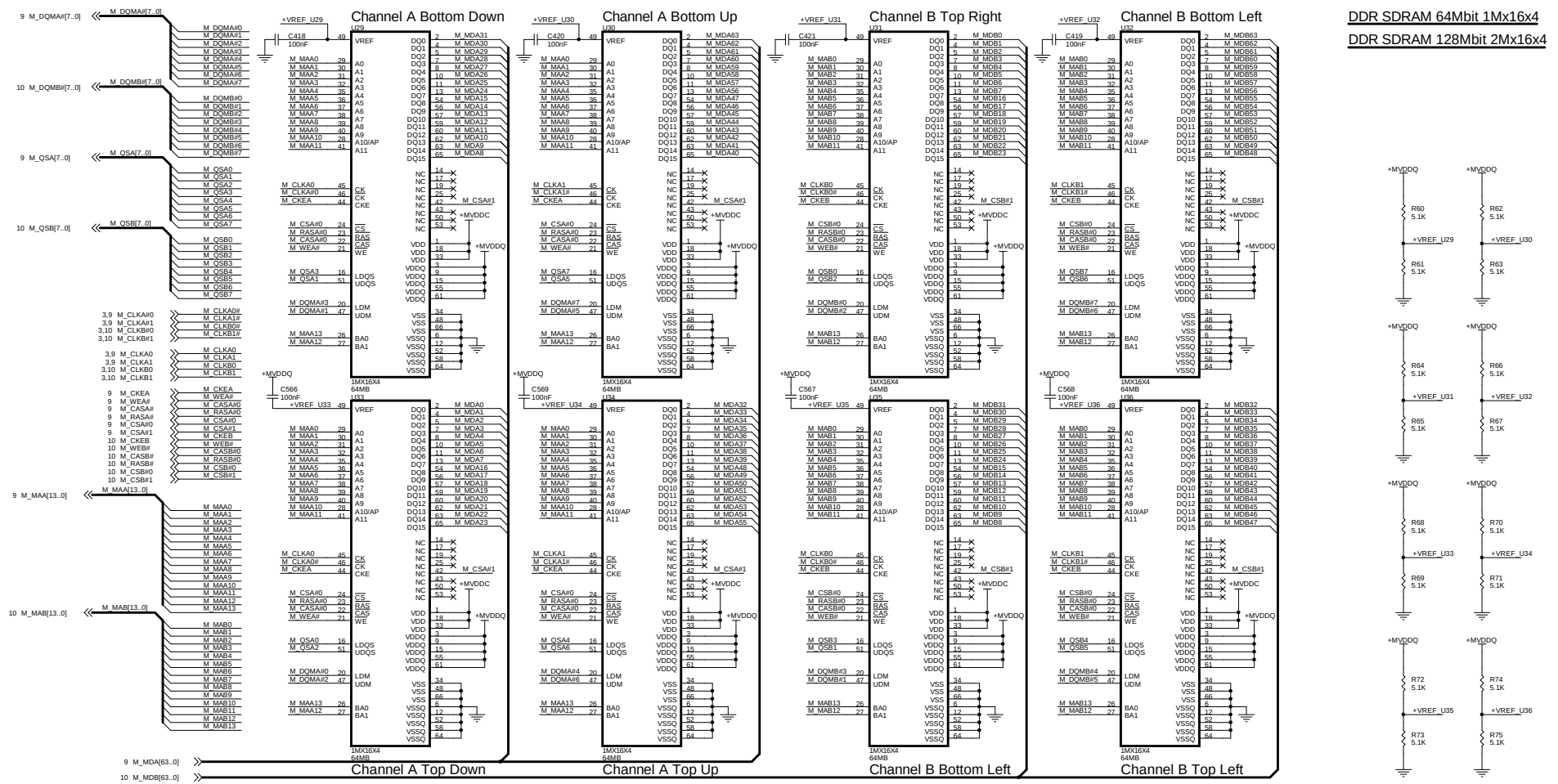


<Variant Name>

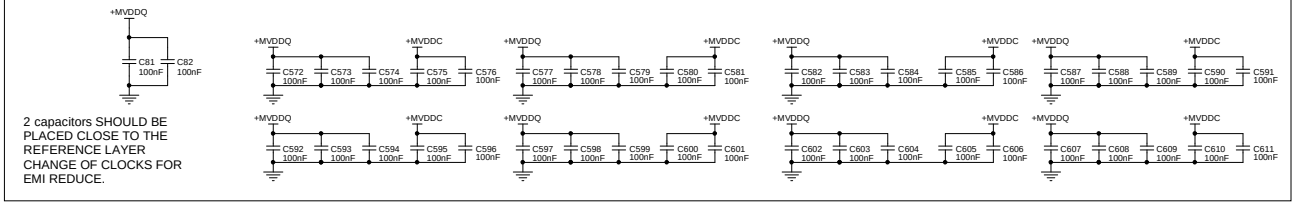
ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV		
Size C	Document Number 81-105-L30100		Rev 1.0
Date: Monday, September 29, 2003	Sheet 10 of 16		

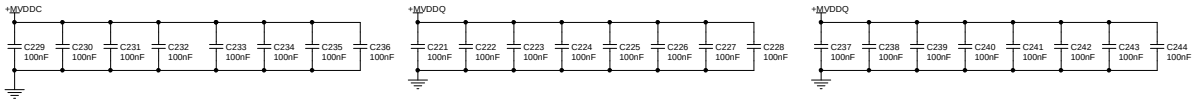


Put 1 1uF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



Part number for 8Mx16: 2354274204 (Samsung)

DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD_MEM_IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

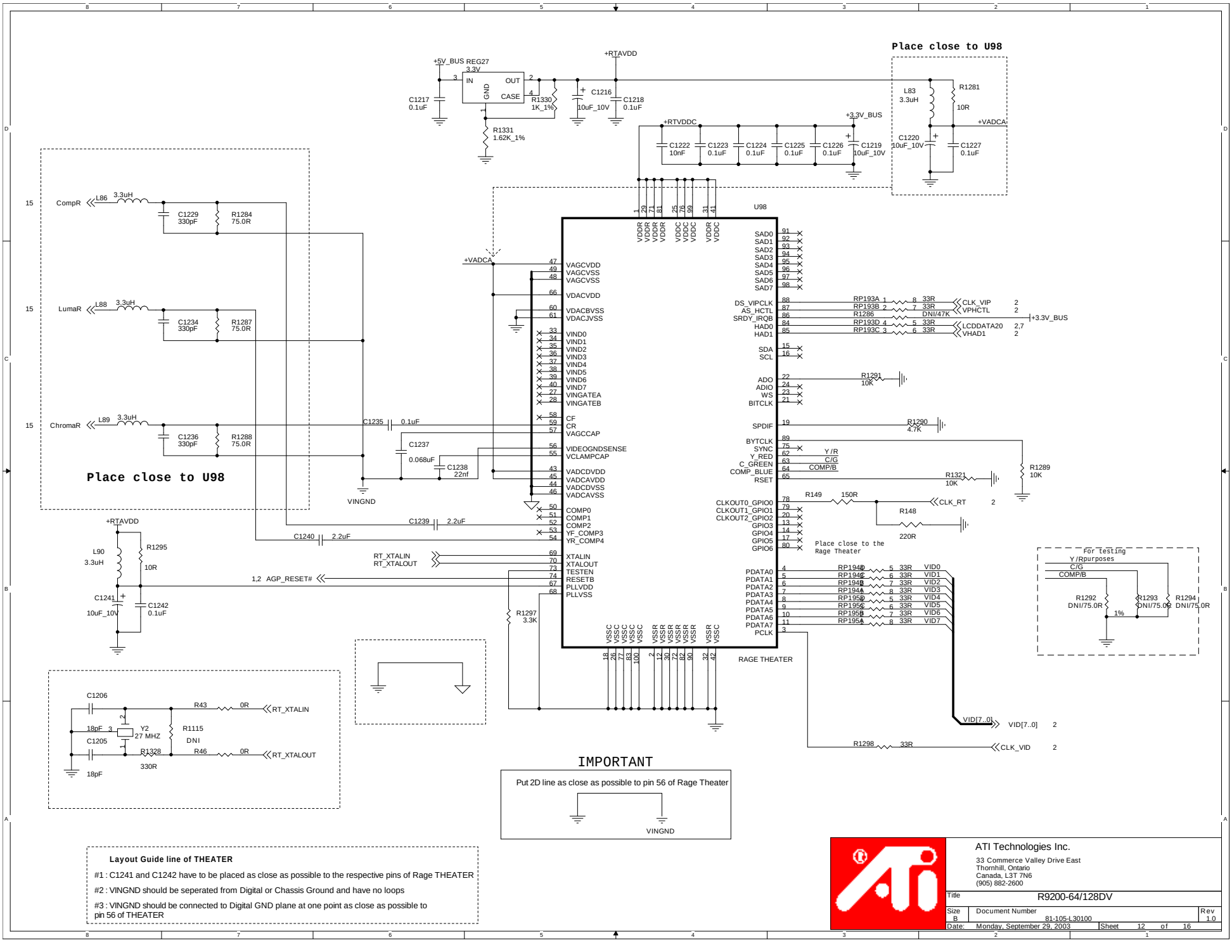
<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

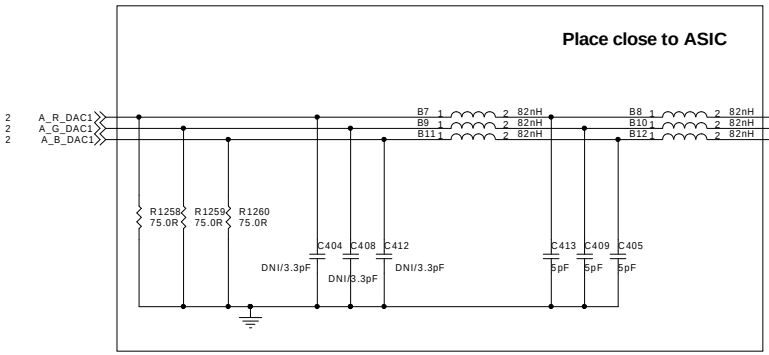
Title: R9200-64/128DV

Size: C | Document Number: 81-105-L30100 | Rev: 1.0

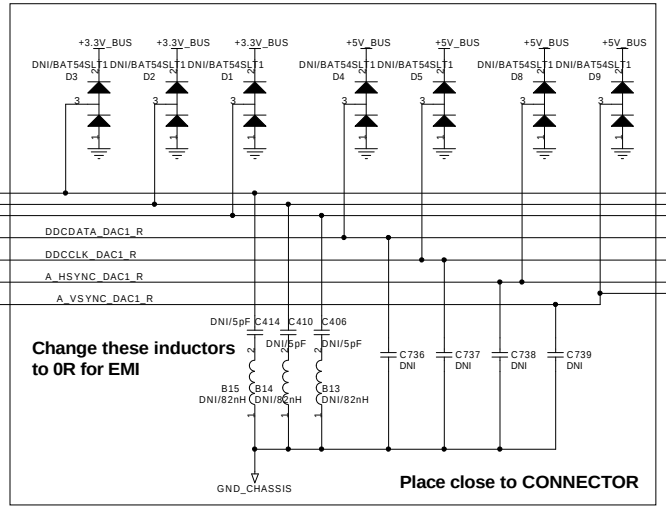
Date: Monday, September 29, 2003 | Sheet 11 of 16

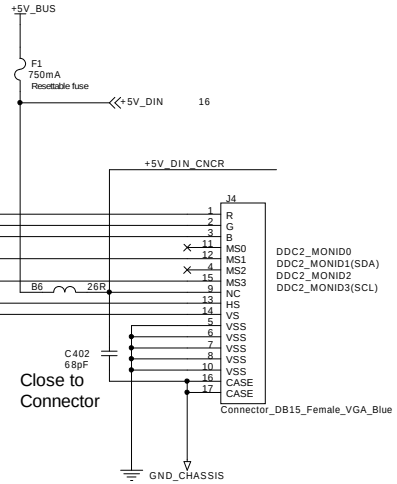

Place close to U98
+5V_BUS REG27
3.3V
IN
OUT
GND
CASE
R1330
1K_1%
R1331
1.62K_1%
C1216
10uF_10V
C1217
0.1uF
C1218
0.1uF
+RTAVDD
+RTVDDC
+3.3V_BUS
C1222
10nF
C1223
0.1uF
C1224
0.1uF
C1225
0.1uF
C1226
0.1uF
C1219
10uF_10V
L83
3.3uH
R1281
10R
+VADCA
C1220
10uF_10V
C1227
0.1uF
U98
VDDR
VDDC
VAGCVDD
VAGCVSS
VDACVDD
VDACBVSS
VDACJVSS
VIND0
VIND1
VIND2
VIND3
VIND4
VIND5
VIND6
VIND7
VINGATEA
VINGATEB
CF
CR
VAGCCAP
VIDEOGNDSENSE
VCLAMPCAP
VADCDVDD
VADCAVDD
VADCDVSS
VADCAVSS
COMP0
COMP1
COMP2
YF_COMP3
YR_COMP4
XTALIN
XTALOUT
TESTEN
RESETB
PLLVDD
PLLVSS
VSSC
VSSR
SAD0
SAD1
SAD2
SAD3
SAD4
SAD5
SAD6
SAD7
DS_VIPCLK
AS_HCTL
SRDY_IRQB
HAD0
HAD1
SDA
SCL
ADO
ADIO
WS
BITCLK
SPDIF
BYTCLK
SYNC
Y_RED
C_GREEN
COMP_BLUE
RSET
CLKOUT0_GPIO0
CLKOUT1_GPIO1
CLKOUT2_GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
PDATA0
PDATA1
PDATA2
PDATA3
PDATA4
PDATA5
PDATA6
PDATA7
PCLK
RAGE THEATER
RP193A
RP193B
RP193D
RP193C
RP194D
RP194C
RP194B
RP194A
RP195D
RP195C
RP195B
RP195A
33R
CLK_VIP
VPHCTL
LCDDATA20
VHAD1
R1286
DNI/47K
R1291
10K
R1290
4.7K
R1289
10K
R1321
10K
R149
150R
R148
220R
CLK_RT
Y /R
C/G
COMP/B
Place close to the
Rage Theater
For testing
Y /Rpurposes
C/G
COMP/B
R1292
DNI/75.0R
R1293
DNI/75.0R
R1294
DNI/75.0R
1%
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VID7
VID[7..0]
R1298
33R
CLK_VID
CompR
L86
3.3uH
C1229
330pF
R1284
75.0R
LumaR
L88
3.3uH
C1234
330pF
R1287
75.0R
ChromaR
L89
3.3uH
C1236
330pF
R1288
75.0R
C1235
0.1uF
C1237
0.068uF
C1238
22nf
VINGND
C1239
2.2uF
C1240
2.2uF
L90
3.3uH
R1295
10R
C1241
10uF_10V
C1242
0.1uF
1,2 AGP_RESET#
RT_XTALIN
RT_XTALOUT
R1297
3.3K
C1206
18pF
Y2
27 MHZ
C1205
18pF
R1115
DNI
R43
0R
R46
0R
R1328
330R
RT_XTALIN
RT_XTALOUT
IMPORTANT
Put 2D line as close as possible to pin 56 of Rage Theater
VINGND
Layout Guide line of THEATER
#1 : C1241 and C1242 have to be placed as close as possible to the respective pins of Rage THEATER
#2 : VINGND should be seperated from Digital or Chassis Ground and have no loops
#3 : VINGND should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER
ATI Technologies Inc.
33 Commerce Valley Drive East
Thornhill, Ontario
Canada, L3T 7N6
(905) 882-2600
Title
R9200-64/128DV
Size
B
Document Number
81-105-L30100
Rev
1.0
Date:
Monday, September 29, 2003
Sheet
12
of
16

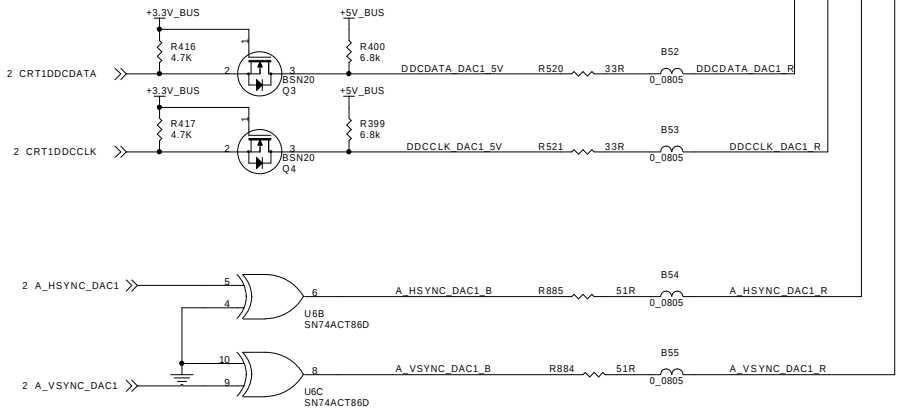
PRIMARY CRT



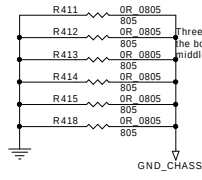
OPTIONAL ESD/HOTPLUG PROTECTION DIODES







*ATTENTION



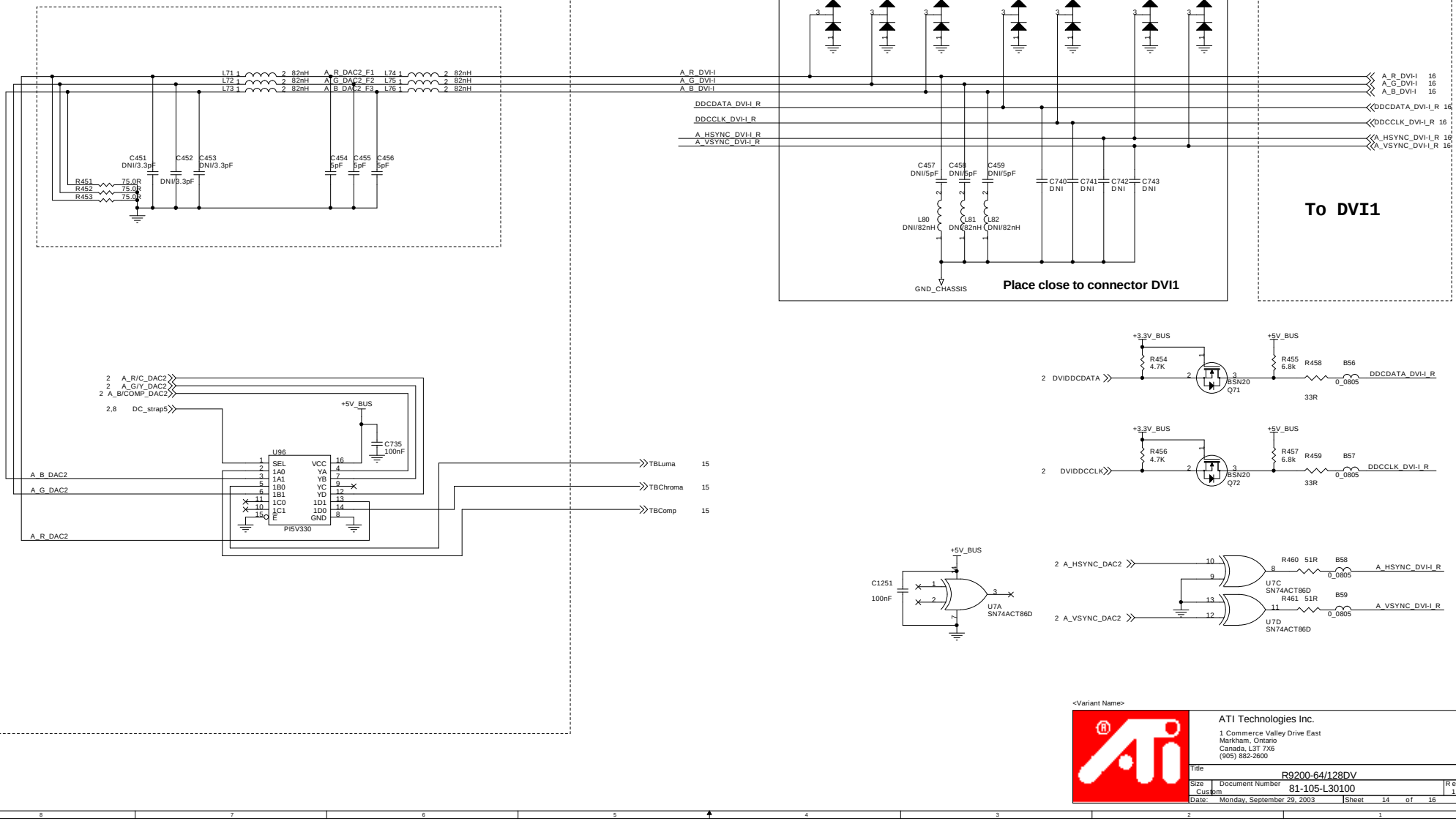
<Variant Name>

ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV	
Size: Custom	Document Number: 81-105-L30100	Rev: 1.0
Date: Monday, September 29, 2003	Sheet 13 of 16	

SECONDARY CRT

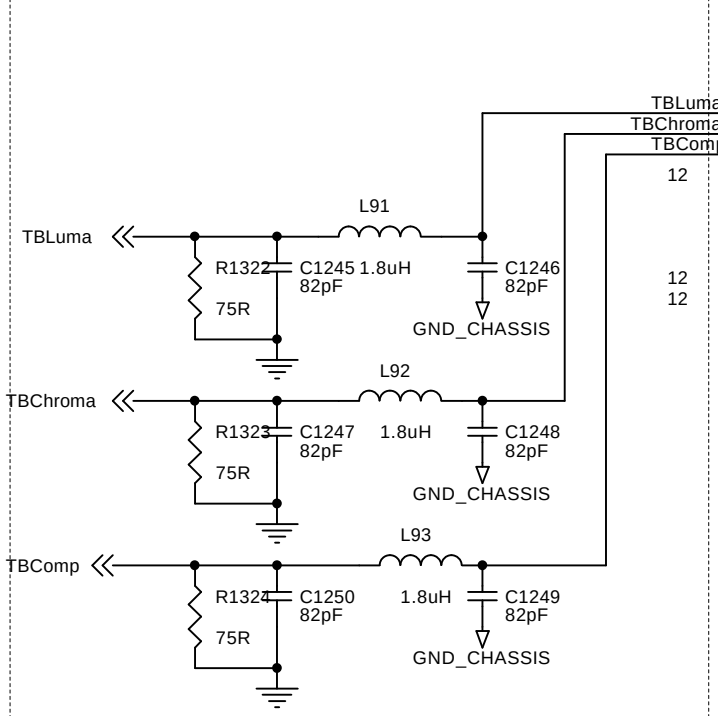


<Variant Name>

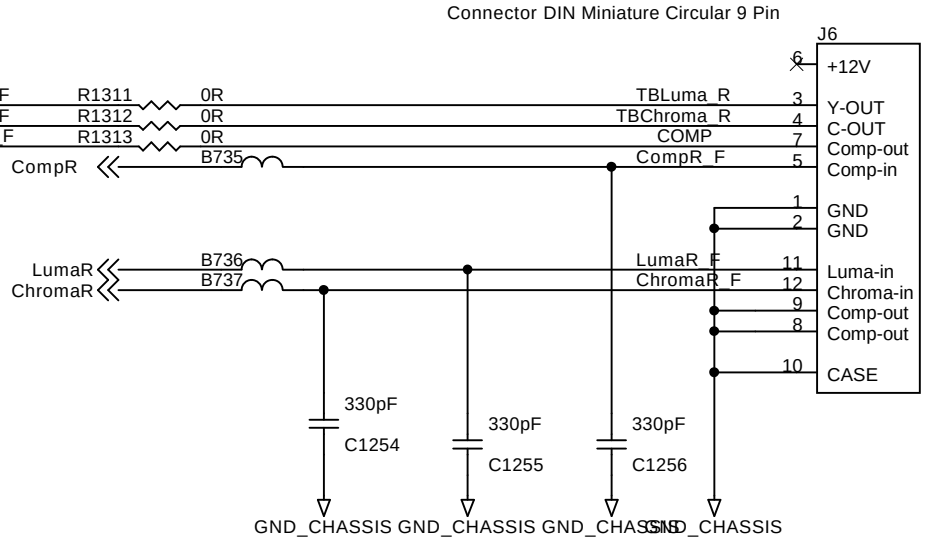
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	R9200-64/128DV	
Size: Custom	Document Number: 81-105-L30100	Rev: 1.0
Date: Monday, September 29, 2003	Sheet 14 of 16	

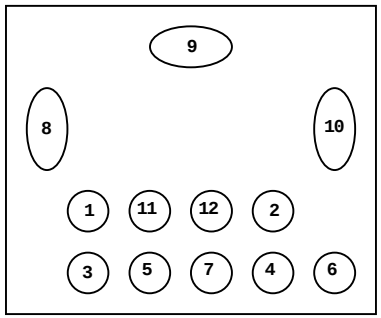
Place close to J6



VIVO MiniDIN 9-pin



J6 Pin define



Top view

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7N6
(905) 882-2600

Title	R9200-64/128DV	
Size A	Document Number 81-105-L30100	Rev 1.0
Date: Monday, September 29, 2003	Sheet 15 of 16	

PRIMARY DVI-I CONNECTOR

INSTALL TERMINATION RESISTORS CLOSE TO ASIC

INSTALL TERMINATION RESISTORS CLOSE TO CONNECTOR

2 TMDS_TX2N
2 TMDS_TX2P
R1268 330
R1269 DNI TMDS

2 TMDS_TX1N
2 TMDS_TX1P
R1270 330
R1271 DNI TMDS

2 TMDS_TX0N
2 TMDS_TX0P
R1272 330
R1273 DNI TMDS

2 TMDS_TXCP
2 TMDS_TXCN
R1274 330
R1275 DNI TMDS

DDCCLK_DVI-I
DDCDATA_DVI-I

13 +5V_DIN
B732 26R

14 A_VSYNC_DVI-I_R
14 A_R_DVI-I
14 A_G_DVI-I
14 A_B_DVI-I
14 A_HSYNC_DVI-I_R

DVI1

25	CASE
26	CASE
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND
27	CASE
28	CASE

DVI_A/D

TMDS

C1209 1.0uF

GND_CHASSIS GND_CHASSIS

2 CHARGE_POW
R1276 20K
D78 2.5V
R1277 100K TMDS

IF HOT PLUG DETECT IS NOT REQUIRED
REMOVE ALL THIS LOGIC EXCEPT
FOR 100K PULL DOWN

14 DDCCLK_DVI-I_R

14 DDCDATA_DVI-I_R

H1
GND GND GND GND GND GND GND GND GND
HG4MMHOLE8

GND_CHASSIS

<Variant Name>

ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: R9200-64/128DV

Size: Custom | Document Number: 81-105-L30100 | Rev: 1.0

Date: Monday, September 29, 2003 | Sheet 16 of 16