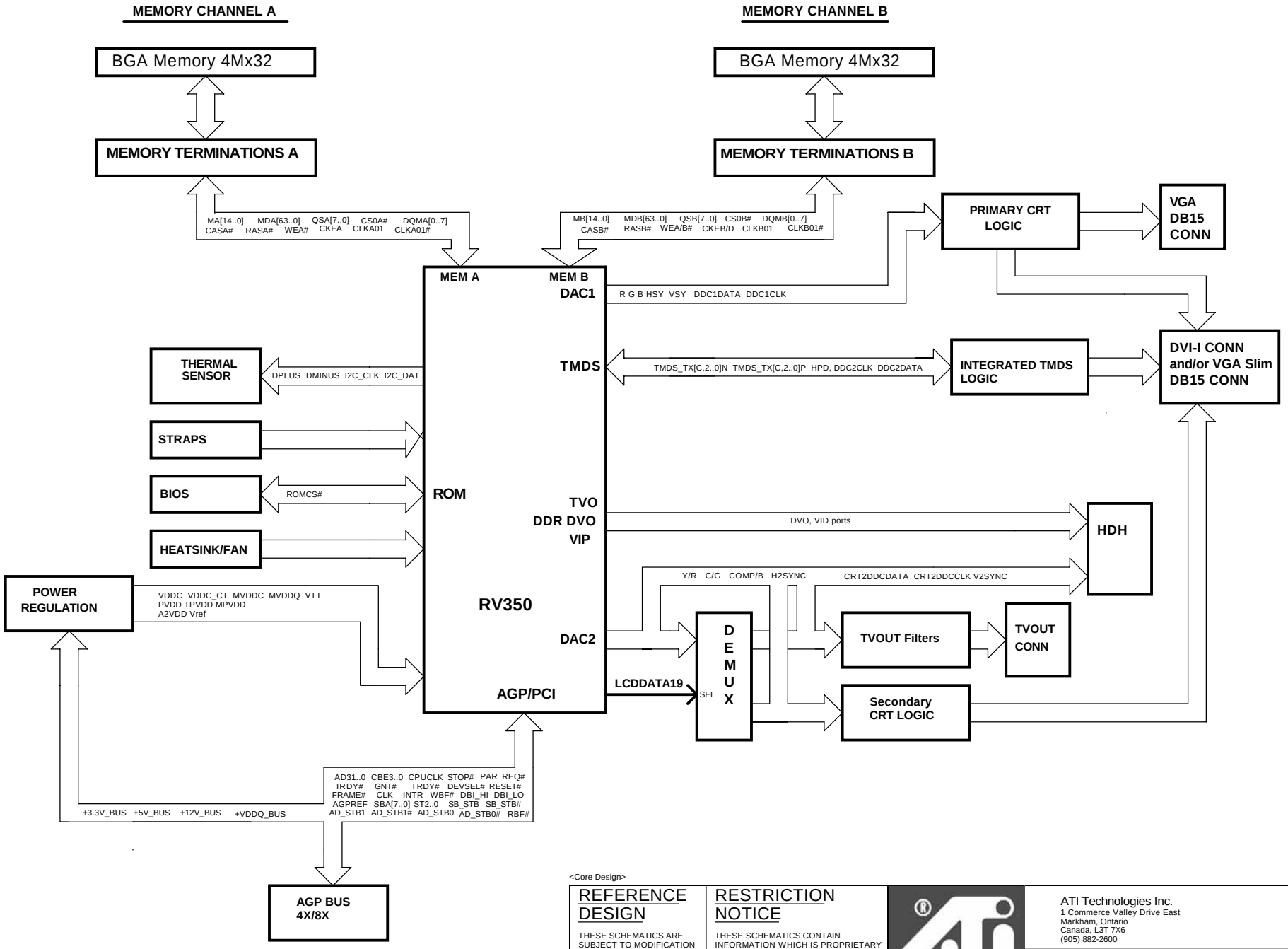
<Core Design>

Title	Schematic No.	Date:
AGP RV350 128M BGA VGA DVI VO	105-A034XX-20	**Monday, February 23, 2004**

REVISION HISTORY

Rev 7

Sch Rev	Date	REVISION DESCRIPTION
0	10/23/02	PRELIMINARY BASED ON "RV-350 REFERENCE (105-REF113-00A)"
1	01/10/03	Removed C168, C169, to make the MVREFS, MVREFD traces shorter (for better noise) Added R91 pull-up to fix "cold boot" problem: some boards would perform like ID DISABLED without the R91, because of floating /CS pin on the ROM (serial output overrides the ID DISABLED strap). Added J5/6 connection for auto detection of component video Added R100, R101 for easier power measurement Changed AGP connector to 4X/8X type
2	01/15/03	Added fix for MVDDQ leakage and R119, C163 Added provision for 3.3V_BUS on the MVDDC power supply PCB changed to rev C to fix component interference with daughtercards Removed R9, R11 Added R102 pull down Fixed connection QSA4, QSA5 on the ASIC side Changed C106, C107 to though-hole, added C166, C167 surface mount, alternate Added C74
3	01/15/03	Added external strap for PKGTYPE Added pullups for ZV_LCDCNTL(3:0) and STEREOSYNC Changed R123 to pull-up to MVDDC Added R255 for VDDC enable Added D122 alternative for cost reduction Added R1007 for EMI Removed R605, R606, R607, R608 to improve EMI
4	03/26/03	Allegro conversion based on the latest -00 revision
5	05/27/03	PCB changes only. No schematic changes from previous revision. This is a pads version based on the -00 revision.
6	07/30/03	Changed thermal sence and fan control circuit Changed temperature interrupt to AUXWIN aand added inverter Added C165
7	09/23/03	Changed p/n for J5, ASSY3, REF2 Deleted ASSY6



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REFERENCE DESIGN

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Title	AGP RV350 128M BGA VGA DVI VO	
Size B	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 1 of 20	

4X/8X AGP BUS

+12V_BUS: C10 100uF_16V
+5V_BUS: C5 100uF_16V
+3.3V_BUS: C8 100uF_16V
+VDDQ_BUS: C2 47uF_16V_Tant >=6.3V
USE 47uF TANTALUM CAPACITOR OR HIGHER

GND_MPVSS GND_TPVSS GND_A2VSSN GND_AVSSQ GND_RSET
GND_AVSSN GND_PVSS GND_TXVSSR GND_A2VSSQ GND_R2SET

NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND

DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

MAGP1

A1	12V	OVRCNT#	B1		
A2	TYPEDET#	5.0V	B2		
A3	GC_DET#/RESERVED	5.0V#B3	B3		
A4	USB-	USB+	B4		
A5	GND	GND#B5	B5		
A6	INTA#	INTB#	B6		
A7	RST#	CLK	B7		
A8	GNT#	REQ#	B8		
A9	VCC3.3	VCC3.3#B9	B9		
A10	ST1	ST0	B10	AGP_ST0	
A11	MB_DET#/RESERVED	ST2	B11	AGP_ST2	
A12	DBI_HI/PIPE#	RBF#	B12		
A13	GND#A13	GND#B13	B13		
A14	WBF#	DBI_LO/RESERVED	B14		
A15	SBA1	SBA0	B15	AGP_SBA0	
A16	VCC3.3#A16	VCC3.3#B16	B16		
A17	SBA3	SBA2	B17	AGP_SBA2	
A18	SB_STB#	SB_STB	B18		
A19	GND#A19	GND#B19	B19		
A20	SBA5	SBA4	B20	AGP_SBA4	
A21	SBA7	SBA6	B21	AGP_SBA6	
A22	RESERVED	RESERVED#B22	B22		
A23	GND#A23	GND#B23	B23		
A24	RESERVED#A24	3.3VAUX	B24		
A25	VCC3.3#A25	VCC3.3#B25	B25		
A26	AD30	AD31	B26	AGP_AD31	
A27	AD28	AD29	B27	AGP_AD29	
A28	AD28	VCC3.3#B28	B28		
A29	AD26	AD27	B29	AGP_AD27	
A30	AD24	AD25	B30	AGP_AD25	
A31	GND#A31	GND#B31	B31		
A32	AD_STB1#	AD_STB1	B32		
A33	C/BE3#	AD23	B33	AGP_AD23	
A34	VDDQ1.5	VDDQ1.5#B34	B34		
A35	AD22	AD21	B35	AGP_AD21	
A36	AD20	AD19	B36	AGP_AD19	
A37	GND#A37	GND#B37	B37		
A38	AD18	AD17	B38	AGP_AD17	
A39	AD16	C/BE2#	B39	AGP_C/BE#2	
A40	VDDQ1.5#A40	VDDQ1.5#B40	B40		
A41	FRAME#	IRDY#	B41		
A42	KEY	KEY#B42	B42		
A43	KEY#A43	KEY#B43	B43		
A44	KEY#A44	KEY#B44	B44		
A45	KEY#A45	KEY#B45	B45		
A46	TRDY#	DEVSEL#	B46		
A47	STOP#	VDDQ1.5#B47	B47		
A48	PME#	PERR#	B48		
A49	GND#A49	GND#B49	B49		
A50	PAR	SERR#	B50		
A51	AD15	C/BE1#	B51	AGP_C/BE#1	
A52	VDDQ1.5#A52	VDDQ1.5#B52	B52		
A53	AD13	AD14	B53	AGP_AD14	
A54	AD11	AD12	B54	AGP_AD12	
A55	GND#A55	GND#B55	B55		
A56	AD9	AD10	B56	AGP_AD10	
A57	C/BE0#	AD8	B57	AGP_AD8	
A58	VDDQ1.5#A58	VDDQ1.5#B58	B58		
A59	AD_STB0#	AD_STB0	B59		
A60	AD6	AD7	B60	AGP_AD7	
A61	GND#A61	GND#B61	B61		
A62	AD4	AD5	B62	AGP_AD5	
A63	AD2	AD3	B63	AGP_AD3	
A64	VDDQ1.5#A64	VDDQ1.5#B64	B64		
A65	AD0	AD1	B65	AGP_AD1	
A66	VREFGC	VREFCG	B66		

1.5V_AGP_BUS

AGP_C/BE#[3..0] → AGP_C/BE#[3..0] [3]
AGP_AD[31..0] → AGP_AD[31..0] [3]
AGP_SBA[7..0] → AGP_SBA[7..0] [3]
AGP_ST[2..0] → AGP_ST[2..0] [3]

TYDET
AGP_GC_8X_DET#
[3] AGP_INTR#
AGP_RST#
[3] AGP_GNT#
AGP_ST1
[3] AGP_MB_8X_DET# R15 0R
[3] AGP_DBI_HI R16 0R
[3] AGP_WBF# R18 0R
AGP_SBA1
AGP_SBA3
[3] AGP_SBSTB# R1 0R
AGP_SBA5
AGP_SBA7
AGP_AD30
AGP_AD28
AGP_AD26
AGP_AD24
[3] AGP_ADSTB1# R5 0R
AGP_C/BE#3
AGP_AD22
AGP_AD20
AGP_AD18
AGP_AD16
[3] AGP_FRAME# R7 0R
[3] AGP_TRDY#
[3] AGP_STOP#
AGP_PAR_R
[3] AGP_PAR
AGP_AD15
AGP_AD13
AGP_AD11
AGP_AD9
AGP_C/BE#0
[3] AGP_ADSTB0# R12 0R
AGP_AD6
AGP_AD4
AGP_AD2
AGP_AD0
AGP_VREFGC

AGP_AGPCLK_R R61 0R → AGP_AGPCLK [3], AGP_REQ# [3]
AGP_DBI_LO_R R62 0R → AGP_RBF# [3], AGP_DBI_LO [3]
AGP_SBSTB_R R2 0R → AGP_SBSTB [3]
AGP_ADSTB1_R R6 0R → AGP_ADSTB1 [3]
R8 0R → AGP_IRDY# [3]
R10 0R → AGP_DEVSEL# [3]
AGP_ADSTB0_R R13 0R → AGP_ADSTB0 [3]
AGP_AGPREF
C4 DNI_10pF
C1 DNI_1.0uF

TYDET — R19 2.2R
For retail, 1K ohm pull-down causes AMD system detects AGP2X only
+12V, TYPEDET# short protection for OEM (1KR)

AGP_GC_8X_DET# — R60 _0R

[3,14] AGP_RESET# — R4 180R — R3 100R — U6A SN74ACT86D — AGP_RST#
+5V_BUS — C11 1.0uF

UNIVERSAL VREFGC CIRCUIT (4X, 8X)

[3] 8X_DET# — R17 47K
[3] AGP_MB_8X_DET# — U6B SN74ACT86D — TEST
Q1 2N7002E
R20 324R_1%
R21 147R_1%
R23 1K
R24 100R_1%
C6 10nF
AGP_VREFGC

UNIVERSAL VREFCG CIRCUIT (4X, 8X)

AGP_AGPREF
+VDDQ_BUS
TEST
Q5 _2N7002E
R66 _324R_1%
R64 DNI_0R
R67 _147R_1%
R65 _100R_1%
C7 10nF
AGP_AGPREFCG → AGP_AGPREFCG [3]

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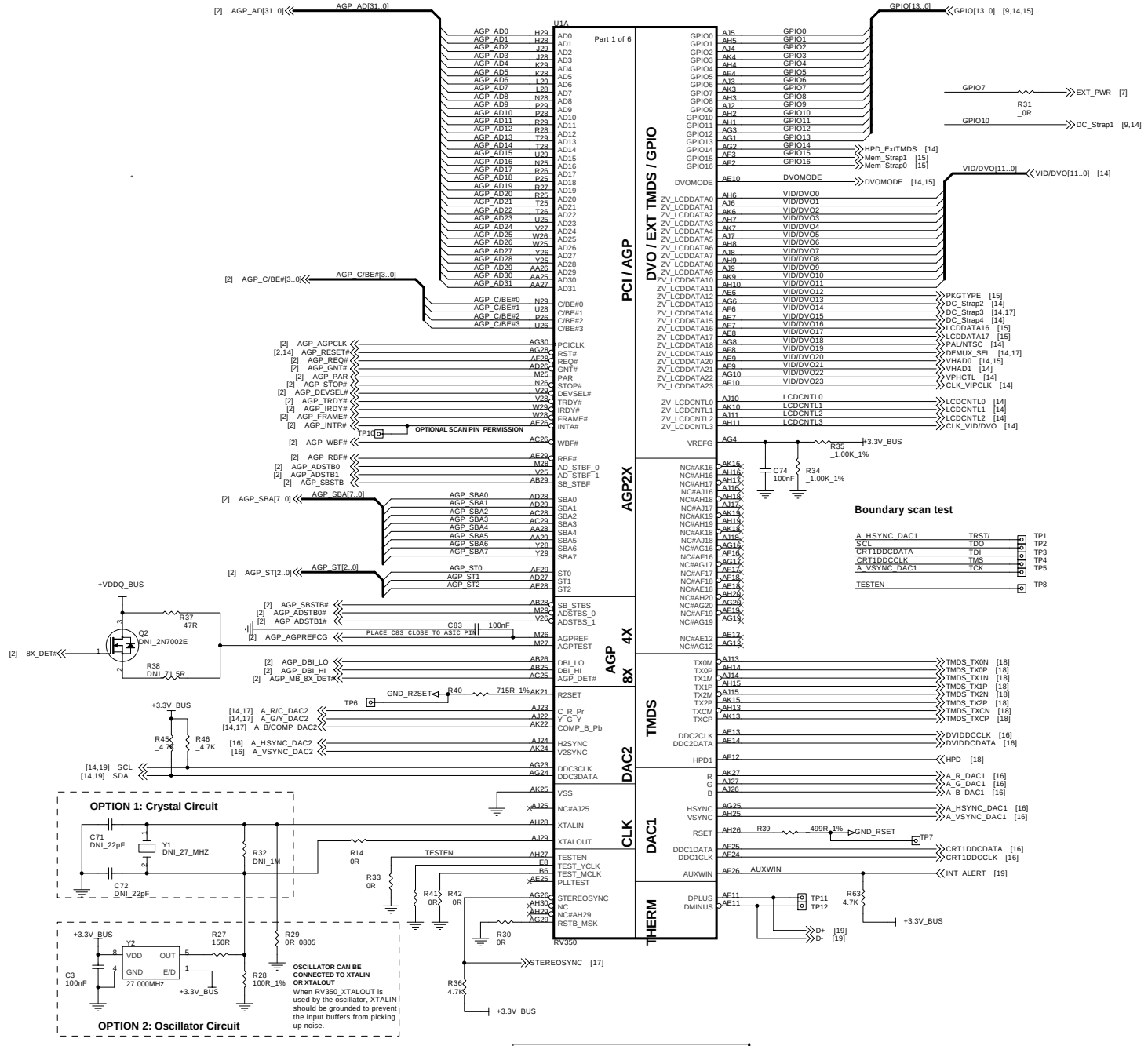
Title	AGP RV350 128M BGA VGA DVI VO		
Size C	Document Number 105-A034XX-20		Rev 7
Date: Monday, February 23, 2004		Sheet 2 of 20	



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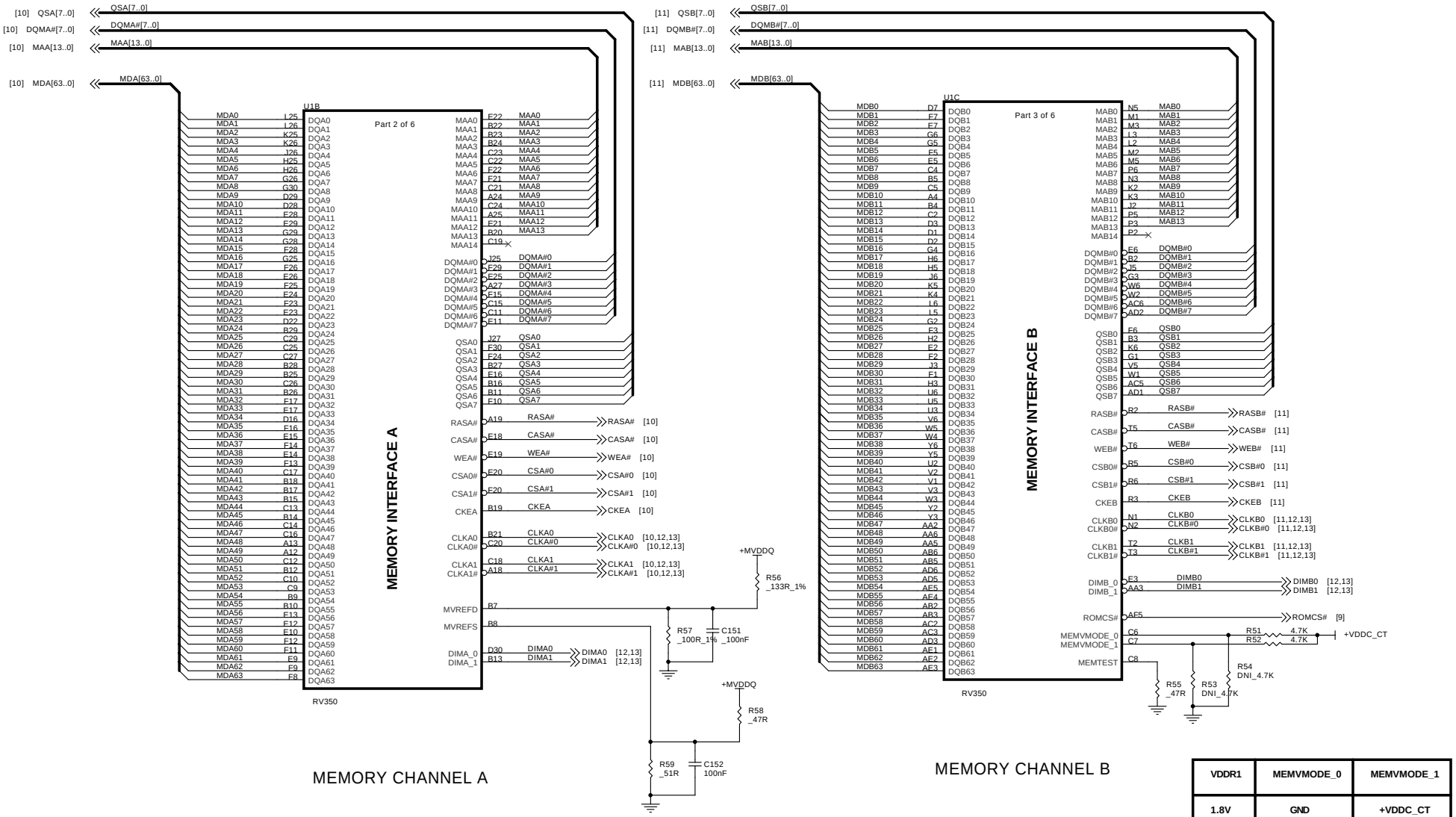
Size: Custom	Document Number: 105-A034XX-20		Rev: 7
Date: Monday, February 23, 2004	Sheet 3 of 20		



MEMORY CHANNEL A

MEMORY CHANNEL B

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

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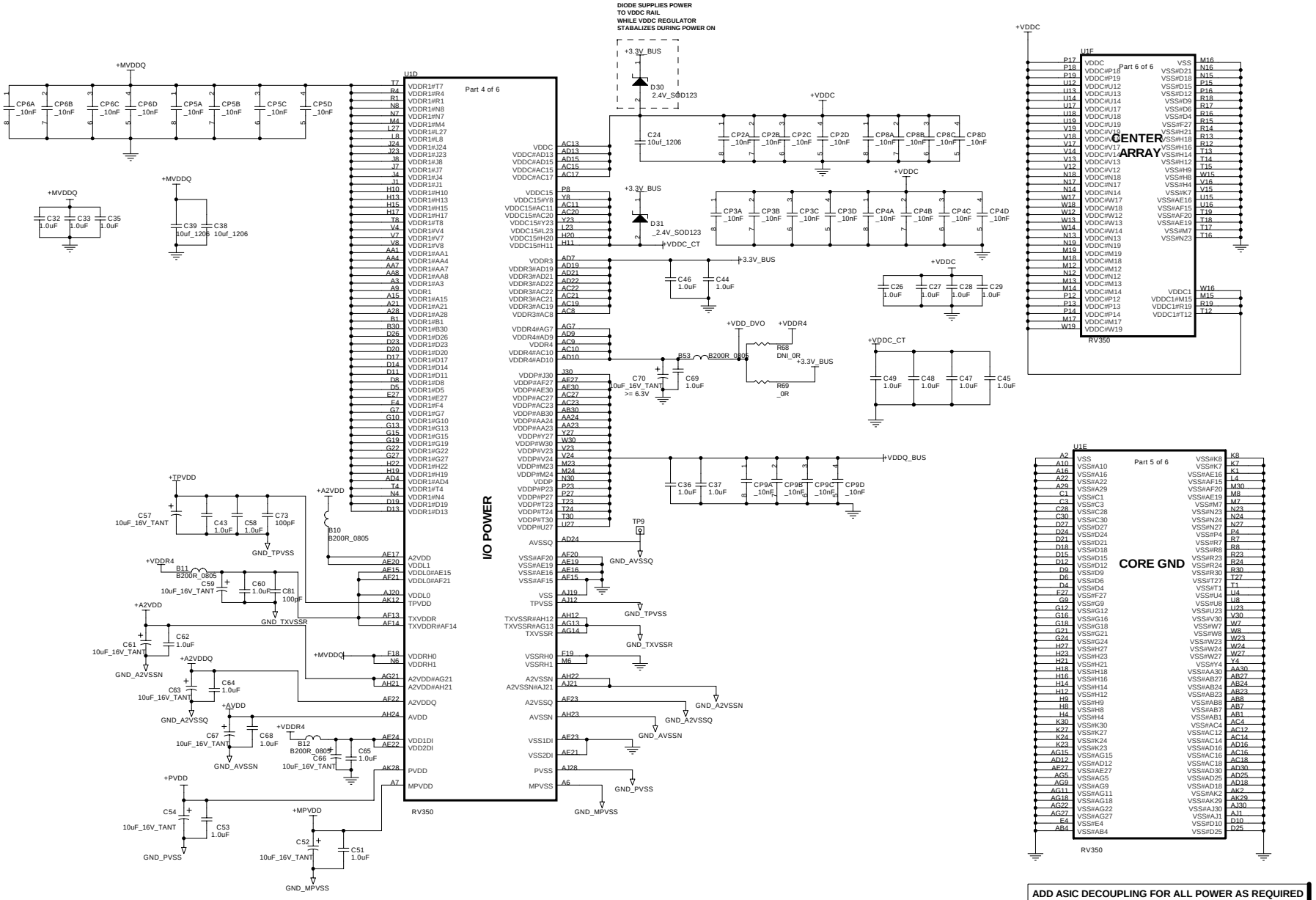
Title: AGP RV350 128M BGA VGA DVI VO

Size: Custom | Document Number: 105-A034XX-20 | Rev: 7

Date: Wednesday, February 25, 2004 | Sheet 4 of 20



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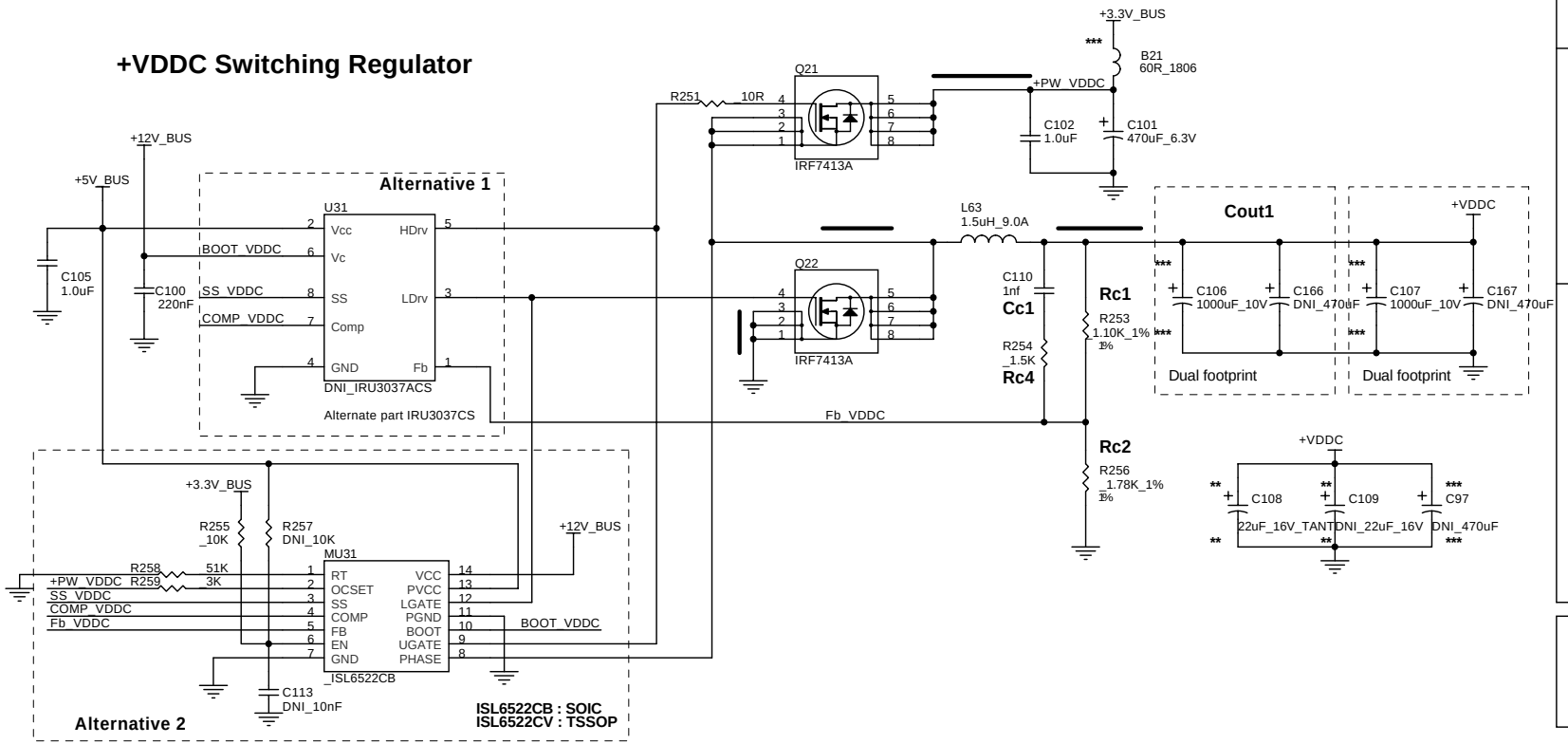
Title	AGP RV350 128M BGA VGA DVI VO		
Size C	Document Number 105-A034XX-20		Rev 7
Date: Monday, February 23, 2004		Sheet 5 of 20	

+VDDC Switching Regulator



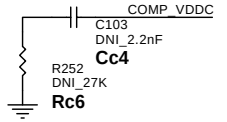
Regulator for VDDC (RV350 Core)
Vin = 3.3V_BUS
Vout = 1.2V
Iout = 7A MAX (load consumption)
Iout = 3A MAX (Power rail consumption)

REG.	VOLTAGE	RESISTORS	
		Rc1	Rc2
ISL6522C	1.2V	1.00K (p/n 3240100100)	2K (p/n 3240200100)
	1.25V	1.00K (p/n 3240100100)	1K78 (p/n 3240178100)
	1.3V	1.10K (p/n 3240110100)	1K78 (p/n 3240178100)

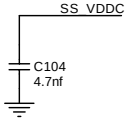
Compensation options for +VDDC regulator

Alt. Compensation 1

This compensation circuit is simplified and will only work with the IRU3037(A) Regulator

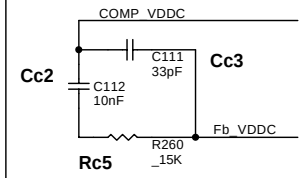


Common



Alt. Compensation 2

This is required for the ISL6522CB regulator, and provides maximum regulation speed for IRU3037 Regultor



Note: Alternative Compensation Circuit 2 will only work if Rc1 is a 1k Ohm Resistor. Alternative Compensation Circuit 1 has no requirements for the divider circuit.

Cout1 470uF thru hole capacitor has 30mR ESR where as 470uF SMT capacitor has 22mR ESR. For current below 4.5A, 1 thru 470uF is enough.

Part	INSTALL	Compensation Circuit	DO NOT INSTALL
IRU3037 IRU3037A	Alternative1	Common, and Either Alt. Compensation 1, or Alt. Compensation 2	Cc4, Rc6 Alternative 2
ISL6522CB	Alternative2	Common and Alt. Compensation 2	Alternative1

*** Indicates number of vias required for the connection

C166, C167 alternate parts for C106, C107

Place C102 capacitor very close to the Q21 pins

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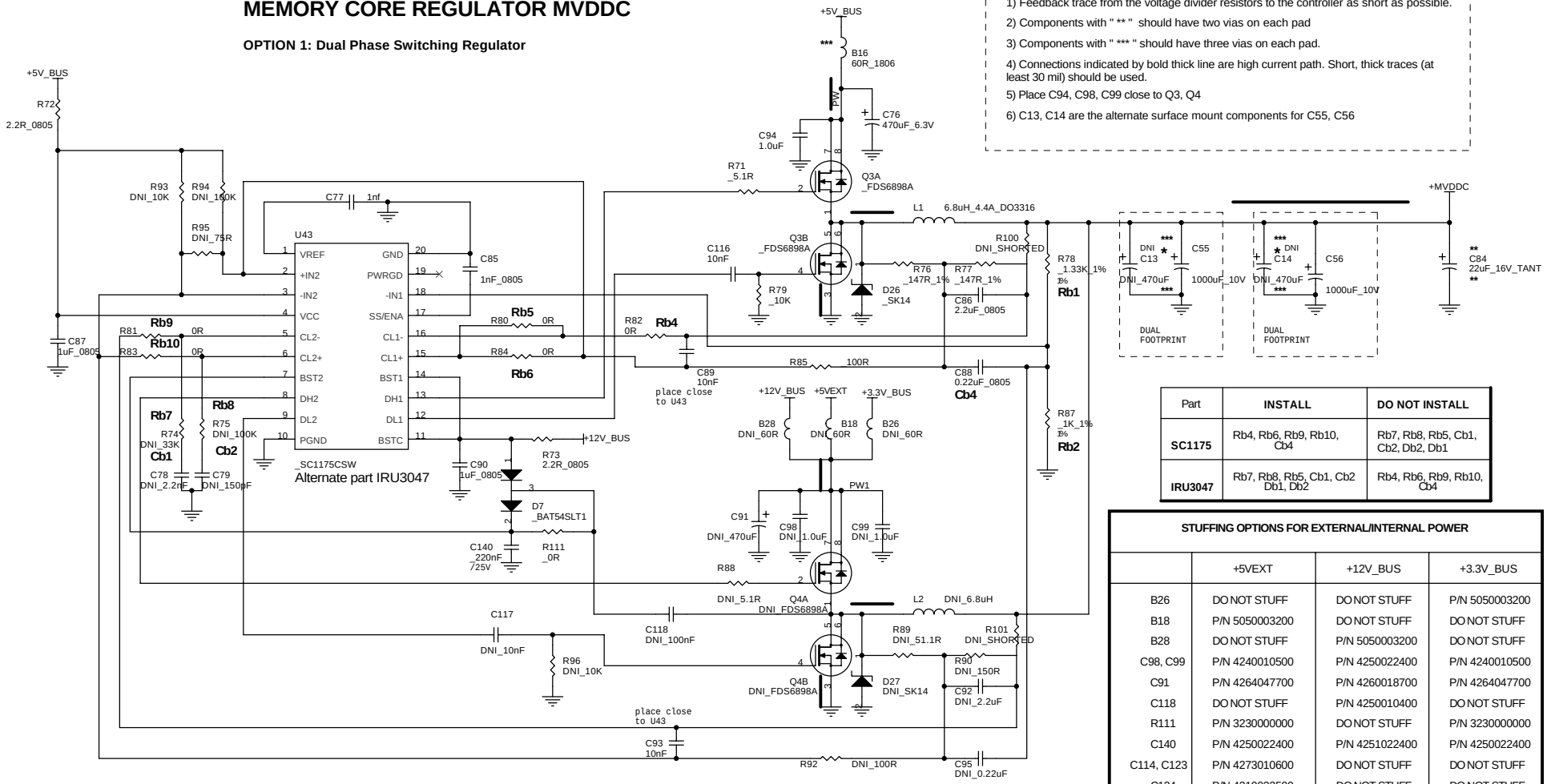
Size B	Document Number 105-A034XX-20	Rev 7
Date: Monday, March 29, 2004	Sheet 6 of 20	

MEMORY CORE REGULATOR MVDDC

OPTION 1: Dual Phase Switching Regulator



Layout Guide Lines for switching regulators

1) Feedback trace from the voltage divider resistors to the controller as short as possible.

2) Components with " ** " should have two vias on each pad

3) Components with " *** " should have three vias on each pad.

4) Connections indicated by bold thick line are high current path. Short, thick traces (at least 30 mil) should be used.

5) Place C94, C98, C99 close to Q3, Q4

6) C13, C14 are the alternate surface mount components for C55, C56

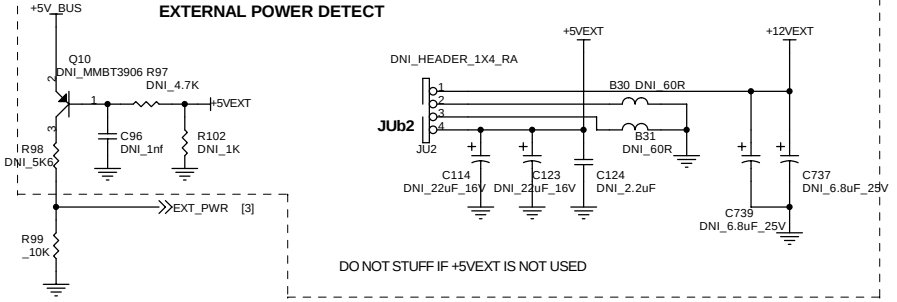
Part	INSTALL	DO NOT INSTALL
SC1175	Rb4, Rb6, Rb9, Rb10, Cb4	Rb7, Rb8, Rb5, Cb1, Cb2, Db2, Db1
IRU3047	Rb7, Rb8, Rb5, Cb1, Cb2 Db1, Db2	Rb4, Rb6, Rb9, Rb10, Cb4

STUFFING OPTIONS FOR EXTERNAL/INTERNAL POWER

	+5VEXT	+12V_BUS	+3.3V_BUS
B26	DO NOT STUFF	DO NOT STUFF	P/N 5050003200
B18	P/N 5050003200	DO NOT STUFF	DO NOT STUFF
B28	DO NOT STUFF	P/N 5050003200	DO NOT STUFF
C98, C99	P/N 4240010500	P/N 4250022400	P/N 4240010500
C91	P/N 4264047700	P/N 4260018700	P/N 4264047700
C118	DO NOT STUFF	P/N 4250010400	DO NOT STUFF
R111	P/N 3230000000	DO NOT STUFF	P/N 3230000000
C140	P/N 4250022400	P/N 4251022400	P/N 4250022400
C114, C123	P/N 4273010600	DO NOT STUFF	DO NOT STUFF
C124	P/N 4210022500	DO NOT STUFF	DO NOT STUFF
B30, B31	P/N 5050003200	DO NOT STUFF	DO NOT STUFF
JU2	P/N 6140011300	DO NOT STUFF	DO NOT STUFF
Q10	P/N 2021390600	DO NOT STUFF	DO NOT STUFF
C96	P/N 4250010200	DO NOT STUFF	DO NOT STUFF
R97	P/N 3230047200	DO NOT STUFF	DO NOT STUFF
R98	P/N 3230056200	DO NOT STUFF	DO NOT STUFF

Part	MVDDC	Rb1	Rb2
SC1175	2.8V	1K24 (p/n 3240124100)	1.00K (p/n 3240100100)
	2.9V	1K33 (p/n 3240133100)	1.00K (p/n 3240100100)

EXTERNAL POWER DETECT



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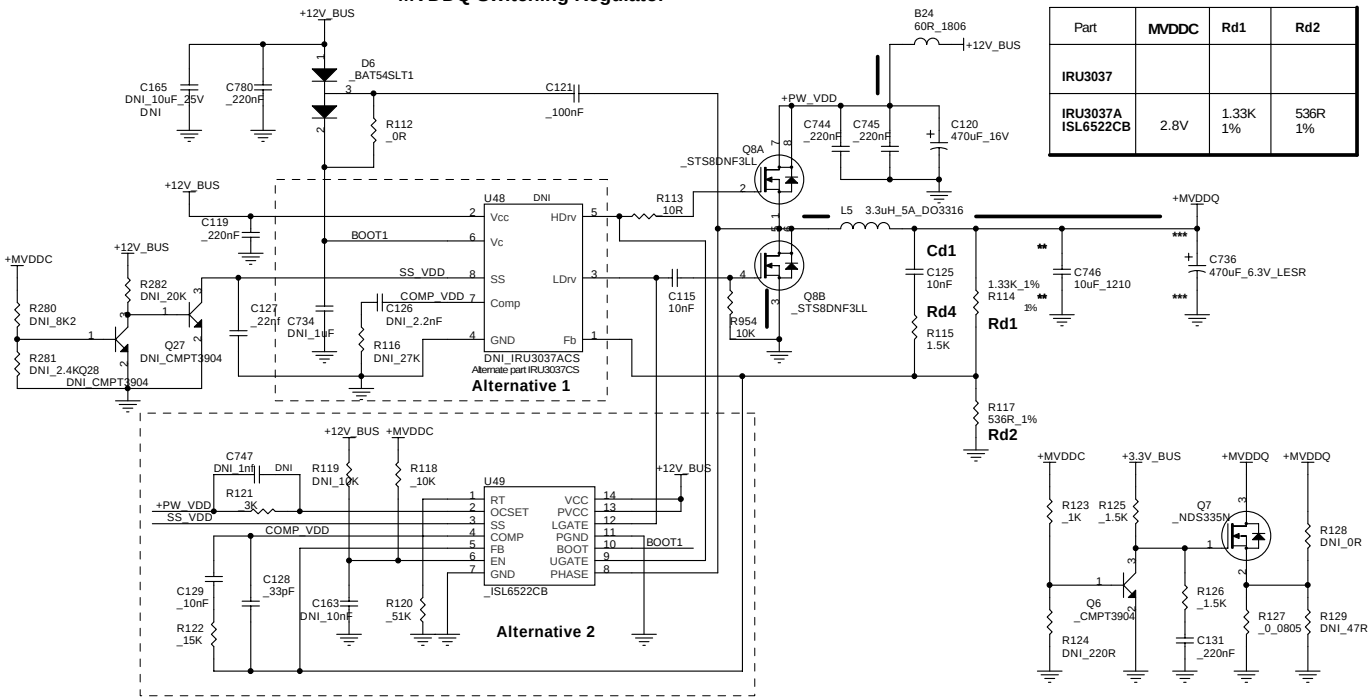
Size B	Document Number 105-A034XX-20		Rev 7
Date: Monday, March 29, 2004	Sheet 7 of 20		

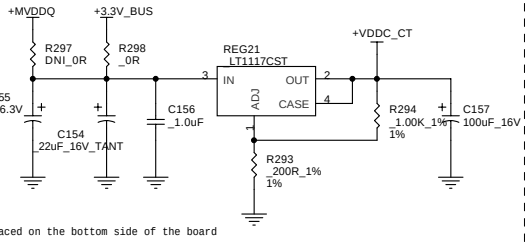
MVDDQ Switching Regulator



Part	MVDDC	Rd1	Rd2
IRU3037			
IRU3037A ISL6522CB	2.8V	1.33K 1%	536R 1%

Regulator for +VDDC_CT

Vin = 3.3V
Vout = 1.5V (MAX TBD)
Iout =

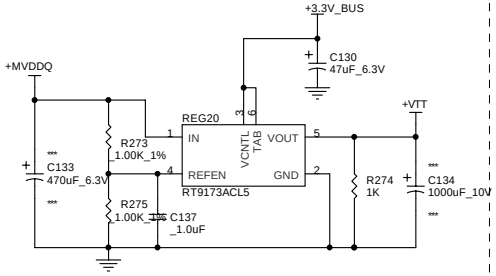


VDDC_CT	R293	R294
1.5V	200R	1K

C154 is Tantalum only if it has to be placed on the bottom side of the board

+VTT Linear Regulator

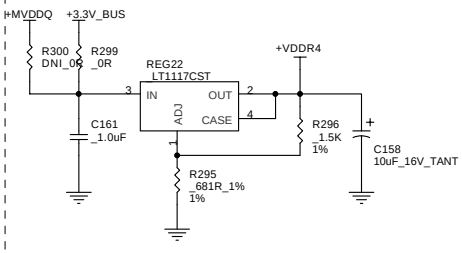
Vin = +MVDDQ
Vout = 1.25V
Iout = 2000mA MAX
Iout = 750mA Est. MAX



	R273	R275
1.4V	1K	1K

Regulator for +VDDR4

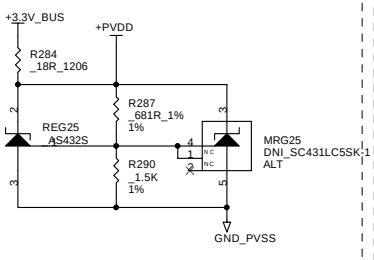
Vin = 3.3V
Vout = 1.8V
Iout =



+VDDR4	R295	R296
1.8V	681R	1K5

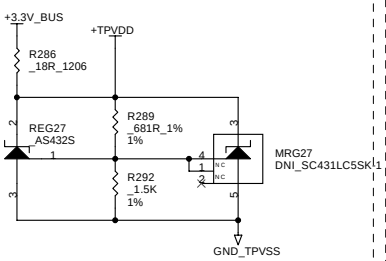
Regulator for +PVDD

Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX



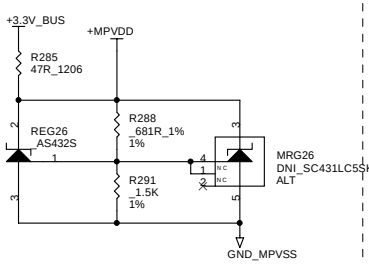
Regulator for +TPVDD

Vin = +3.3V AGP
Vout = 1.8V
Iout = 75mA MAX



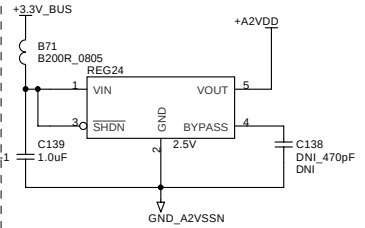
Regulator for +MPVDD

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX



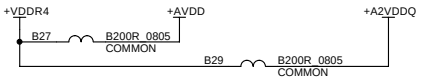
Regulator for +A2VDD

Vin = +3.3V AGP
Vout = 2.5V
Iout = 150mA MAX



+A2VDD and GND_A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch.

AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)



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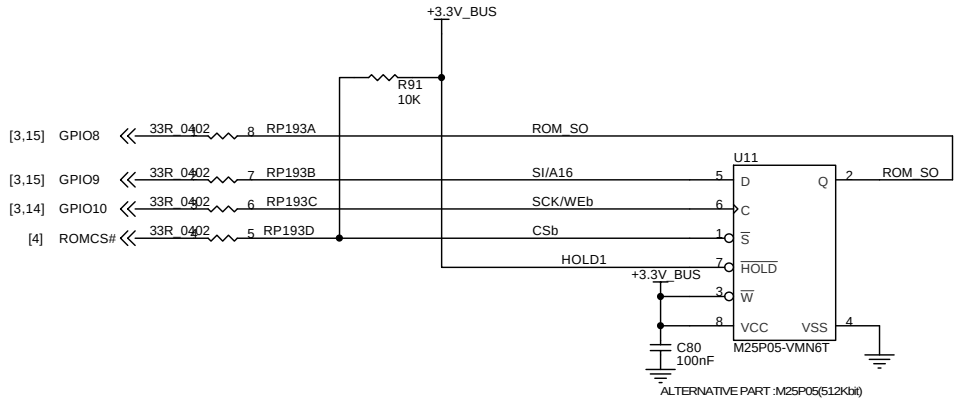
Title	AGP RV350 128M BGA VGA DVI VO	
Size: Custom	Document Number: 105-A034XX-20	Rev: 7
Date: Monday, March 29, 2004	Sheet 8 of 20	

SERIAL EEPROM 512K/1M



<Core Design>

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Title	AGP RV350 128M BGA VGA DVI VO	
Size B	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 9 of 20	

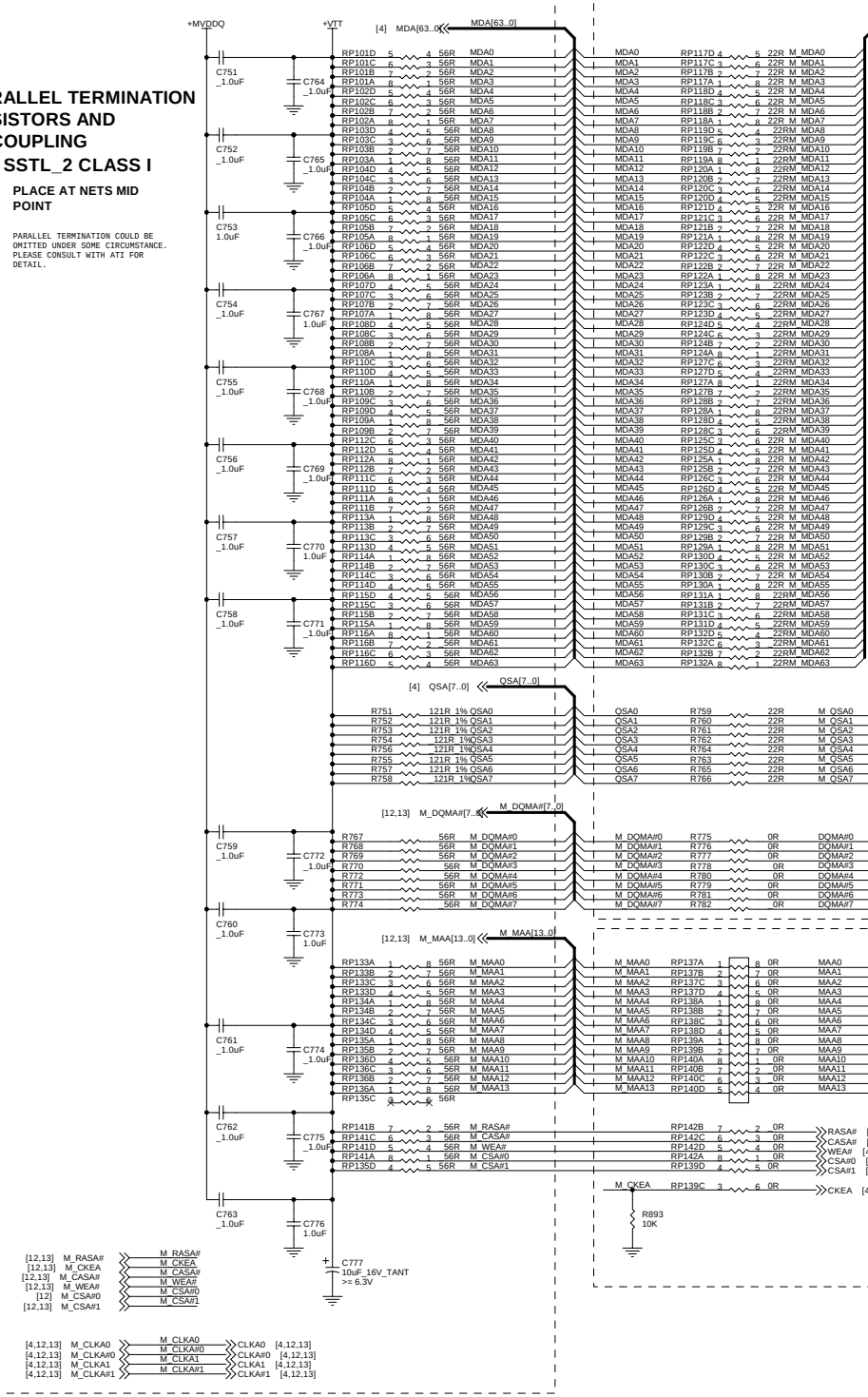
TERMINATION FOR MEMORY CHANNEL A

PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.



SERIES Resistors

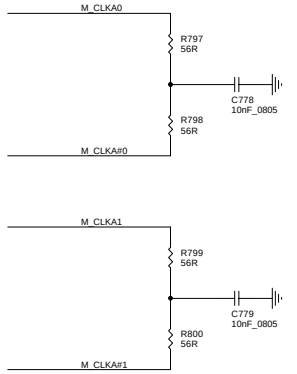
For Bi-Directional signals, Series resistors should be placed close to the memory

For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



<Core Design>

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Title: AGP RV350 128M BGA VGA DVI VO

Size: Custom | Document Number: 105-A034XX-20 | Rev: 7

Date: Monday, February 23, 2004 | Sheet 10 of 20

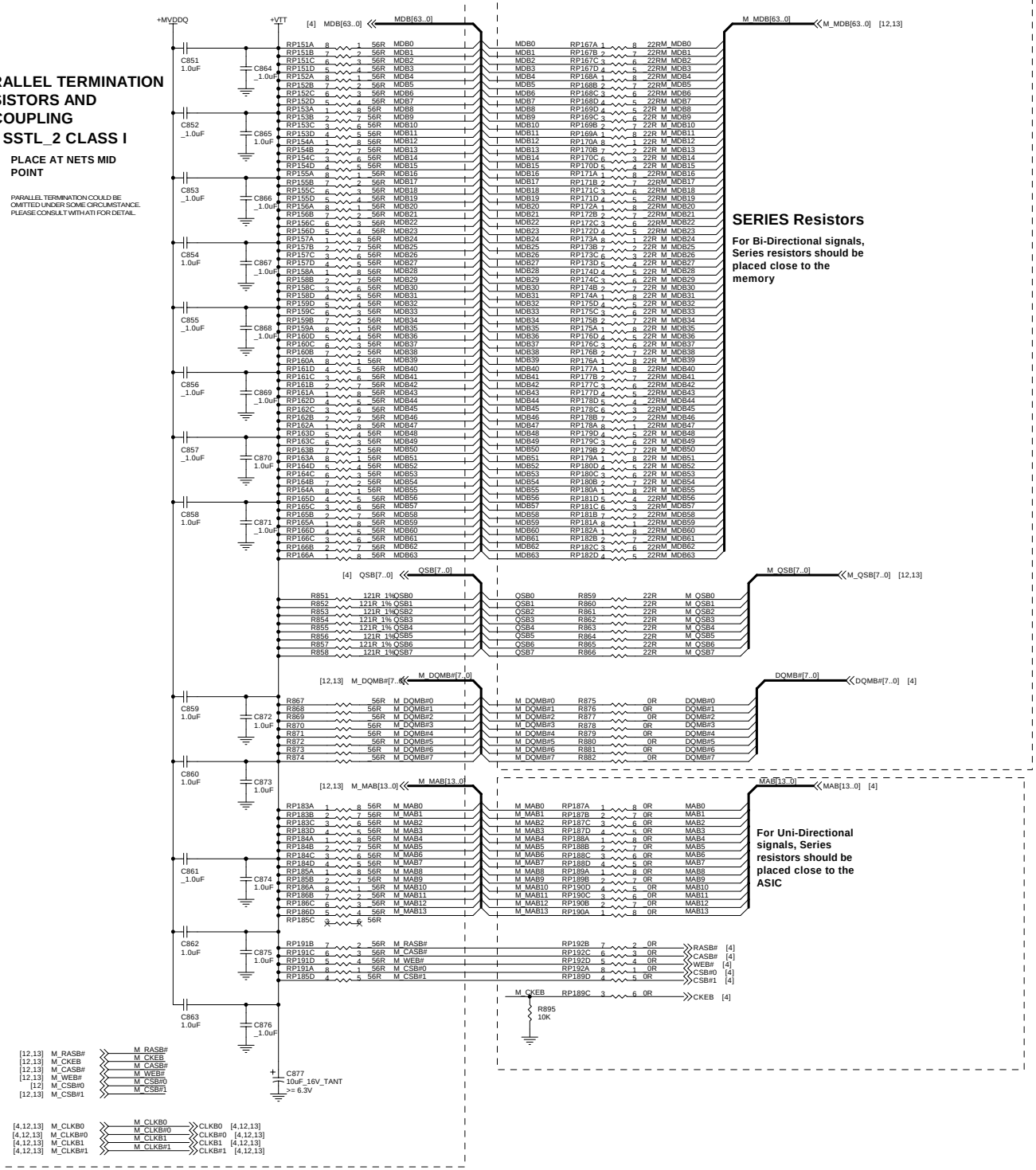
TERMINATION FOR MEMORY CHANNEL B

PARALLEL TERMINATION RESISTORS AND DECOUPLING

SSTL_2 CLASS I

PLACE AT NETS MID POINT

PARALLEL TERMINATION COULD BE OMITTED UNDER SOME CIRCUMSTANCE. PLEASE CONSULT WITH ATI FOR DETAIL.



SERIES Resistors

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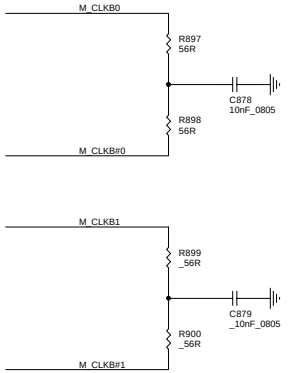
For Uni-Directional signals, Series resistors should be placed close to the ASIC

CLOCK terminations

Change from 1:1 spacing to at least a 2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory



<Core Design>

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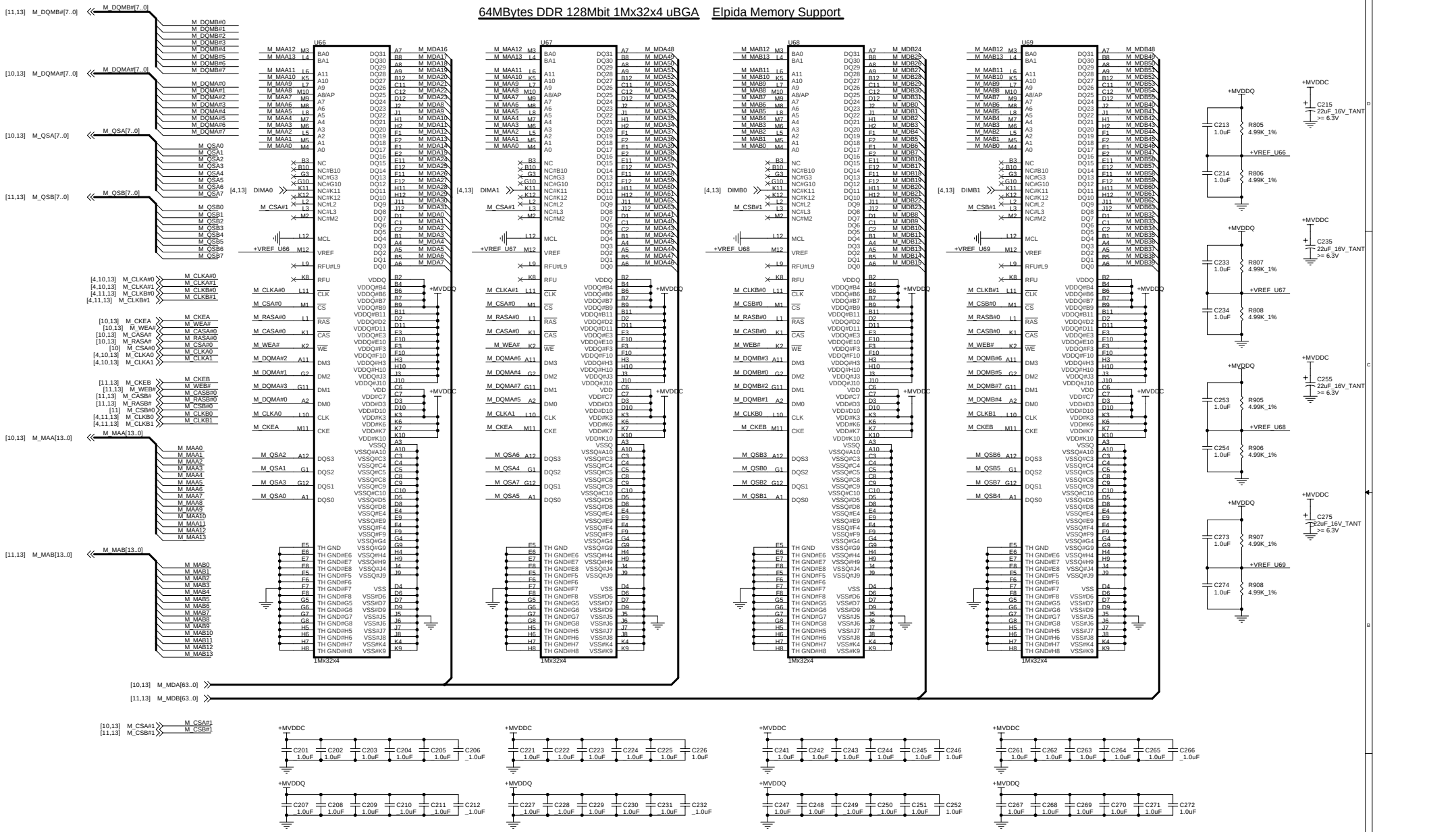
Title	AGP RV350 128M BGA VGA DVI VO	
Size C	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 11 of 20	

rank 1

64MBytes DDR 128Mbit 1Mx32x4 uBGA Elpida Memory Support



<Core Design>

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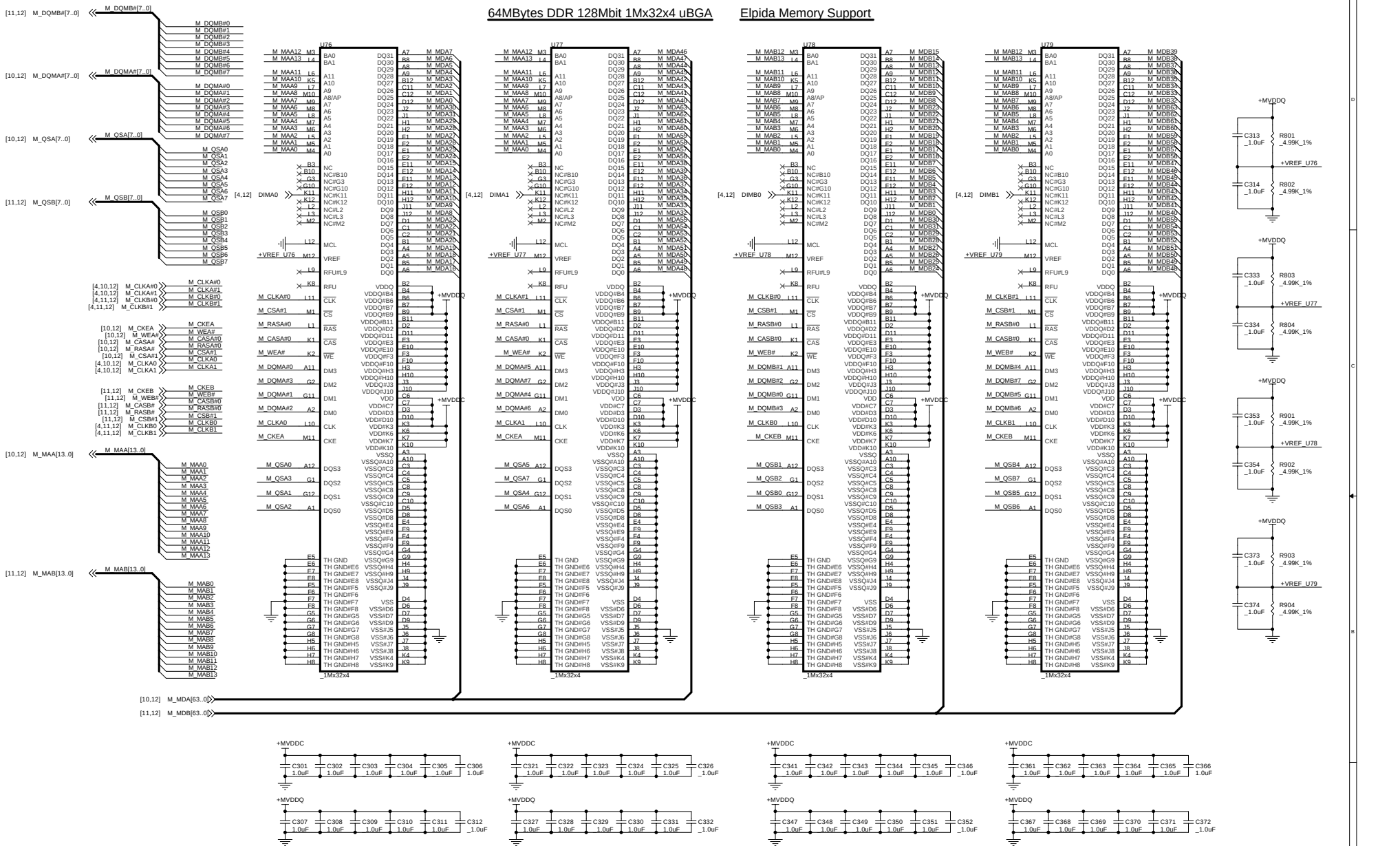
Size: Custom	Document Number: 105-A034XX-20	Rev: 7
Date: Monday, February 23, 2004	Sheet 12 of 20	

rank 2

64MBytes DDR 128Mbit 1Mx32x4 uBGA Elpida Memory Support



<Core Design>

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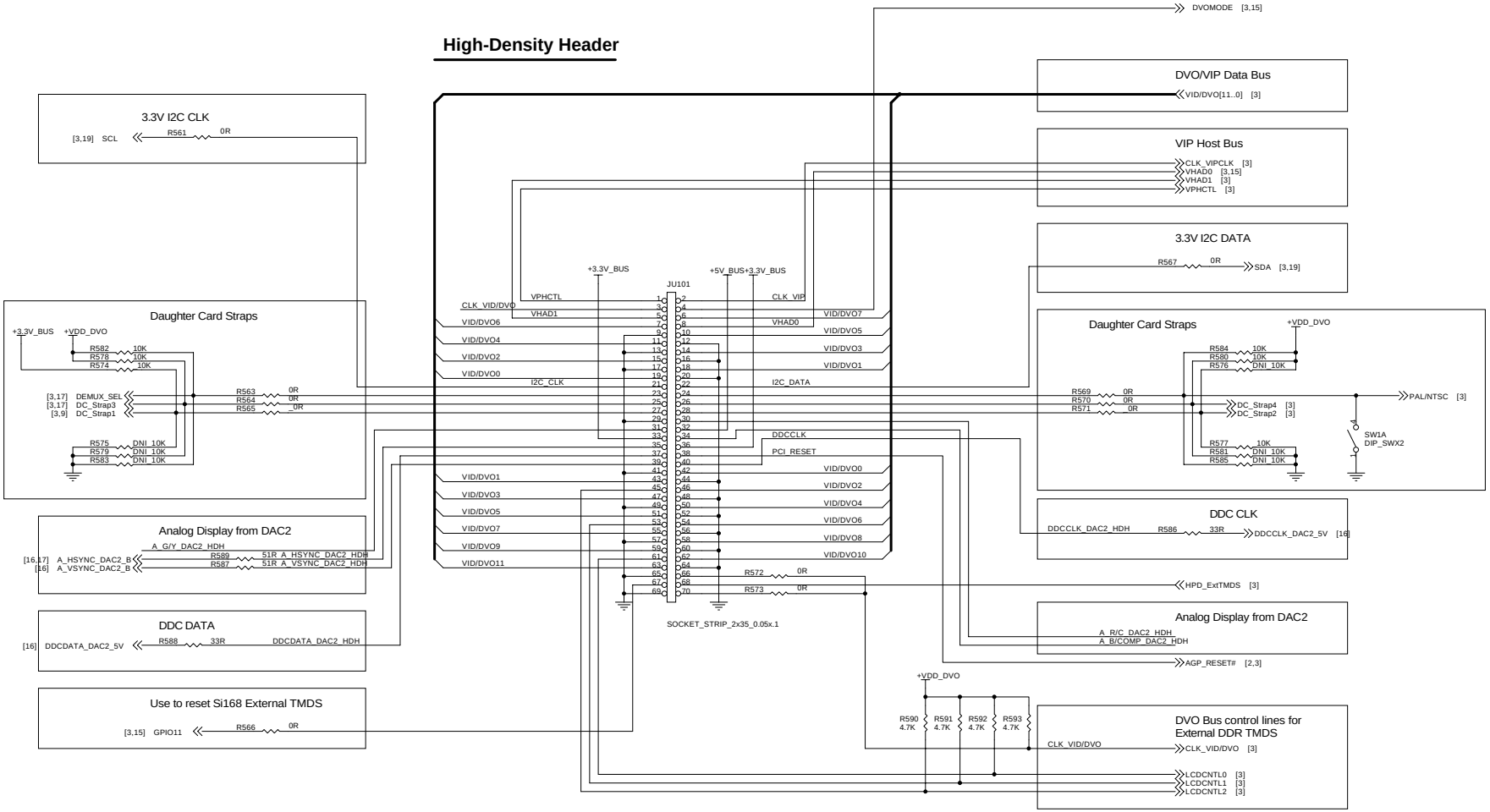
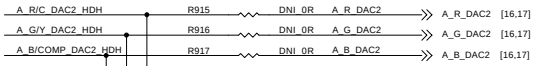
Title	AGP RV350 128M BGA VGA DVI VO	
Size: Custom	Document Number: 105-A034XX-20	Rev: 7
Date: Monday, February 23, 2004	Sheet 13 of 20	

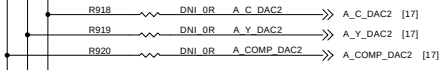
High-Density Header



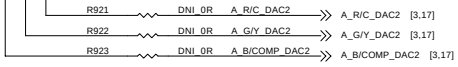
Map DAC2 CRT to HDH



Map DAC2 VO to HDH



Map DAC2 to HDH



STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDS Enabled **0 - Disabled** 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled **0 - Disabled** 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19 0 0 0 1 1 0 1 1	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 -NTSC (on board resistor pull-up)

<Core Design>

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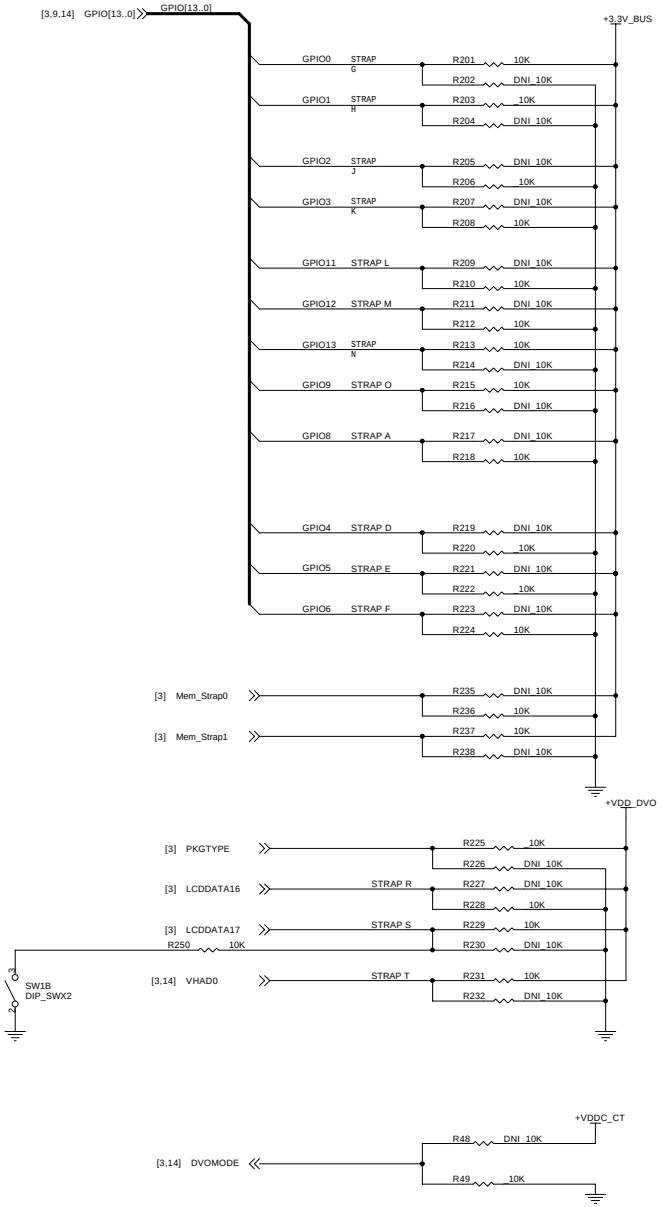
Size C	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 14 of 20	

OPTION STRAPS



STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFBSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(cpuclk) 00 - refclk slightly earlier then feedback 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback **11 - refclk 2 taps earlier then feedback clock**	11
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk **00 - 0 tap delay** 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	1100
ID_DISABLE	GPIO(8)	**0 - Normal operation** 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two throught a jumper.	0
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL **000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16** 000 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x/2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 **11 - two function device. AGP in both functions** If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	11
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present **1 - No slave VIP host port devices reporting presence during reset**	0

STRAP P	INTERRUPT
LOW	**ENABLED (DEFAULT)**
HIGH	DISABLED

MEMORY TYPE STRAPS		
	Mem_Strap0	Mem_Strap1
SAM	**0**	**0**
INF	1	0
HYN	0	1
ELPIDA	1	1

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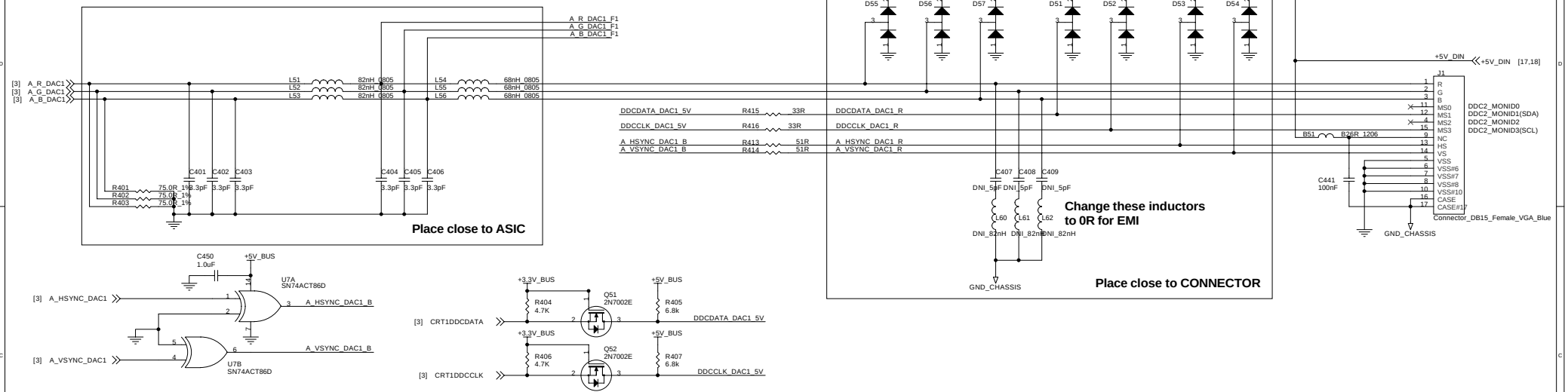
Title: AGP RV350 128M BGA VGA DVI VO

Size: Custom | Document Number: 105-A034XX-20 | Rev: 7

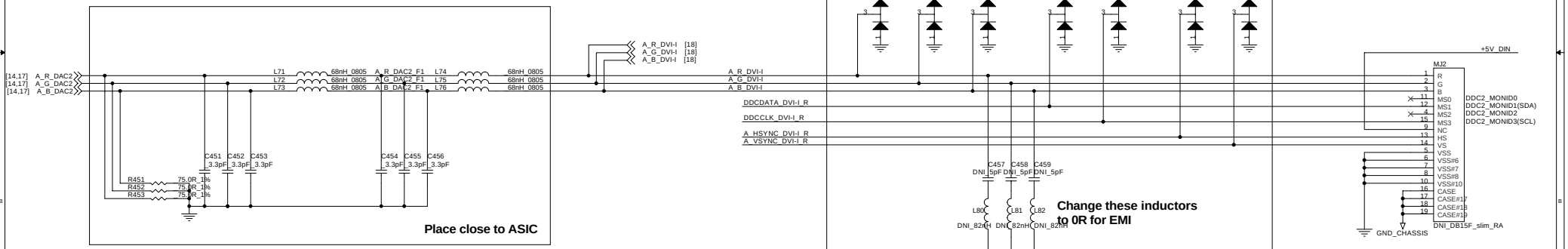
Date: Tuesday, March 23, 2004 | Sheet 15 of 20

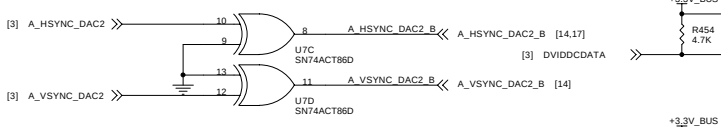
OPTIONAL ESD/HOTPLUG PROTECTION DIODES

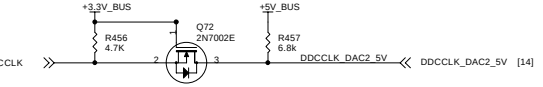
PRIMARY CRT

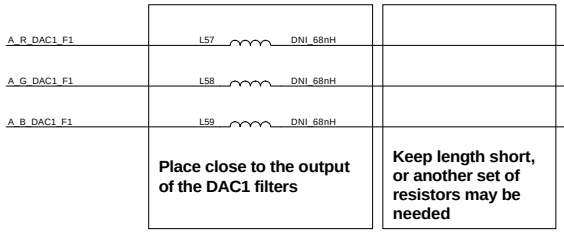


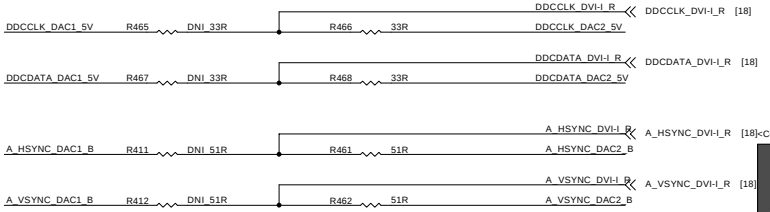
SECONDARY CRT

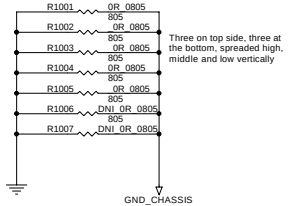












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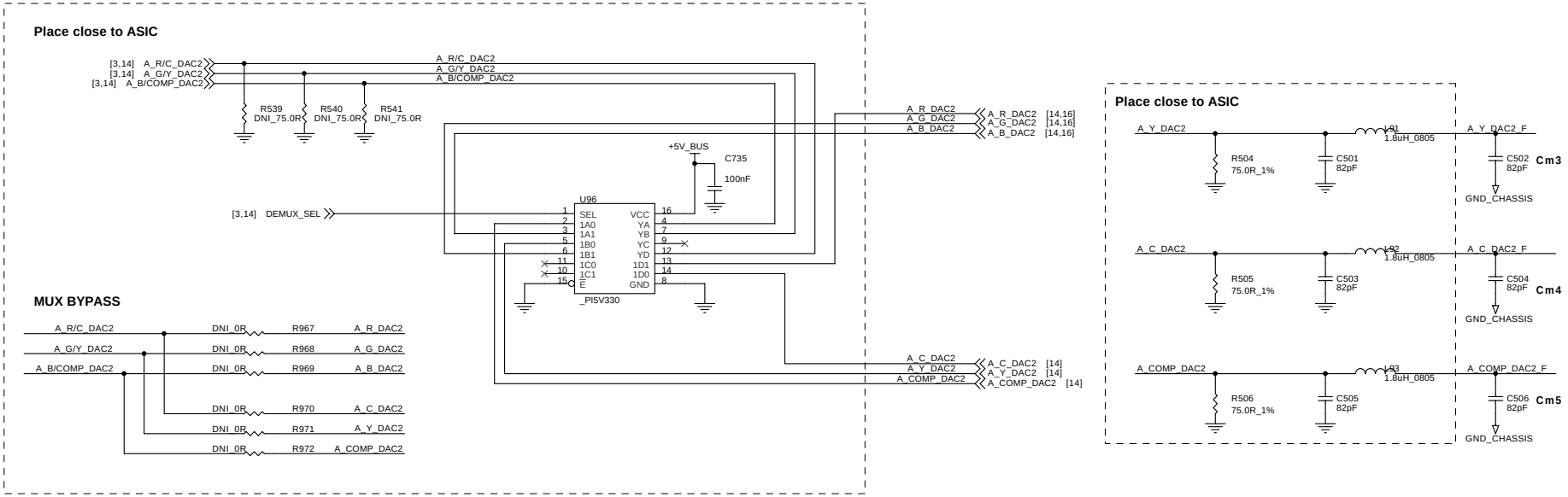
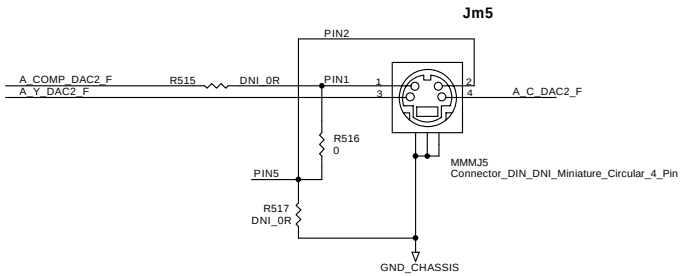
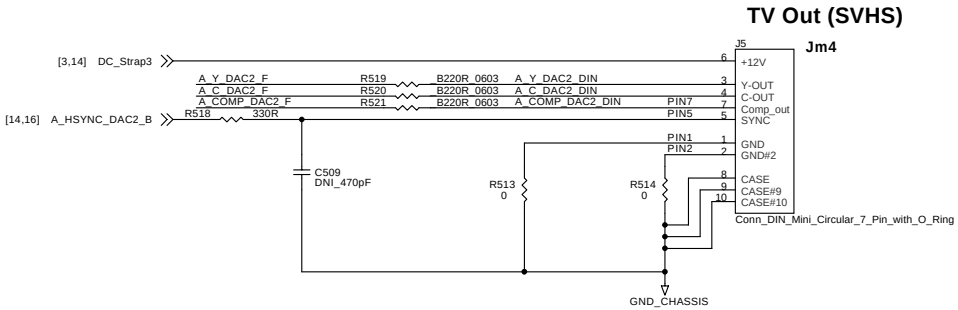
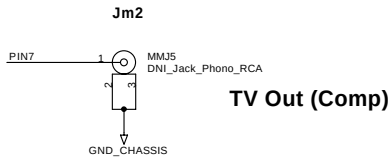
Title	AGP RV350 128M BGA VGA DVI VO	
Size C	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 16 of 20	

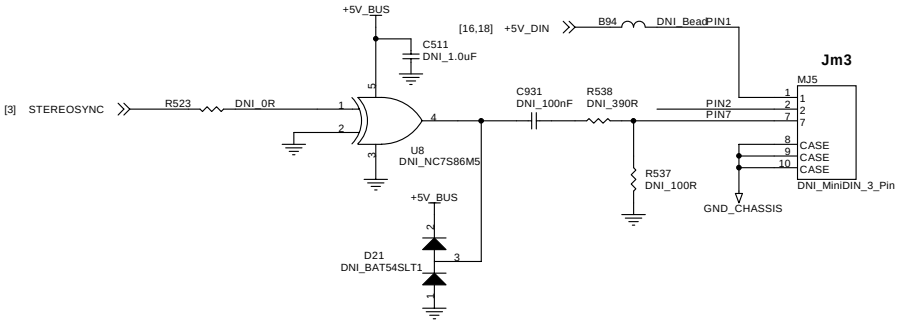








TV Out (Comp)



Jm2, Jm3, Jm4 and Jm5 use the same footprint

<Core Design>

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Title: AGP RV350 128M BGA VGA DVI VO

Size: Custom | Document Number: 105-A034XX-20 | Rev: 7

Date: Wednesday, February 25, 2004 | Sheet 17 of 20

PRIMARY DVI-I CONNECTOR

INSTALL TERMINATION RESISTORS CLOSE TO ASIC

[3] TMDS_TX2N
[3] TMDS_TX2P
R601 330R

[3] TMDS_TX1N
[3] TMDS_TX1P
R602 330R

[3] TMDS_TX0N
[3] TMDS_TX0P
R603 330R

[3] TMDS_TXCP
[3] TMDS_TXCN
R604 330R

[3] HPD

[16] DDCCLK_DVI-I_R
[16] DDCDATA_DVI-I_R

DDCCLK_DVI-I
DDCDATA_DVI-I

[16,17] +5V_DIN
B52 B26R_1206

[16] A_VSYNC_DVI-I_R
[16] A_R_DVI-I
[16] A_G_DVI-I
[16] A_B_DVI-I
[16] A_HSYNC_DVI-I_R

D122
DNI_MMBZ5222BLT1

D121
2.5V_SOT23

R609
100K

R610
20K

IF HOT PLUG DETECT IS NOT REQUIRED
REMOVE ALL THIS LOGIC EXCEPT
FOR 100K PULL DOWN

C510
_100nF

GND_CHASSIS GND_CHASSIS

J2
DVI_A/D

M1	CASE
M3	CASE#M3
1	TMDS Data2-
2	TMDS Data2+
3	TMDS Data2/4 Shield
4	TMDS Data4-
5	TMDS Data4+
6	DDC Clock
7	DDC Data
8	Analog VSYNC
9	TMDS Data1-
10	TMDS Data1+
11	TMDS Data1/3 Shield
12	TMDS Data3-
13	TMDS Data3+
14	+5V Power
15	GND (for +5V)
16	Hot Plug Detect
17	TMDS Data0-
18	TMDS Data0+
19	TMDS Data0/5 Shield
20	TMDS Data5-
21	TMDS Data5+
22	TMDS Clock Shield
23	TMDS Clock+
24	TMDS Clock-
C1	Analog Red
C2	Analog Green
C3	Analog Blue
C4	Analog HYNC
C5	Analog GND
C6	Analog GND#C6
M4	CASE#M4
M2	CASE#M2

<Core Design>

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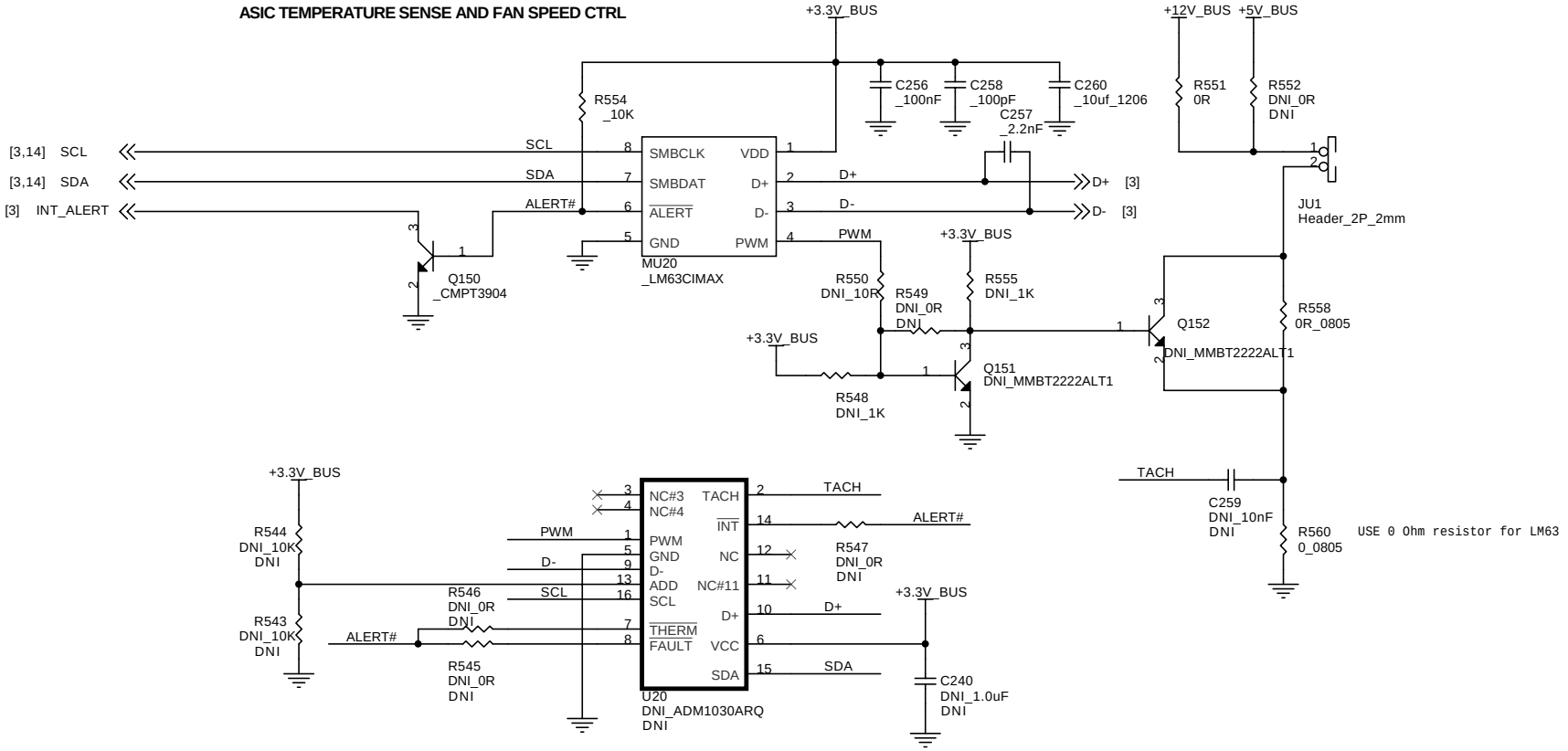
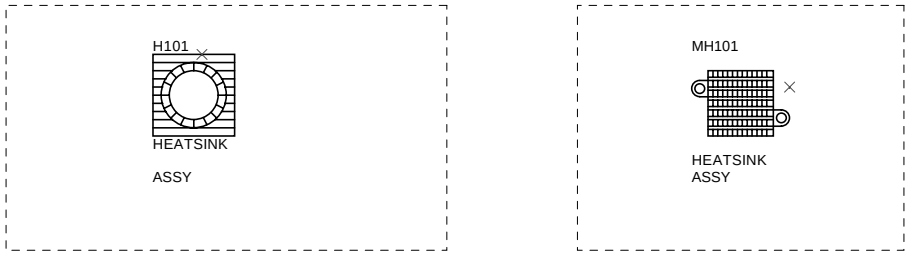
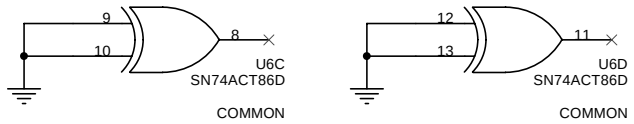
Title	AGP RV350 128M BGA VGA DVI VO	
Size B	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 18 of 20	

ASIC TEMPERATURE SENSE AND FAN SPEED CTRL







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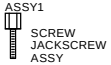
Title	AGP RV350 128M BGA VGA DVI VO	
Size: Custom	Document Number: 105-A034XX-20	Rev: 7
Date: Monday, February 23, 2004	Sheet 19 of 20	

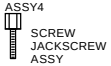
CRT SCREWS

ASSY1



SCREW
JACKSCREW
ASSY

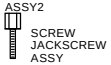
ASSY4



SCREW
JACKSCREW
ASSY

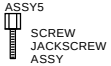
DVI SCREWS

ASSY2



SCREW
JACKSCREW
ASSY

ASSY5



SCREW
JACKSCREW
ASSY

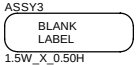
ASSY8

BRACKET

NO_TABS,_VGA,_DIN,_DVI

MISC. BOARD PARTS

ASSY3

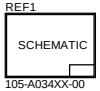


1.5W_X_0.50H

ASSY7

6_X_11
ASSY

REF1



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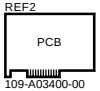

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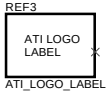

ATI_LOGO_LABEL

<Core Design>

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Title	AGP RV350 128M BGA VGA DVI VO	
Size B	Document Number 105-A034XX-20	Rev 7
Date: Monday, February 23, 2004	Sheet 20 of 20	