# UMC UM8881 HB4 Super Energy Star Green (reverse engineered)

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## Introduction

UMC didn't make "UM8881 HB4 Super Energy Star Green" technical reference public, so I made my own. Pinout obtained *pain*stakingly by measuring my ATC-1415 board. Some pin definitions may be inaccurate, incomplete or missing. The board used for experiment has UM8881F 9536-ETA chip, only 2 SIMM slots, noninterleaved cache up to 512kB. The board has been configured for Am5x86-133, which may cause some pins to be left disconnected and so unidentified. Also different processors have different locations for some pins. The board had also leaked NiCd accu which could damage some traces.

### TODO

Further measurements would be appreciated. Especially for boards with:

- Is CPU address 3 connected to some bank in interleaved cache boards?
- At what cache size configurations are CPU address 18 and 17 connected to the tag SRAM? (on my board the 256kB jumper connects PA17 to tag A14, but the pin is not implemented in the smallest usable tag SRAM)
- Which pins are used for aditional IDSEL on boards with more than 3 PCI devices (including integrated)
- Is pin 99 routed to through AND to turbo led? is it input or output?
- Is pin 170 used somewhere?
- Are pins 202 and 203 routed somewhere?

### References

DRAM pinout and naming used from wikipedia SIMM.

ISA bus pinout and naming used from wikipedia ISA.

PCI bus pinout and naming used from wikipedia Peripheral Component Interconnect.

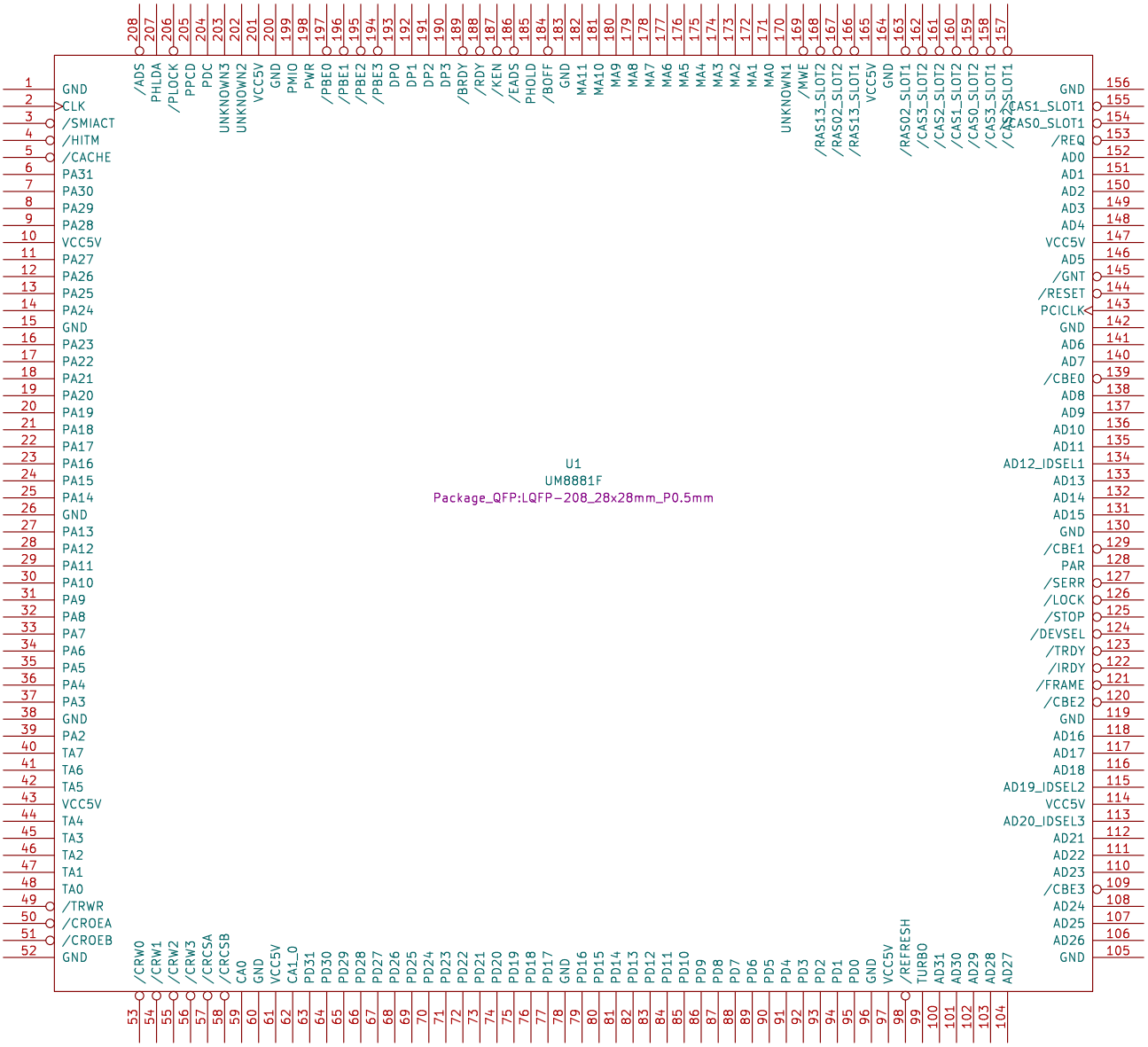
486 pinout from 486-/PODP-Pinout and Differences. NOTICE A13 and A16 is swapped.

Vogons discussion UMC8881/8886 Datasheet. Also MITAC 5023 used as a source of pin names.

Initial kicad symbol generated by Quick KICAD Library Component Builder.

# Pin assignment and description

## Schematic symbol




TODO (regenerate symbol)

## Pin list overview

| | |
|---|---|
| 1 | GND |
| 2 | CLK |
| 3 | /SMIACT |
| 4 | /HITM |
| 5 | /CACHE |
| 6 | PA31 |
| 7 | PA30 |
| 8 | PA29 |
| 9 | PA28 |
| 10 | VCC5V |
| 11 | PA27 |
| 12 | PA26 |
| 13 | PA25 |
| 14 | PA24 |
| 15 | GND |
| 16 | PA23 |
| 17 | PA22 |
| 18 | PA21 |
| 19 | PA20 |
| 20 | PA19 |
| 21 | PA18 |
| 22 | PA17 |
| 23 | PA16 |
| 24 | PA15 |
| 25 | PA14 |
| 26 | GND |
| 27 | PA13 |
| 28 | PA12 |
| 29 | PA11 |
| 30 | PA10 |
| 31 | PA9 |
| 32 | PA8 |
| 33 | PA7 |
| 34 | PA6 |
| 35 | PA5 |
| 36 | PA4 |
| 37 | PA3 |
| 38 | GND |
| 39 | PA2 |
| 40 | TA7 |
| 41 | TA6 |
| 42 | TA5 |
| 43 | VCC5V |
| 44 | TA4 |
| 45 | TA3 |
| 46 | TA2 |
| 47 | TA1 |
| 48 | TA0 |
| 49 | /TRWR |
| 50 | /CROEA |
| 51 | /CROEB |
| 52 | GND |

| | |
|---|---|
| 53 | /CRW0 |
| 54 | /CRW1 |
| 55 | /CRW2 |
| 56 | /CRW3 |
| 57 | /CRCSA |
| 58 | /CRCSB |
| 59 | CA0 |
| 60 | GND |
| 61 | VCC5V |
| 62 | CA1_0 |
| 63 | PD31 |
| 64 | PD30 |
| 65 | PD29 |
| 66 | PD28 |
| 67 | PD27 |
| 68 | PD26 |
| 69 | PD25 |
| 70 | PD24 |
| 71 | PD23 |
| 72 | PD22 |
| 73 | PD21 |
| 74 | PD20 |
| 75 | PD19 |
| 76 | PD18 |
| 77 | PD17 |
| 78 | GND |
| 79 | PD16 |
| 80 | PD15 |
| 81 | PD14 |
| 82 | PD13 |
| 83 | PD12 |
| 84 | PD11 |
| 85 | PD10 |
| 86 | PD9 |
| 87 | PD8 |
| 88 | PD7 |
| 89 | PD6 |
| 90 | PD5 |
| 91 | PD4 |
| 92 | PD3 |
| 93 | PD2 |
| 94 | PD1 |
| 95 | PD0 |
| 96 | GND |
| 97 | VCC5V |
| 98 | /REFRESH |
| 99 | TURBO |
| 100 | AD31 |
| 101 | AD30 |
| 102 | AD29 |
| 103 | AD28 |
| 104 | AD27 |

| | |
|---|---|
| 105 | GND |
| 106 | AD26 |
| 107 | AD25 |
| 108 | AD24 |
| 109 | /CBE3 |
| 110 | AD23 |
| 111 | AD22 |
| 112 | AD21 |
| 113 | AD20_IDSEL3 |
| 114 | VCC5V |
| 115 | AD19_IDSEL2 |
| 116 | AD18 |
| 117 | AD17 |
| 118 | AD16 |
| 119 | GND |
| 120 | /CBE2 |
| 121 | /FRAME |
| 122 | /IRDY |
| 123 | /TRDY |
| 124 | /DEVSEL |
| 125 | /STOP |
| 126 | /LOCK |
| 127 | /SERR |
| 128 | PAR |
| 129 | /CBE1 |
| 130 | GND |
| 131 | AD15 |
| 132 | AD14 |
| 133 | AD13 |
| 134 | AD12_IDSEL1 |
| 135 | AD11 |
| 136 | AD10 |
| 137 | AD9 |
| 138 | AD8 |
| 139 | /CBE0 |
| 140 | AD7 |
| 141 | AD6 |
| 142 | GND |
| 143 | PCICLK |
| 144 | /RESET |
| 145 | /GNT |
| 146 | AD5 |
| 147 | VCC5V |
| 148 | AD4 |
| 149 | AD3 |
| 150 | AD2 |
| 151 | AD1 |
| 152 | AD0 |
| 153 | /REQ |
| 154 | /CAS0_SLOT1 |
| 155 | /CAS1_SLOT1 |
| 156 | GND |

| | |
|---|---|
| 157 | /CAS2_SLOT1 |
| 158 | /CAS3_SLOT1 |
| 159 | /CAS0_SLOT2 |
| 160 | /CAS1_SLOT2 |
| 161 | /CAS2_SLOT2 |
| 162 | /CAS3_SLOT2 |
| 163 | /RAS02_SLOT1 |
| 164 | GND |
| 165 | VCC5V |
| 166 | /RAS13_SLOT1 |
| 167 | /RAS02_SLOT2 |
| 168 | /RAS13_SLOT2 |
| 169 | /MWE |
| 170 | UNKNOWN1 |
| 171 | MA0 |
| 172 | MA1 |
| 173 | MA2 |
| 174 | MA3 |
| 175 | MA4 |
| 176 | MA5 |
| 177 | MA6 |
| 178 | MA7 |
| 179 | MA8 |
| 180 | MA9 |
| 181 | MA10 |
| 182 | MA11 |
| 183 | GND |
| 184 | /BOFF |
| 185 | PHOLD |
| 186 | /EADS |
| 187 | /KEN |
| 188 | /RDY |
| 189 | /BRDY |
| 190 | DP3_/LGNT1 |
| 191 | DP2_/LGNT2 |
| 192 | DP1_/LREQ1 |
| 193 | DP0_/LREQ2 |
| 194 | /PBE3 |
| 195 | /PBE2 |
| 196 | /PBE1 |
| 197 | /PBE0 |
| 198 | PWR |
| 199 | PMIO |
| 200 | GND |
| 201 | VCC5V |
| 202 | /LRDY |
| 203 | /LDEV |
| 204 | PDC |
| 205 | PPCD |
| 206 | /PLOCK |
| 207 | PHLDA |
| 208 | /ADS |

## Pin description

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | GND | power input | Ground |
| 2 | CLK | edge input | Chipset clock, via 10R + buffer to UM8886 pin 51 |
| 3 | /SMIACT | inverted input | Jumper J27, (also near J21 BREQ) |
| 4 | /HITM | inverted input | multiple jumpers |
| 5 | /CACHE | inverted input | J12.1 (via J12.2 to CPU), connected to J13.2 (via J13.1 to J26.2) |
| 6 | PA31 | bidir | CPU address 31 |
| 7 | PA30 | bidir | CPU address 30 |
| 8 | PA29 | bidir | CPU address 29 |
| 9 | PA28 | bidir | CPU address 28 |
| 10 | VCC5V | power input | Power supply +5V |
| 11 | PA27 | bidir | CPU address 27 |
| 12 | PA26 | bidir | CPU address 26 |
| 13 | PA25 | bidir | CPU address 25 |
| 14 | PA24 | bidir | CPU address 24 |
| 15 | GND | power input | Ground |
| 16 | PA23 | bidir | CPU address 23 |
| 17 | PA22 | bidir | CPU address 22 |
| 18 | PA21 | bidir | CPU address 21 |
| 19 | PA20 | bidir | CPU address 20 |
| 20 | PA19 | bidir | CPU address 19 |
| 21 | PA18 | bidir | CPU/cache/tag address 18/16/14, cache pin A16, tag pin A13/CE2 (via 512k 1-2 J1 jumper – closer to U1) |
| 22 | PA17 | bidir | CPU/cache/tag address 17/15/13, cache pin A15, tag pin A14/NC (via 256k 3-4 J1 jumper) |
| 23 | PA16 | bidir | CPU/cache/tag address 16/14/12, cache pin A14, tag pin A11 |
| 24 | PA15 | bidir | CPU/cache/tag address 15/13/11, cache pin A13, tag pin A10 |
| 25 | PA14 | bidir | CPU/cache/tag address 14/12/10, cache pin A2, tag pin A2 |
| 26 | GND | power input | Ground |
| 27 | PA13 | bidir | CPU/cache/tag address 13/11/9, cache pin A3, tag pin A3 |
| 28 | PA12 | bidir | CPU/cache/tag address 12/10/8, cache pin A4, tag pin A4 |
| 29 | PA11 | bidir | CPU/cache/tag address 11/9/7, cache pin A5, tag pin A5 |
| 30 | PA10 | bidir | CPU/cache/tag address 10/8/6, cache pin A6, tag pin A6 |
| 31 | PA9 | bidir | CPU/cache/tag address 9/7/5, cache pin A7, tag pin A7 |
| 32 | PA8 | bidir | CPU/cache/tag address 8/6/4, cache pin A12, tag pin A12 |
| 33 | PA7 | bidir | CPU/cache/tag address 7/5/3, cache pin A0, tag pin A0 |
| 34 | PA6 | bidir | CPU/cache/tag address 6/4/2, cache pin A1, tag pin A1 |
| 35 | PA5 | bidir | CPU/cache/tag address 5/3/1, cache pin A8, tag pin A8 |
| 36 | PA4 | bidir | CPU/cache/tag address 4/2/0, cache pin A9, tag pin A9 |
| 37 | PA3 | output | CPU address 3 |
| 38 | GND | power input | Ground |
| 39 | PA2 | output | CPU address 2 |
| 40 | TA7 | bidir | Tag address, to tag data pin 7 (may have permutation) |
| 41 | TA6 | bidir | Tag address, to tag data pin 6 (may have permutation) |
| 42 | TA5 | bidir | Tag address, to tag data pin 5 (may have permutation) |
| 43 | VCC5V | power input | Power supply +5V |
| 44 | TA4 | bidir | Tag address, to tag data pin 4 (may have permutation) |
| 45 | TA3 | bidir | Tag address, to tag data pin 3 (may have permutation) |
| 46 | TA2 | bidir | Tag address, to tag data pin 2 (may have permutation) |
| 47 | TA1 | bidir | Tag address, to tag data pin 1 (may have permutation), bootstrap J5.2 via 2k2 to GND or VCC5V |
| 48 | TA0 | bidir | Tag address, to tag data pin 0 (may have permutation), bootstrap J4.2 via 2k2 to GND or VCC5V |

| Pin | Name | Type | Description |
|---|---|---|---|
| 49 | /TRWR | inverted output | Cache tag write enable |
| 50 | /CROEA | inverted output | Cache output enable for bank A (or a single bank), via 33R |
| 51 | /CROEB | inverted output | Cache output enable for bank B, possibly also via 33R (reported by mkarcher) |
| 52 | GND | power input | Ground |
| 53 | /CRW0 | inverted output | Cache write enable [7:0], to U5 SRAM |
| 54 | /CRW1 | inverted output | Cache write enable [15:7], to U4 SRAM |
| 55 | /CRW2 | inverted output | Cache write enable [23:16], to U3 SRAM |
| 56 | /CRW3 | inverted output | Cache write enable [32:24], to U2 SRAM |
| 57 | /CRCSA | inverted output | Cache chip select for bank A (or a single bank), via 33R |
| 58 | /CRCSB | inverted output | Cache chip select for bank B, possibly also via 33R (reported by mkarcher) |
| 59 | CA0 | output | Cache address 0 (single or first interleaved), pin A11 |
| 60 | GND | power input | Ground |
| 61 | VCC5V | power input | Power supply +5V |
| 62 | CA1_0 | output | Cache address 1 (single bank), address 0 (second interleaved), pin A10 |
| 63 | PD31 | bidir | CPU (host) data 31 |
| 64 | PD30 | bidir | CPU data 30 |
| 65 | PD29 | bidir | CPU data 29 |
| 66 | PD28 | bidir | CPU data 28 |
| 67 | PD27 | bidir | CPU data 27 |
| 68 | PD26 | bidir | CPU data 26 |
| 69 | PD25 | bidir | CPU data 25 |
| 70 | PD24 | bidir | CPU data 24 |
| 71 | PD23 | bidir | CPU data 23 |
| 72 | PD22 | bidir | CPU data 22 |
| 73 | PD21 | bidir | CPU data 21 |
| 74 | PD20 | bidir | CPU data 20 |
| 75 | PD19 | bidir | CPU data 19 |
| 76 | PD18 | bidir | CPU data 18 |
| 77 | PD17 | bidir | CPU data 17 |
| 78 | GND | power input | Ground |
| 79 | PD16 | bidir | CPU data 16 |
| 80 | PD15 | bidir | CPU data 15 |
| 81 | PD14 | bidir | CPU data 14 |
| 82 | PD13 | bidir | CPU data 13 |
| 83 | PD12 | bidir | CPU data 12 |
| 84 | PD11 | bidir | CPU data 11 |
| 85 | PD10 | bidir | CPU data 10 |
| 86 | PD9 | bidir | CPU data 9 |
| 87 | PD8 | bidir | CPU data 8 |
| 88 | PD7 | bidir | CPU data 7 |
| 89 | PD6 | bidir | CPU data 6 |
| 90 | PD5 | bidir | CPU data 5 |
| 91 | PD4 | bidir | CPU data 4 |
| 92 | PD3 | bidir | CPU data 3 |
| 93 | PD2 | bidir | CPU data 2 |
| 94 | PD1 | bidir | CPU data 1 |
| 95 | PD0 | bidir | CPU data 0 |
| 96 | GND | power input | Ground |
| 97 | VCC5V | power input | Power supply +5V |
| 98 | /REFRESH | inverted input | DRAM refresh, shared with ISA /REFRESH, via R22 (470R) to +5V, via R23 (33R) to UM8886 p145, via C7 to GND |

| Pin | Name | Type | Description |
|---|---|---|---|
| 99 | TURBO | output | TODO, via R38 (10k) to +5V, to U18.2 (AND.I1), AND.I2 to UM8886 pin 54 (SMI2/LB2/KBCI), AND.Q via R88 to turbo LED |
| 100 | AD31 | bidir | PCI Address/Data 31 |
| 101 | AD30 | bidir | PCI Address/Data 30 |
| 102 | AD29 | bidir | PCI Address/Data 29 |
| 103 | AD28 | bidir | PCI Address/Data 28 |
| 104 | AD27 | bidir | PCI Address/Data 27 |
| 105 | GND | power input | Ground |
| 106 | AD26 | bidir | PCI Address/Data 26 |
| 107 | AD25 | bidir | PCI Address/Data 25 |
| 108 | AD24 | bidir | PCI Address/Data 24 |
| 109 | /CBE3 | inverted bidir | PCI command/byte enable 3 |
| 110 | AD23 | bidir | PCI Address/Data 23 |
| 111 | AD22 | bidir | PCI Address/Data 22 |
| 112 | AD21 | bidir | PCI Address/Data 21 |
| 113 | AD20_IDSE | bidir | PCI Address/Data 20, IDSEL slot 3 |
| 114 | VCC5V | power input | Power supply +5V |
| 115 | AD19_IDSE | bidir | PCI Address/Data 19, IDSEL slot 2 |
| 116 | AD18 | bidir | PCI Address/Data 18 |
| 117 | AD17 | bidir | PCI Address/Data 17 |
| 118 | AD16 | bidir | PCI Address/Data 16 |
| 119 | GND | power input | Ground |
| 120 | /CBE2 | inverted bidir | PCI command/byte enable 2 |
| 121 | /FRAME | inverted bidir | PCI frame signal |
| 122 | /IRDY | inverted bidir | PCI initiator ready, via R17 (33R) |
| 123 | /TRDY | inverted bidir | PCI target ready, via R18 (33R) |
| 124 | /DEVSEL | inverted bidir | PCI target selected |
| 125 | /STOP | inverted bidir | PCI target halt request |
| 126 | /LOCK | inverted bidir | PCI locked transaction |
| 127 | /SERR | inverted open collector | PCI system error |
| 128 | PAR | bidir | PCI parity |
| 129 | /CBE1 | inverted bidir | PCI command/byte enable 1 |
| 130 | GND | power input | Ground |
| 131 | AD15 | bidir | PCI Address/Data 15 |
| 132 | AD14 | bidir | PCI Address/Data 14 |
| 133 | AD13 | bidir | PCI Address/Data 13 |
| 134 | AD12_IDSE | bidir | PCI Address/Data 12, IDSEL slot 1 |
| 135 | AD11 | bidir | PCI Address/Data 11 |
| 136 | AD10 | bidir | PCI Address/Data 10 |
| 137 | AD9 | bidir | PCI Address/Data 9 |
| 138 | AD8 | bidir | PCI Address/Data 8 |
| 139 | /CBE0 | inverted bidir | PCI command/byte enable 0 |
| 140 | AD7 | bidir | PCI Address/Data 7 |
| 141 | AD6 | bidir | PCI Address/Data 6 |
| 142 | GND | power input | Ground |
| 143 | PCICLK | edge input | PCI clock input driven via 10R and buffer from UM8886 pin 53 |
| 144 | /RESET | inverted input | PCI bus + main reset, via inverter (U10) to ISA RESET and UM8886 pin 157 |
| 145 | /GNT | inverted input | CPU gets granted PCI bus, driven from UM8886 pin 121 |
| 146 | AD5 | bidir | PCI Address/Data 5 |
| 147 | VCC5V | power input | Power supply +5V |
| 148 | AD4 | bidir | PCI Address/Data 4 |
| 149 | AD3 | bidir | PCI Address/Data 3 |
| 150 | AD2 | bidir | PCI Address/Data 2 |

| Pin | Name | Type | Description |
|---|---|---|---|
| 151 | AD1 | bidir | PCI Address/Data 1 |
| 152 | AD0 | bidir | PCI Address/Data 0 |
| 153 | /REQ | inverted output | CPU requests PCI bus, sent to UM8886 pin 124 |
| 154 | /CAS0_SLO | inverted output | DRAM column address strobe 0, SIMM slot 1 (possible permutations) |
| 155 | /CAS1_SLO | inverted output | DRAM column address strobe 1, SIMM slot 1 (possible permutations) |
| 156 | GND | power input | Ground |
| 157 | /CAS2_SLO | inverted output | DRAM column address strobe 2, SIMM slot 1 (possible permutations) |
| 158 | /CAS3_SLO | inverted output | DRAM column address strobe 3, SIMM slot 1 (possible permutations) |
| 159 | /CAS0_SLO | inverted output | DRAM column address strobe 0, SIMM slot 2 (possible permutations) |
| 160 | /CAS1_SLO | inverted output | DRAM column address strobe 1, SIMM slot 2 (possible permutations) |
| 161 | /CAS2_SLO | inverted output | DRAM column address strobe 2, SIMM slot 2 (possible permutations) |
| 162 | /CAS3_SLO | inverted output | DRAM column address strobe 3, SIMM slot 2 (possible permutations) |
| 163 | /RAS02_SL( | inverted output | DRAM row address strobe 0/2, via buffer to SIMM slot 1 (possible permutations) |
| 164 | GND | power input | Ground |
| 165 | VCC5V | power input | Power supply +5V |
| 166 | /RAS13_SL( | inverted output | DRAM row address strobe 1/3, via buffer to SIMM slot 1 (possible permutations) |
| 167 | /RAS02_SL( | inverted output | DRAM row address strobe 0/2, via buffer to SIMM slot 2 (possible permutations) |
| 168 | /RAS13_SL( | inverted output | DRAM row address strobe 1/3, via buffer to SIMM slot 2 (possible permutations) |
| 169 | /MWE | inverted output | DRAM write enable, via buffer and 10R to all SIMM slots |
| 170 | UNKNOWN | | TODO, possibly DRAM oriented, could be control for a buffer between DRAM and CPU |
| 171 | MA0 | output | DRAM column/row address 0, via buffer |
| 172 | MA1 | output | DRAM column/row address 1, via buffer |
| 173 | MA2 | output | DRAM column/row address 2, via buffer |
| 174 | MA3 | output | DRAM column/row address 3, via buffer |
| 175 | MA4 | output | DRAM column/row address 4, via buffer |
| 176 | MA5 | output | DRAM column/row address 5, via buffer |
| 177 | MA6 | output | DRAM column/row address 6, via buffer |
| 178 | MA7 | output | DRAM column/row address 7, via buffer |
| 179 | MA8 | output | DRAM column/row address 8, via buffer |
| 180 | MA9 | output | DRAM column/row address 9, via buffer |
| 181 | MA10 | output | DRAM column/row address 10, via buffer |
| 182 | MA11 | output | DRAM column/row address 11, via 10R |
| 183 | GND | power input | Ground |
| 184 | /BOFF | inverted output | CPU backoff from bus |
| 185 | PHOLD | output | CPU bus hold, pin E15 |
| 186 | /EADS | inverted output | CPU external address strobe |
| 187 | /KEN | inverted output | CPU cache enable |
| 188 | /RDY | inverted output | CPU non-burst ready, pin F16 |
| 189 | /BRDY | inverted output | CPU burst ready, pin H15 |
| 190 | DP3_/LGNT | bidir | CPU data parity 3, VLB local grant 1 (output) |
| 191 | DP2_/LGNT | bidir | CPU data parity 2, VLB local grant 2 (output) |
| 192 | DP1_/LREQ | bidir | CPU data parity 1, VLB local request 1 (input) |

| Pin | Name | Type | Description |
|---|---|---|---|
| 193 | DP0_/LREQ | bidir | CPU data parity 0, VLB local request 2 (input) |
| 194 | /PBE3 | inverted input | CPU byte enable 3 |
| 195 | /PBE2 | inverted input | CPU byte enable 2 |
| 196 | /PBE1 | inverted input | CPU byte enable 1 |
| 197 | /PBE0 | inverted input | CPU byte enable 0 |
| 198 | PWR | input | CPU write/read bus cycle, goes to jumpers (J15 INV, J17) |
| 199 | PMIO | input | CPU memory/IO bus cycle |
| 200 | GND | power input | Ground |
| 201 | VCC5V | power input | Power supply +5V |
| 202 | /LRDY | input | VLB target ready, not implemented has a pull up via 4k7 (RP12) to VCC5V, TODO direction |
| 203 | /LDEV | input | VLB device cycle, not implemented has a pull up via 4k7 (R52) to VCC5V, TODO direction |
| 204 | PDC | input | CPU data/control bus cycle, pin M15 |
| 205 | PPCD | input | Page cache disable, pin J17 |
| 206 | /PLOCK | inverted input | CPU bus lock, pin N15 |
| 207 | PHLDA | input | CPU hold acknowledge, pin P15 |
| 208 | /ADS | inverted input | CPU address status |

# Registers

## North Bridge

```
50.80  L2 cache enable
50.40  L2 cache mode (WT/WB)
50.30  Cache read burst (3-2-2-2/3-1-1-1/2-2-2-2/2-1-1-1)
50.08  Two banks of cache
50.07  L2 cache size (none/64K/128K/256K/512K/1024K/resvd/resvd)

51.C0  Read WS (3/2/1/0)
51.30  Write WS (3/2/1/0)
51.04  A0000-BFFFF(?) PCI write merge
51.02  Set after memory test, cleared for L1WB
51.01  Tag allocation (7Tag+1Dirty/8Tag+0Dirty)

52.80  CPU to PCI Post Write (1WS/0WS)
52.70  bank 2/3 total size (1M/2M/4M/8M/16M/32M/64M/128M)
52.08  swap banks 0/1 with 2/3
52.07  bank 0/1 total size (1M/2M/4M/8M/16M/32M/64M/128M)

53.80  CPU to PCI Burst Write
53.40  Burst copy back option
53.20  swap bank 2/3
53.10  swap bank 0/1
53.0C  bank 2/3 row mode (1*double sided/1*single sided/2*single sided/2*double sided)
53.03  bank 0/1 row mode (1*double sided/1*single sided/2*single sided/2*double sided)

54.80  DC00 shadow read enable
54.40  D800 shadow read enable
54.20  D400 shadow read enable
54.10  D000 shadow read enable
54.08  CC00 shadow read enable
54.04  C800 shadow read enable
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54.02  C0/C4 shadow read enable
54.01  ESEG shadow read enable

55.80  FSEG shadow read enable
55.40  Global shadow write protect
55.20  System BIOS cachable
55.01  Video BIOS cachable

56.FF  Memory hole base (in 64K blocks)

57.80  Memory hole enabled/disabled
57.70  Memory hole size (64k/128k/256k/1M/2M/4M/8M/off)

58.FF  0F if system BIOS cachable

59.FF  00 if system BIOS cachable

5A.40  Force cache hit
5A.10  Enable memory parity
5A.02  Some kind of deturbo
5A.01  Cleared during processor clock measurement

5C.FF  SMRAM base A27..A20

5D.80  Early Cache Write mode
5D.10  Slow Referesh
5D.0F  SMRAM base A31..A28

60.20  Set when enabling classic AMD SMRAM
60.02  Disable memory(?) parity
60.01  Open SMRAM space
61.C0  EDO mode? (no/resvd/resvd/yes)

61.08  EDO speed (4-2-2-2/3-1-1-1)
61.02  Cyrix L1WB mode

62.01  Set on early boot for revision "E"
62.02  Burst mode (interleaved/linear)
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## South Bridge

There seems to be differences between UM886N (from mitac schematic) and UM8886BF in the keyboard connection. On ATC-1415 the keyboard clock is connected to UM8886BF pin 57 but UM886N has this pin labeled PGP1/LDEV#/GA20 and the keyboard input KBCLK is on pin 55 instead.

Also the keyboard data leads to pin 56, which is called PGP0(RC#*). UM886N could have keyboard input on pin 54m which is labeled “SMI2#/LB2#/KBCI”.

Data bus for BIOS and address/data bus for RTC is buffered via 74F245 and then connected to ISA. Transmit/receive T/R pin 1 of 74F245 is driven from UM8886BF pin 41 XDIR/PGP3/TCWR. Output enable OE pin 19 is driven from UM8886BF pin 40 XDEN/PGP2/AS01.

```
40.10  Set on B2 revision, but cleared if no PS/2 mouse
40.04  PCI posted memory write
40.03  IBC devsel decoding (medium/slow/fast/resvd?)

41.40  Disable parity check (maybe PCI SERR#?)
41.20 Set during UM8886BF FIFO mode and restored to prior state afterward
```

```
41.04  Enhance PCI performance (enabled/disabled) // PCI bus park option (enabled/disabled)

43.F0  INTA target IRQ
43.0F  INTB target IRQ

44.F0  INTC target IRQ
44.0F  INTD target IRQ

45.04  Set on B2 revision
45.01  Set on B2 revision, but cleared if no PS/2 mouse

46.80  PM IRQ (10/15)
46.40  PM interrupt method (SMI/IRQ)
46.10  Preempt PCI master option
46.08  INTD enabled
46.04  INTC enabled
46.02  INTB enabled
46.01  INTA enabled

47.40  Enable flash writes (0=enabled, 1=disabled). Interop with 57.4 unknown.
47.08  INTD level triggered
47.04  INTC level triggered
47.02  INTB level triggered
47.01  INTA level triggered

50.80  Set if PCI video BIOS is installed
50.01  Set by bootblock after

51.FE  Size of RAM in units of 4M (rounded down, exception: 4M if rounding down results in 0M)

56.80
56.60  Cleared by boot block, under some circumstances set by video card setup
56.0C  KBD clock (7MHz/by4/by3/by2)
56.03  ISA clock (by3/by4/by2/resvd?)

57.20  Set to flash. For whatever reason
57.10  Set on B2 revision
57.08  Keyboard Emulation
57.04  Some bit used for flash write protection (Guessed: GPO, but seems wrong)
  8886AF/8886BF: Shuttle HOT433 and Biostar UUD8433: Set = Protected, Clear = Writeable
  8886F:         Gigabyte GA486IM:                   Clear = Protected, Set = Writeable
57.03  IO recovery time (2BLCK/4BCLK/8BCLK/12BCLK)

70.80  Monitor PCI4 master activity
70.40  Monitor PCI3 master activity
70.20  Monitor PCI2 master activity
70.0F  Green Timer minutes (0.5/1/2/4/8/16/32/64/128/256/512/rsvd/rsvd/rsvd/disable/0.25)

71.80  Monitor PCI1 master activity
71.40  Monitor LPT access
71.20  Monitor COM access
71.10  Monitor ISA DMA master access
71.08  Monitor IDE access
71.04  Monitor Floppy access
71.02  Monitor Graphics card access
```

```
72.80  Monitor extra region A9
72.7E  Monitor extra region mask (1=don't care for A0..A5) Really A0?
72.01  Monitor VL slave access

73.FF  Monitor extra region A8-A1

74.01  Monitor ISA shared memory access (A0000-D0000)

76.40  Set in flash-related code
76.30  SMI interface mode (Intel/Cyrix classic/?/AMD classic)
76.08  Will be set by non-PCI VGA access? Cleared and probed in write-merge setup code
76.04  Cleared by APM init
76.02  Set by APM CPU idle, cleared by APM init

82.03  Set on B2 revision to 3

90.08  Wake-Up on IRQ3
90.10  Wake-Up on IRQ4
90.20  Wake-Up on IRQ5
90.40  Wake-Up on IRQ6
90.80  Wake-Up on IRQ7

91.01  Wake-Up on IRQ8
91.02  Wake-Up on IRQ9
91.04  Wake-Up on IRQ10
91.08  Wake-Up on IRQ11
91.10  Wake-Up on IRQ12
91.40  Wake-Up on IRQ14
91.80  Wake-Up on IRQ15

A0     Set to 0 by Boot Block
       Set to 34 by APM init (SMI mask?, 1 = enable)

A2.01  SMM event 0
A2.02  SMM event 1
A2.04  SMM event 2
A2.08  SMM event 3
A2.10  SMM event 4
A2.20  SMM event 5
A2.40  SMM event 6
A2.80  SMM event 7

A4.03  CPU-to-PCI (2:1/1:1/3:2/resvd?)
```

## IDE controller (only on 8886BF)

The UM8886BF FIFO is 60 bytes in size. There is no intelligence of sector size, multiple sector transfers, ATA vs. ATAPI commands, etc. so the UM8886BF has to be told when to stop reading from the drive by flipping from filling to draining mode at the correct moment, then from draining to disabled when done, on every transfer. This requires changes to the IRQ 14/15 handler. The FIFO cannot just be enabled at boot.

The UM8886BF bus mastering does not support hardware scatter-gather I/O, limiting its utility in a multitasking OS as the driver has to watch register 58h count down to zero before loading the address of the next physical page. There are also alignment restrictions leading to an unaligned head/tail that gets accessed in FIFO PIO or plain PIO mode when doing a bus master read.

The UM8886AF FIFO is 8 bytes in size, and there is no bus mastering, and it doesn't use PCI configuration registers as was already shown above, and doesn't show up as a PCI IDE controller in the list of PCI devices, as if it were a VLB interface. The IDE portion of UM8886AF was also sold as a discrete UM8673 chip on a PCI card but with jumper configuration: Re: UMC IDE/EIDE controller datasheets

The UM8886F lacks IDE and on some boards, is paired with a CMD640 or other non-UMC PCI IDE chip.

```
40.08 Set when secondary interface owns FIFO, clear for primary or FIFO disabled
40.40 Set when FIFO is being accessed using bus mastering, clear otherwise
40.20 Set when FIFO is being accessed using PIO, clear otherwise
40.10 Set when FIFO is filling, clear when draining or disabled

41.80  Enable primary channel
41.40  Enable secondary channel
41.0F Unknown, set to 0D if north bridge is UM8881N/UM8891N or 09 otherwise
41.04  Cleared above PCI33

42.FF  Set to 33 on boot if north bridge is NexGen/UM8881N/UM8891N or 30 otherwise

43.C0  Something for PM (0=fast, 3=slow)
43.30  Something for PS
43.0C  Something for SM
43.03  Something for SS

44.F0  Another thing for PM (2=fast, 12=slow)
44.0F  Another thing for PS

45.F0  Another thing for SM
45.0F  Another thing for SS

46.F0  Third thing for PM (0=fast, 12=slow)
46.0F  Third thing for PS

47.F0  Third thing for SM
47.0F  Third thing for SS

48-49  just like 44-45

4A-4B  just like 46-47

54-57 Bus mastering physical memory address

58-59 Bus mastering number of DWORDs remaining to transfer
```

## IO 108, key: 4A/6C (only before 8886BF)

```
B0.40  Enable secondary IDE channel

B2.F0  Something for PM (0=fast, 4=slow)
B2.0F  Something for PS

B3.F0  Something for SM
B3.0F  Something for SS

B4.F0  Another thing for PM (3=fast, 12=slow)

B5.0F  Another thing for PS
```

```
B6.F0  Another thing for SM
B6.0F  Another thing for SS

B7.F0  Third thing for PM (2=fast, 12=slow)
B7.0F  Third thing for PS

B8.F0  Third thing for SM
B8.0F  Third thing for SS
```