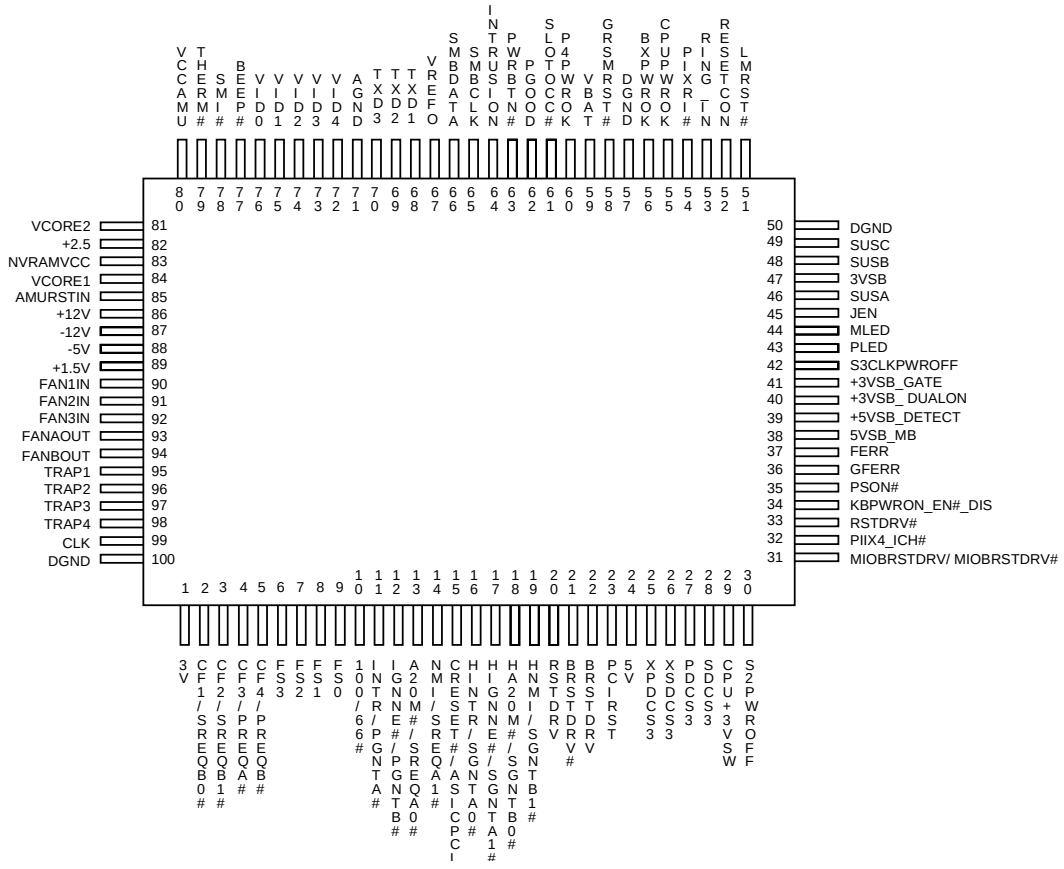
AS99127F Pin Definition

ASIC for ASUSTek

Pin No.	Pin Name	Pin No.	Pin Name
1	3V	51	$\overline{\text{LMRST}}$
2	CF1/SREQB0#	52	RESETCON
3	CF2/SREQB1#	53	RING_IN
4	CF3/PREQA#	54	$\overline{\text{PIXRI}}$
5	CF4/PREQB#	55	CPUPWROK
6	FS3	56	BXPWROK
7	FS2	57	DGND**
8	FS1	58	$\overline{\text{GRSMRST}}$
9	FS0	59	VBAT
10	100/66#	60	P4PWROK
11	INTR/PGNTA#	61	$\overline{\text{SLOTOCC}}$
12	$\overline{\text{IGNNE}}$ /PGNTB#	62	PGOOD
13	$\overline{\text{A20M}}$ /SREQA0#	63	$\overline{\text{PWRBTN}}$
14	NMI/SREQA1#	64	INTRUSION
15	$\overline{\text{CRESET}}$ /ASICPCLK	65	SMBCLK
16	HINTR/SGNTA0#	66	SMBDATA
17	$\overline{\text{HIGNNE}}$ /SGNTA1#	67	VREF(O/Analog)
18	$\overline{\text{HA20M}}$ /SGNTB0#	68	TXD1(I/Analog)
19	HNMI/SGNTB1#	69	TXD2(I/Analog)
20	RSTDRV	70	TXD3(I/Analog)
21	$\overline{\text{BRSTDRV}}$	71	AGND
22	BRSTDRV	72	VID4
23	$\overline{\text{PCIRST}}$	73	VID3
24	5V	74	VID2
25	$\overline{\text{XPDCS3}}$	75	VID1
26	$\overline{\text{XSDCS3}}$	76	VID0
27	$\overline{\text{PDCS3}}$	77	$\overline{\text{BEEP}}$
28	$\overline{\text{SDCS3}}$	78	$\overline{\text{SMI}}$
29	CPU+3VSW	79	$\overline{\text{THERM}}$
30	$\overline{\text{S2PWROFF}}$	80	VCCAMU(Power)
31	MIOBRSTDRV/ MIOBRSTDRV#	81	VCORE2(I/Analog)
32	PIIX4_ICH# **	82	+2.5(I/Analog)
33	RSTDRV#(5V)**	83	NVRAMVCC
34	KBPWRON_EN#_DIS	84	VCORE1(I/Analog)
35	$\overline{\text{PSON}}$	85	AMURSTIN
36	MEMW#	86	+12V(I/Analog)
37	WP_MEMW#	87	-12V(I/Analog)

38	5VSB_MB	88	-5V(I/Analog)
39	+5VSB_DETECT	89	+1.5V(I/Analog)
40	$\overline{\text{+3VSB\_DUALON}}$	90	FAN1IN
41	+3VSB_GATE	91	FAN2IN
42	S3CLKPWROFF	92	FAN3IN
43	PLED	93	FANAOUT
44	MLED	94	FANBOUT
45	JEN	95	TRAP1
46	$\overline{\text{SUSA}}$	96	TRAP2
47	3VSB	97	TRAP3
48	$\overline{\text{SUSB}}$	98	TRAP4
49	$\overline{\text{SUSC}}$	99	CLK
50	DGND	100	DGND

PIN CONFIGURATION



PIN DESCRIPTION

IN_t- TTL level input.
IN_c- CMOS level input.

$IN_{t\text{-}1K\text{-}5V\text{-}up}$- TTL level input with 1Kohm 5V pull-up.
$IN_{t\text{-}10K\text{-}5V\text{-}up}$- TTL level input with 10Kohm 5V pull-up.
$IN_{t\text{-}100K\text{-}3VSB\text{-}up}$- TTL level input with 100Kohm 3VSB pull-up.
$IN_{t\text{-}1K\text{-}down}$- TTL level input with 1Kohm pull-down.
$IN_{t\text{-}100K\text{-}down}$- TTL level input with 100Kohm pull-down.
$IN_{tx\text{-}100K\text{-}down}$- Special TTL level input with 100Kohm pull-down.
IN_{ts}- TTL level input with schmitt-trigger.
OD $_{10K\text{-}3V\text{-}up}$ - Open-drain with 10Kohm 3V pull-up, 8mA sink current.
OD $_{4.7K\text{-}3V\text{-}up}$ - Open-drain with 4.7Kohm 3V pull-up, 8mA sink current.
OD $_{2.2K\text{-}2.5V\text{-}up}$ - Open-drain with 2.2Kohm 2.5V pull-up, 8mA sink current.
OD_8- Open-drain with 8mA sink current.
OD_{12}- Open-drain with 12mA sink current.
OD_{16}- Open-drain with 16mA sink current.
OD_{48}- Open-drain with 48mA sink current.
OUT_4- Output buffer with 4mA drive/sink current.
OUT_8- Output buffer with 8mA drive/sink current.
OUT_{16}- Output buffer with 16mA drive/sink current.
I/O_{8ts}- TTL level bi-directional pin with schmitt-trigger, and ouput with 8mA drive/sink current.
$I/OD_{8t\text{-}10K\text{-}5V\text{-}up}$- TTL level bi-directional pin with open-drain output 8mA sink current, 10Kohm 5V pull-up.

SYMBOL	PIN No.	I/O	Function
3V	1		
CF1/SREQB0#	2	OD $_{10K\text{-}3V\text{-}up}/IN_t$	
CF2/SREQB1#	3	OD $_{10K\text{-}3V\text{-}up}/IN_t$	
CF3/PREQA#	4	OD $_{10K\text{-}3V\text{-}up}/OUT_8$	
CF4/PREQB#	5	OD $_{10K\text{-}3V\text{-}up}/OUT_8$	
FS3	6	OD $_{10K\text{-}3V\text{-}up}$	
FS2	7	OD $_{10K\text{-}3V\text{-}up}$	
FS1	8	OD $_{10K\text{-}3V\text{-}up}$	
FS0	9	OD $_{10K\text{-}3V\text{-}up}$	
100/66#	10	OD $_{10K\text{-}3V\text{-}up}$	
INTR/PGNTA#	11	IN_t	
IGNNE#/PGNTB#	12	IN_t	
A20M#/SREQA0#	13	IN_t	
NMI/SREQA1#	14	IN_t	
CRESET#/ASICPCLK	15	IN_t	
HINTR/SGNTA0#	16	OD $_{2.2K\text{-}2.5V\text{-}up}/OUT_{16}$	
HIGNNE#/SGNTA1#	17	OD $_{2.2K\text{-}2.5V\text{-}up}/OUT_{16}$	
HA20M#/SGNTB0#	18	OD $_{2.2K\text{-}2.5V\text{-}up}/OUT_{16}$	
SYMBOL	**PIN No.**	**I/O**	**Function**
HNMI/SGNTB1#	19	OD $_{2.2K\text{-}2.5V\text{-}up}/OUT_{16}$	
RTSDRV	20	$IN_{t\ 1K\text{-}5V\text{-}up}$	
BRSTDRV#	21	OUT_{16}	

BRSTDRV	22	OUT_{16}	
PCIRST#	23	OUT_{16}	
5V	24		
XPDCS3#	25	IN_{t}	
XSDCS3#	26	IN_{t}	
PDCS3#	27	OUT_{16}	
SDCS3#	28	OUT_{16}	
CPU+3VSW	29	OUT_{8}	
S2PWROFF	30	OUT_{8}	
MIOBRSTDRV/ MIOBRSTDRV#	31	OUT_{8}	
PIIX4/ICH#	32	IN_{t}	Pull-up to high for PIIX4 and pull-down to low for ICH.
RSTDRV#	33	$IN_{t\text{-}1K\text{-}down}$	
KBPWRON_EN#_DIS	34	OUT_{8}	
PSON#	35	OUT_{16}	
GFERR#	36	$IN_{tx\text{-}100K\text{-}down}$	
FERR#	37	$OD_{4.7K\text{-}3V\text{-}up}$	
5VSB_MB	38		
+5VSB_DETECT	39	OD_{16}	
+3VSB_DUALON	40	OD_{8}	
+3VSB_GATE	41	OUT_{8}	
S3BXCLKSTOP	42	OUT_{8}	
MLED	43	OD_{16}	
PLED	44	OD_{16}	
JEN	45	IN_{c}	
SUSA#	46	IN_{c}	
3VSB	47		
SUSB#	48	IN_{c}	
SUSC#	49	IN_{c}	
DGND	50		
LMRST#	51	$IN_{t\text{-}100K\text{-}3VSB\text{-}up}$	
RESETCON	52	IN_{t}	
RING_IN	53	IN_{c}	
PIXRI#	54	OUT_{8}	
CPUPWROK	55	OUT_{8}	
BXPWROK	56	OUT_{8}	
DGND	57		
SYMBOL	**PIN No.**	**I/O**	**Function**
GRSMRST#	58	OUT_{4}	
VBAT	59		
P4PWROK	60	OUT_{4}	
SLOTOCC#	61	IN_{t}	

PGOOD	62	IN_t	
PWRBTN#	63	IN_{ts}	
INTRUSION	64	IN_{ts}	
SMBCLK	65	IN_{ts}/OD_8	
SMBDAT	66	IN_{ts}/OD_8	
VREF	67	Analog Output	
TXD1	68	Analog Input	
TXD2	69	Analog Input	
TXD3	70	Analog Input	
AGND	71	Analog GND	
VID4	72	I/O_{8ts}	
VID3	73	I/O_{8ts}	
VID2	74	I/O_{8ts}	
VID1	75	I/O_{8ts}	
VID0	76	I/O_{8ts}	
BEEP#	77	OD_{48}	
SMI#	78	OD_{12}	
THERM#	79	OD_{12}	
VCCAMU	80	5V for AMU	
VCORE2	81	Analog Input	
+2.5V	82	+2.5V power Input	
NVRAMVCC	83	VCC for NVRAM	
VCORE1	84	Analog Input	
AMURSTIN	85	IN_{ts}	GPO1~GPO12, GPO15and CLKRST# are reset when LMRST#, AMURSTIN, or GRSMRST# is asserted.
+12V	86	Analog Input	
-12V	87	Analog Input	
-5V	88	Analog Input	
+1.5V	89	Analog Input	
FANIN1	90	IN_{ts}	
FANIN2	91	IN_{ts}	
FANIN3	92	IN_{ts}	
FANAOUT	93	Analog Output	Output range from 0V to 4.68V. 16 different voltage levels are provided including 0V and 4.68V.

SYMBOL	PIN No.	I/O	Function
FANBOUT	94	Analog Output	Output range from 0V to 4.68V. 16 different voltage levels are provided including 0V and 4.68V.
TRAP1	95	$IN_{t\text{-}10K\text{-}5V\text{-}up}$	
TRAP2	96	$IN_{t\text{-}100K\text{-}down}$	
TRAP3	97	$IN_{t\text{-}100K\text{-}down}$	
TRAP4	98	$IN_{t\text{-}100K\text{-}down}$	
CLK	99	IN_t	
DGND	100		

AMU SPECIFICATIONS

ASUSTeK Management Unit spec.

Allen S.C. Wang

June 25, 1998

rev 1.10

0. Revision history

19-Jun-98	Put all SUSTEK ASIC" related control/status registers in one of the LM75-like device to avoid LM78 I2C address non-registration problem.
2-Sep-98	Confirm to include 1Kbyte I2C NVRAM.
2-Sep-98	One trap pin is applied to set the I2C address of environment monitor (the extended set for LM78)
2-Sep-98	Register field are defined to identify the use of transistor or thermal diode as a sense device.
2-Sep-98	Primary LM75 gets I2C address of 1001001b. The 2nd Lm75 gets I2C address 1001000b.
2-Sep-98	The fan control output is now defined as 4mA drive and 16-level DAC from 0V to +4.68V.
2-Sep-98	Due to the increase of register and the compatability of former environment monitor, register bank concept has been adopted and three more register banks are used to access 1) primary LM75, 2) secondary LM75, and 3) control register.
2-Sep-98	In order to adapt to the possible process migration for the thermal sense device (especially for transistor and Intel thermal diode), offset registers are added to be able to adjust the reported temperature output and then compensate the change of different process. temperature adjust 1/2 registers are defined to be added before the datum has been accessed by the related S/W.
2-Sep-98	Register 50~55h in Bank0 are now reserved for the ASIC vendor to implement their own design for production test. There should be no impact for system H/W or S/W design.
2-Sep-98	Add bit<4> in register 57h/bank#0 to enable/disable the beeper output for FAN3 interrupt generation.
2-Sep-98	Register 5Bh, 5Ch in Bank #0 are reserved. Register 5Bh in Bank #0 are changed to indicate the use of thermister, 3904 transistor, or Intel thermal diode.
2-Sep-98	To cooperate the multiple voltage sources monitoring, Interrupt Status 3, SMI# Mask 3 registers are moved to Bank #3. New registers are added to enable/disable the beeper under various violation detected.
2-Sep-98	The alarm of beeper is now totally de-coupled from the set/reset of interrupt status. This is because that interrupt status will be cleared once it has been accessed. However, if the abnormal situation persists, related interrupt status bit will be set again. So, the beeper will beep-stop-beep-stop..... A set of beeper enable/disable status registers are provided to independently control the enable/disable of beeper. Noted that those register will be set in the same time when the corresponding interrupt status is set. However, it won be cleared until a write has been performed to clear it. In the mean time, interrupt status register will still be cleared when a read access is launched for it. Register 56h/57h are renamed to Beeper Mask registers to reflect this fact. Also, bit3 and bit4 definition in register 57h are changed.
2-Sep-98	For safety, register 5Eh and 5Fh are also moved to bank#3.
2-Sep-98	Value RAM will be extended to include all the 14 monitored voltages.
2-Sep-98	A pull-up on TRAP2/3/4 pins indicate either a 3904 transistor or Intel thermal diode is applied While a pull-down (default) on those pins indicate the thermister is adopted.
2-Sep-98	The voltage monitor pins are connected to various voltage source as below. Be careful for current leakage on the battery or standby related pins. VIN7-> +5VSB VIN8-> CMOS battery VIN9-> 2.5V VIN10-> 1.5V VIN11-> NVRAM battery VIN12-> +3VSB VIN13-> LOAD test

17-Sep-98	Add VID Input/Output control register and GPO13 to control MSG_LED off(81h). Fix TXD* register assignment error(10h~12h). Change 83781 clock default value(4Bh). Add NVRAM control register(5Ch). Add ”bank” value for Appendix LM75 (00h~03h, 80h~82h).
22-Sep-98	The FANAOUT, FANBOUT fan speed control output driving capacity is now defined to drive a high impedance OP such that we don need large current on those pins. An output directly from the DAC is acceptable. The OP adopted is LM358. The voltage output is still defined from 0V to 4.68V with 0.3125V as increment step.
22-Sep-98	The I2C address of the enhanced environment monitor is changed back to be compatible with the LM78 (0101101B) for better S/W compatibility. The definition of TRAP1 pin is also revised.
22-Sep-98	The default value and the Bit 7 of register 40h/bank#0 is revised.
22-Sep-98	The definition of bit 5 of register 41h/bank#0 is redefined for TXD2 signaling.
22-Sep-98	The definition of bit 5 of register 42h/bank#0 is redefined for TXD3 signaling
22-Sep-98	The default value and bit 5 of register 43h/bank#0 is revised.
22-Sep-98	The default value and bit 5 of register 44h/bank#0 is revised.
24-Sep-98	Clarify the definition and action of General Purpose Output 2 register bit 4.
24-Sep-98	The LOAD TEST pin and VIN13 relative bit/function fields are removed. However, the pin for LOADTEST/VIN13 is now defined as an active high AMURSTIN signal for AMU itself. (AMU uses this reset signal which is not shared with all the other circuits in this ASIC. The reason comes that the AMU may be connected to a standby power plane which means in some application, even though the main power fail/loss, the AMU can still work to provide information for outside standby/battery backup controller. If AMU share the same reset (RSTDRV) signal with the other circuit, it may not work when system main power disappears. However, the Automatic Server Restart (ASR) function in the AMU will generate system reset. This system reset must be combined into the original system reset circuitry to reset the system when main power is supplied.
24-Sep-98	The default clock setting is defined as 24Mhz. It is because that either user implement a 14.318M or 48Mhz, there will be no more than 2 times the real clock be input.
24-Sep-98	While FAN control is set for temperature setting mode, the voltage is always either incremented or decremented from current voltage level. No other voltage changing method should be implemented.
24-Sep-98	Another two registers, Power on voltage check mask1/2, to individually control which voltage sources will be checked on power on.
24-Sep-98	The target temperature tolerance is now separated for TXD2 and TXD3 in case there are two different heat-sources (ex. CPU) which has different temperature characteristics. The bit <6:0> of Power on voltage check/4Dh register is revised.
24-Sep-98	Remove the access path of LM75s in AMU. (register bank #1/#2 are now reserved)
24-Sep-98	The default value and bit 5 of BEEPER Mask 1 register/56h is revised.
24-Sep-98	The default value and bit 5 of BEEPER Mask 2 register/57h is revised.
24-Sep-98	Fan control B/5Ah register is revised due to typing error.
24-Sep-98	A new register, fan step control/5Dh, is specified to describe the time step for fan control voltage to be adjusted.
24-Sep-98	Interrupt Statue 3/00h/Bnak#3 register is revised for specification error.
24-Sep-98	SMI# mask 3/02h/Bnak#3 register is revised for specification error.
24-Sep-98	Beeper Status 1/04h/Bank#3 register is revised due to typing error.
24-Sep-98	Beeper Status 2/05h/Bank#3 register is revised due to specification error.
24-Sep-98	Beeper Status 3/06h/Bank#3 register is revised due to specification error.
24-Sep-98	Beeper Mask 3/08h/Bank#3 register is revised due to specification error.
24-Sep-98	Temperature adjust 1/2/3 registers are revised/added due to specification error. The temperature adjust granularity is changed from 1 degree to 2 degree.
24-Sep-98	In Appendix, bit 6 of General Purpose Output 2 register is revised as reserved bit. A new register, General Purpose Output 4 register, is defined to provide a capability to set the VID4~0 pin of this ASIC to LOW state.
24-Sep-98	In Appendix, General Purpose Output 2 register is added.

24-Sep-98 Due to the implementation variation, there is no way to standardize the measured voltage vs. temperature characteristic of CPU thermal diode and 3904 transistor. Both vendor should design and test on their own way. As the temperature can be read out, it represents the CPU die temperature. Be noted, it is not the CPU heat-sink nor P-II heat-spreader temperature.

26-Sep-98 Add Power_on_voltage_check_Mask_1/2 (offset 5Eh/5Fh) registers to control the power on voltage check items. In according to the unmasked voltage check items, the AMU will check each voltage within their target range or not. If the unmasked voltage runs out of the target range, the AMU will activate the BEEPER# output to notify a power on voltage violation has been detected.

1-Oct-98 The relationship of AMURSTOUT, AMURSTIN, and other reset related signals is tried to be specified more clearly as below. The whole AMU will only be reset through the AMURSTIN signal (except the register 5Eh/5Fh of bank#0) which is directly connected from an outside pin (Originally, it is used for LOADTEST signal). There is no internal signal within this ASIC can reset the AMU. However, the AMU can asserted an AMURSTOUT signal (this is an internal signal which will be connected to the circuit in ASUSTeK schematic PAGE 2. That circuit will finally generate a PWROK signal for the chipset to generate CPU reset, PCI reset, and also ISA reset. The AMU may then be reset indirectly (here means not be reset through some internal signal of this ASIC) if the AMURSTIN is connected to one of those reset. The generation of AMURSTOUT should not be affected by the assertion of AMURSTIN signal. In other words, once asserted, AMURSTOUT, it will last as least 30 ms then be deasserted automatically. The Note 4 is also updated.

1-Oct-98 The Power_on_voltage_check_mask registers (5Eh/5Fh) are powered by +5V standby voltage. It means that once being set, it will be recorded and kept by +5V standby voltage. Every time when the system is powered on, AMU will check the voltage automatically in according to the bit pattern in those two registers. Those two register will be reset by RSMRST signal (in ASUSTeK schematic PAGE 2) which used to indicate a AC power loss condition, in other words, the loss of +5V standby voltage.

1-Oct-98 Due to the addition of general_purpose_output_4 register, the VID4~VID0 signals are changed from pure input signals to open-drained I/O signals.

1-Oct-98 The NVRAM enable/disable control (bit_0 of NVRAM control register/5Ch) is defined as: 1, Enable the NVRAM; 0, Disable the NVRAM.

1-Oct-98 The basic time adjust interval for fan_step_control register (5Dh) is changed from 1 second to 2 seconds. In other words, the AMU will adjust (when the fan_control register is configured to be in temperature setting mode) the FANOUT voltage with a maximum interval of 30 seconds.

1-Oct-98 The VIN1 voltage will still be able to be checked through the setting of Power_on_voltage_check_mask voltage. The target voltage of each voltage input is list below:

VIN0- Vcore0_10%,
VIN1- Vcore1_10%,
VIN2- 3.3V_10%,
VIN3- 5V_10%,
VIN4- 12V_20%,
VIN5- -12V_20%,
VIN6- -5V_20%,
VIN7- 5V_10%,
VIN8- 3.3V_20%,
VIN9- 2.5V_10%,
VIN10- 1.5V±10%,
VIN11- 3.3V±20%,
VIN12- 3.3V± 20%.

1-Oct-98 The counter for ASR (offset 21h/bank#3) should count in minute rather than second.

1-Oct-98 For proper system operation, the polarity of THERM# output (can be controlled through the Control register/01h in LM75) must be kept in active LOW configuration.

1-Oct-98 All registers/circuits are powered by VCCAMU except those who are defined explicitly. General_Purpose_Output_1/2/4, General_Purpose_Input_1 registers are powered by VCC/+5V not by VCCAMU. Power_on_voltage_check_mask_1/2 registers are powered by +5V standby voltage.

1-Oct-98 BEEPER Control register, offset 0Ah/Bank#3, is defined to provide alternative identification method. For visual identification, the BEEPER# output will be a square wave with 50% duty cycle and 2 seconds period. If the BEEPER# output is configured as audio identification, bit_7~bit_4 of Beeper_control_register are ignored and the BEEPER# output is compliant to the W83781D to produce the alarm sound. The main purpose of this mechanism is to provide different identification method (visual- LED, audio- BEEPER) after the power on voltage check.

1-Oct-98 The ASR mechanism is revised as stated below: Once enabled, the SMI counter will begin to count down. The system management software must periodically reload the SMI counter in order not to let this counter count down to zero. As the SMI counter counts down to zero, the system SMI# signal is asserted. Depends on the system status, Host CPU may invoke the SMI routine and then take whatever actions/procedures to handle this situation. At the same time when the SMI# signal is asserted, another counter, RESET counter, begins to count down. If the host CPU can execute instruction successfully in the SMI handling routine, it should reload the RESET counter whenever necessary to prevent it from counting down to zero. Once the RESET counter counts down to zero, the AMURSTOUT will then be asserted and the whole system will be reset. The RESET counter won begin to count until the SMI# signal is asserted. The bit 7 and bit 6 of the Intrusion reset register/46h are revised to manipulate this new feature.

1-Oct-98 The embedded 1KB serial NVRAM should implement the SMB bus block transfer capability for performance. Be noted that SMB block transfer is different from the one defined in I2C specification. Please refer to Intel SMB specification.

2-Oct-98 Change RESETIN pin to AMURSTIN for consistency.

2-Oct-98 The LM75 temperature register/offset 00h should be powered by VCCAMU rather than +5V VDD.

2-Oct-98 The ASR SMI and RESET count register will begin to count down as long as their corresponding value are set to be non-zero. It doesn't matter whether the ASR function is enabled or disabled.

2-Oct-98 Add GPO13, 14, RESETFLAG, CLKRST# and JEN status register for internal use.

3-Oct-98 As it can be identified between a block SMB transfer and a non-block SMB transfer from the data transfer point of view, **the NVRAM can only be accessed through a "block transfer" command**. Even though the transfer length can be set to a 1 to perform a single byte transfer, the protocol still be a SMB block transfer. The SMB bus master is required to specify the "transfer data length" to the SMB target. For a block command, it is **embedded** in the command format. 32-byte datum is the maximum transfer length defined in specification. Never the last, the NVRAM is organized to be 4 page by 256 Byte (a total of 1Kbyte). It is possible to have a transfer cross the age" boundary. Here is defined that the auto-addressing sequence are page 11 symbol 224 \f "Wingdings" \s 12遒 page 10 symbol 224 \f "Wingdings" \s 12遒 page 01 symbol 224 \f "Wingdings" \s 12遒 page 00 symbol 224 \f "Wingdings" \s 12遒 page 11 as Intel defined the first transferred data must be with the "highest" address. In other words, for a block transfer with starting address 11 (page) 1111_1110 and data length 00000011 (3-byte), the first data transferred is addressed as 00_0000_0000. The second data transferred is addressed as 11_1111_1111. And, the last data transferred is addressed as 11_1111_1110. Both S/W and H/W engineers must pay attention on this transfer characteristic.

3-Oct-98 To assert SMI# signal for ASR SMI counter counting down to zero, two conditions must be met before the signal can be really asserted. 1) bit_0 of ASR signal control register is set to a "1", and 2) ASR must be enabled through the certification process of writing ASR control register. Also, the internal AMURSTOUT won't be really asserted until 1) bit_1

of ASR signal control register is set to a "1", and 2) ASR has been enabled through the certification process of writing ASR control register.

3-Oct-98 The ASR RESET count register is now defined to count down only when the SMI# due to the ASR SMI counter count down to zero is still asserted. In other words, the bit_7 of Intrusion reset register is a "1". The ASR RESET counter won't count if the bit_7 of Intrusion reset register is a "0". It is defined that when the bit_7 of Intrusion reset register is set (due to ASR SMI count reaches zero) and the SMI# assertion is enabled for ASR SMI count down, the AMU will assert SMI# signal until either the bit_7 of Intrusion reset register is reset to "0" or the ASR SMI# assertion is disabled. The ASR RESET count register will only count down while the bit_7 of Intrusion reset register is set. It is SMI# handler's responsibility to reset the bit_7 of Intrusion reset register to prevent the system from being reset. The ASR RESET count register will "re-load" its original set value when SMI# is deasserted either by reset the bit_7 of Intrusion reset register or disable the assertion of ASR SMI#. However, if AMURSTOUT is asserted, both register will be reset to 0 when the AMURSTIN is asserted.

9-Oct-98 The NVRAM block transfer protocol is clarified and specified here:
The host driving cycle is described by ***underlined-bold-italian*** stype character. The device/slave driving cycle is described by normal character.
For a block write to NVRAM, the transfer protocol is:
<S> Slave address/Wr <A>***Index***<A>***Byte_count***<A>***DATA0/Index***<A>
DATA1/Index+1<A>***DATA2/Index+2***<A>***DATA3/Index+3***<A>__..
DATAN/Index+byte_count-1<A>***<P>***
For a block read from NVRAM, the transfer protocol is:
<S> Slave address/Wr <A>***Index***<A>***<S> Slave address/Wr*** <A>_
Byte_count***<A>*** DATA0/Index***<A>***DATA1/Index+1***<A>***
DATA2/Index+2***<A>***DATA3/Index+3***<A>***_____…
DATAN/Index+byte_count-1***<A><P>***
The data transfer sequence is defined from index, index+1, index+2,_.in an incremental style.
<S> represents START, <A> represents ACKNOWLEDGE, and <P> depicts STOP.
Please be noted the transfer of byte_count value is different from a write to a read. For a block write, the host drives out the byte_count. However, for a block read, the device/slave will drive out the byte_count.
In order to enable the variable length of block transfer, for a block read, a new register is defined as "block read length" register/0Bh/Bank#3 which contains the information that device/slave can drive out in the byte_count phase during a block read transfer. Also, it will guide the device/slave how many bytes will be read.

9-Oct-98 By writing a "1" to this bit, all the AMU will be reset back to its default state (include the registers and internal state machines) except the registers:
bit<7>, bit<6> of Intrusion reset register/46h/Bank#0.
Bank#0, registers 5Eh/5Fh.
General Purpose Input _ registers, and
General Purpose Output 1/2/3/4 registers.

20-Oct-98 Add GPO15 for ASIC page 1.

20-Oct-98 Add security circuit I/F registers(include I2C address setting register 86h).

26-Oct-98 Change VID0~VID4 pins I/O cell from I/OD to I/O, make these pins can drive high when they are set as output pins. And Reg. 85h bit5 is the control bit of these pins, default is 0 means they are input pins. Reg 85h is powered by 5VSB and reset by 5VSB power-on reset.

29-Oct-98 Add GPO16 for ASIC page 3. This GPO16 is controlled by Reg 83h bit 1 which is powered by 3V battery.

30-Oct-98 Modify BRSTDRV#(pin 21), BRSTDRV(pin 22), and PCIRST#(pin 23) drive/sink current from 8mA to 16mA .

2-Nov-98 ***Move RESETFLAG from Reg 81h bit 5 to Reg 83h bit 2, and this bit can be reset by battery power-on reset only.***

2-Nov-98 ***GPO14, Reg 83h bit 0, this bit can be cleared by GRSMRST# and battery power-on reset.***

2-Nov-98 ***Remove SLOTOCC#(pin 61) and INTRUSION(pin 64) debounce ckt.(external RC ckt. needed).***

8-Feb-99

1.Remove the Resetflag function in ASIC circuit page2. Refer to the final ASIC circuit.

2.The delay time of the CLKRST# assertion after 81H bit 4 being programmed is changed to 300ms.

3.Add IN_NEWCPU# as reset source for VID0~VID4 and their I/O control bit(85H). Reset to their default value.

4.GPIO Byte 80H, 81H, 87H can be reset by PWROK to their default values.

5.CF1~CF4, 100/66#, FS0~FS3 can be read back. The values returned are the register values. And the following address are used:

For winbond: BANK#3 80H<bit0~bit3>=CF1~CF4; <bit4~bit7>=Reserved.
BANK#3 81H<bit0~bit4>=100/66#, FS0~FS3; <bit5~bit7>=Reserved.

For Holtek: BANK#2 88H<bit0~bit3>=CF1~CF4; <bit4~bit7>=Reserved.
BANK#2 89H<bit0~bit4>=FS0~FS3, 100/66#; <bit5~bit7>=Reserved.

NOTE: BANK#2 refers to secondary LM75.

6.100/66#, FS0~FS3 internal pull-up resistors change to 1K Ohm.

7.Pin36 and Pin37 change function. Pin36 OR with GPO4(default high) to generate the output Pin37. The OR gate is powered by +5V. Refer to fianl ASIC circuit for detail.

8.Chip ID(BANK#0 58h) changes to 31H(00110001).

9.FAN1IN, FAN2IN, FAN3IN 10K Ohm internal pull-up to +5V.

10.SLOTOCC# 2M Ohm(or higher)internal pull-up to BATT.

11.INTRUSION 2M Ohm(or higher) internal pull-up to BATT.

12. The security circuit should be modified. The system failure or pass is decided by software(BIOS) not by hardware.

1. Function description

The ASUSTeK Management Unit is the third generation of system environment monitor/control component. There are 4 I2C devices in this unit: 1) one I2C LM75-register-compatible thermal sensor, 2) one enhanced LM78/W83781D environment monitor, 3) one 1KB I2C NVRAM, 4) one LM75-register compatible thermal sensor with ASUSTeK ASIC register extension. The LM75 thermal sensors are designed to have default I2C address of 1001001b (primary LM75, for power supply or 2nd CPU temperature) and 1001000b (secondary LM75, default to measure CPU temperature). The one with ASUSTeK ASIC register extension has default I2C address of 1001000b. However, the I2C addresses can be modified through register in environment monitor. The enhanced environment monitor is designed to have default I2C address of 0101101b. One trap pins are provided to enable the change of default environment monitor I2C address. The I2C NVRAM has a default I2C address of 11100PPb (where P represents Page number in the NVRAM, each pages includes 256Byte data area which can be addressed by the following 8-bit I2C datum after the I2C address phase) while the address can be modified through register in environment monitor.

The LM75-compatible thermal sensor utilizes external component (3904 transistor, thermister, Intel thermal diode) to obtain the temperature measurement. As all these three thermal devices have their own electrical characteristic, identification can be provided through a H/W trapping (thermister or transistor/diode) and also bit-field in register (transistor or Intel diode). Except the original Temperature, Configuration, Tos set point, and Thyst set point registers in the Lm75, several other registers are designed in the enhanced environment monitor sub-unit to adapt the selection of different thermal sense device. After an over-temperature condition is detected, THERM# pin can be configured to be asserted to alarm the system. Also, SMI# can also be configured to be asserted after over-temperature is detected. As the whole ASIC can detect upto three temperatures, the following thermal sense device arrangement is required to enable the best cost/performance selection: 1) temperature sensor #1 (TXD1) is used to measure the environment/ambient temperature. Either 3904-type transistor or thermister can be used as temperature sensing component. 2) temperature sensor #2 (TXD2) is used to measure the CPU heatsink temperature. Thermister or Intel thermal diode can be used as the sensing device. 3) temperature sensor #3 (TXD3) is used to measure either power supply or CPU heatsink (Dual-processor system) temperature. Thermister or Intel thermal diode can be used as the sensing device.

The enhanced environment monitor subunit monitor the environment variables, such as: up to three fans can be monitored for their speed, various voltage sources of +12V, -12V, +5V, -5V, +3.3V, Vcore1, Vcore2, +2.5V, +1.5V, +5VSB, +3VSB, CMOS battery, NVRAM battery are monitored, one input is designed to reflect the chassis security state (chassis intrusion), the 5-bit VID can be accessed through register to identify the correct Vcore voltage level. The BEEP# or SMI# outputs are designed to be configured to be asserted on any specified abnormal situation detected. 2 fan speed control pins are also designed to enable the fan speed control based on the output voltage (0V depicts fan stop to 4.68V depicts 100% fan speed) of those pins. As there are three fans, it is required that one fan speed control pin is used to control the speed of CPU fan (FANOUTA), the other fan speed control pin is used to control the other two fans- chassis and power supply fans (FANOUTB). Another useful function, Automatic Server Restart (ASR), is included in this monitor sub-unit. Once ASR is enabled, if system can't update the ASR count register within a specified period of time (due to a software hang, system crash, or system trap), the AMURSTOUT output will be asserted for 30ms to reset the whole system (it will be combined into the system reset logic).

A 1KB battery back-up I2C NVRAM is designed to provide non-volatile system log feature. This NVRAM can be enabled or disabled through register in the environment sub-unit. Different from general I2C device addressing, the two address bits (A1/A0) during device selection phase represent the highest 2 address bits for the NVRAM. In combining the following 8-bit pointer, a

10-bit NVRAM addresses are formed to enable the access of 1KB NVRAM. The upper five I2C address bits can be programmed through register in environment monitor sub-unit.

2. Pin description

The whole row is covered with gray color indicates that the pin is shared with the other logic blocks in this ASIC.

Only the first column is covered with gray color depicts the signal is internal used in the ASIC. No external pin/pad is required for it.

#	Pin name	type	Description	Remark
	AMURSTOUT	O VCCAMU	Automatic Server Restart reset output	This signal must be connected to the ASIC internal reset/ power good circuit to reset the system. Watch out the possible current leakage problem
	SMBCLK	I/OD VCCAMU TTL	I2C bus clock	
	SMBDATA	I/OD VCCAMU TTL	I2C bus data	
	INTRUSION	I BATT/ VCCAMU TTL	Chassis intrusion detection HIGH, intruded; LOW, no intrusion.	The INTRUSION signal is powered by BATTERY such that AMU INTRUDE pin must be designed to prevent leakage.
	VREF	O VCCAMU	Reference Voltage output (4.096V)	
	TXD1	Analog I xxV~yyV	Thermal sensor input 1. Two thermal detection mechanisms should be supported: 1) 3904 transistor/diode, 2) thermister. (ambient temperature)	In register, information must be provided to enable the manage-ment software to identify which kind of mechanism is adopted. While there is no thermal sense device applied the temperature read out should be FFh.
	TXD2	Analog I xxV~yyV	Thermal sensor input 2. Two thermal detection mechanisms should be supported: 1) Intel deschute thermal diode/3904 transistor, 2) thermister. (CPU temperature) The temperature can be readout from primary LM75.	In register, information must be provided to enable the manage-ment software to identify which kind of mechanism is adopted. While there is no thermal sense device applied the temperature read out should be FFh.
#	Pin name	type	Description	Remark

	TXD3	Analog I xxV~yyV	Thermal sensor input 3. Two thermal detection mechanisms should be supported: 1) Intel deschute thermal diode/3904 transistor, 2) thermister. (PWR/CPU temperature) The temperature can be readout from secondary LM75.	In register, information must be provided to enable the manage-ment software to identify which kind of mechanism is adopted. While there is no thermal sense device applied the temperature read out should be FFh.
	AGND	Analog	Analog ground	
	VID4	I/OD	Pentium II Voltage ID output	External pull-up to +5V
	VID3	I/OD	Pentium II Voltage ID output	External pull-up to +5V
	VID2	I/OD	Pentium II Voltage ID output	External pull-up to +5V
	VID1	I/OD	Pentium II Voltage ID output	External pull-up to +5V
	VID0	I/OD	Pentium II Voltage ID output	External pull-up to +5V
	BEEP#	OD 48mA VCCAMU	Beeper output	
	SMI#	OD VCCAMU	System Management Interrupt output to alert on event	
	THERM#	OD VCCAMU	Over-temperature output. It is configurable that TXD1/2/3 will assert this signal on detecting over-temperature respectively.	
	VCCAMU	Analog Power	VDD for AMU.	As AMU may be powered by +5VSB, care must be taken to prevent leakage.
	BATT	Analog Power	VDD to power chassis intrusion memory (74HCT14+74HC74) circuit. It will also be monitored as an voltage source.	Low power consumption is required. This pin is shared through ASUSTeK ASIC. Be care of leakage.
	+5VSB	Analog I	+5VSB voltage monitor input	Be care about leakage
	+3VSB	Analog I	+3VSB voltage monitor input	Be care about leakage
	VCORE2	Analog I	Vcore2 voltage monitor input	Be care of leakage
	+2.5V	Analog I	+2.5V voltage monitor input	Be care of leakage
#	Pin name	type	Description	Remark
	NVRAMVCC	Analog Power	Extra Battery input to power on-chip I2C NVRAM for event	The design of NVRAM should be proposed and discussed.

			logging. It is also be monitored as a voltage source.	
	VCORE1	Analog I	Vcore1 voltage monitor input for CPU core voltage.	Be care of leakage
	+3V	Analog I	+3V voltage monitor input	Be care of leakage
	+5V	Analog I	+5V voltage monitor input	Be care of leakage
	+12V	Analog I	+12V voltage monitor input	Be care of leakage
	-12V	Analog I	-12V voltage monitor input	Be care of leakage
	-5V	Analog I	-5V voltage monitor input	Be care of leakage
	+1.5V	Analog I	+1.5V voltage monitor input	Be care of leakage
	AMURSTIN	I TTL	Reset signal to reset AMU	Must come directly from an external pin and must not be interfered by any other reset related circuitry in this ASIC.
	DGND	Analog	Digital ground	
	GPO1	O	General Purpose Output 1 for internal use	Refer to ASIC spec.
	GPO2	O	General Purpose Output 2 for internal use	Refer to ASIC spec.
	GPO3	O	General Purpose Output 3 for internal use	Refer to ASIC spec.
	GPO4	O	General Purpose Output 4 for internal use	Refer to ASIC spec.
	GPO5	O	General Purpose Output 5 for internal use	Refer to ASIC spec.
	GPO6	O	General Purpose Output 6 for internal use	Refer to ASIC spec.
	GPO7	O	General Purpose Output 7 for internal use	Refer to ASIC spec.

#	Pin name	type	Description	Remark
	GPO8	O	General Purpose Output 8 for internal use	Refer to ASIC spec.
	GPO9	O	General Purpose Output 9 for internal use	Refer to ASIC spec.
	GPO10	O	General Purpose Output 10 for internal use	Refer to ASIC spec.
	GPO11	O	General Purpose Output 11 for internal use	Refer to ASIC spec.
	GPO12	O	General Purpose Output 12 for internal use	Refer to ASIC spec.
	GPO13	O	General Purpose Output 13 for internal use	Refer to ASIC spec.
	GPO14	O	General Purpose Output 14 for internal use	Refer to ASIC spec.
	GPO15	O	General Purpose Output 14 for internal use	Refer to ASIC spec.
	GPO16	O	General Purpose Output 14 for internal use	Refer to ASIC spec.
	GPI1	I	General Purpose Input 1 for internal use	Refer to ASIC spec.
	GPI2	I	General Purpose Input 2 for internal use	Refer to ASIC spec.
	CLKRST#	O	For internal use	Refer Register Definition for details.
	JEN	I	JEN status for internal use. Take care of the leakage current problem.	Refer to ASIC spec.
	FAN1IN	I TTL	Fan tachometer input	With internal diode/pull-up, any kind of fan can be used. As AMU may be powered by +5VSB, care should be taken for leakage. Due to the design, the real input LOW threshold voltage should be high enough (>1.2V) to enhance fan compatibility.

#	Pin name	type	Description	Remark
	FAN2IN	I TTL	Fan tachometer input	With internal diode/pull-up, any kind of fan can be used. As AMU may be powered by +5VSB, care should be taken for leakage. Due to the design, the real input LOW threshold voltage should be high enough (>1.2V) to enhance fan compatibility.
	FAN3IN	I TTL	Fan tachometer input	With internal diode/pull-up, any kind of fan can be used. As AMU may be powered by +5VSB, care should be taken for leakage. Due to the design, the real input LOW threshold voltage should be high enough (>1.2V) to enhance fan compatibility.
	FANAOUT	Analog O (0~4.68V)	Fan speed control output. This pin is designed to control the speed of CPU fan.	Output voltage range from 0V to 4.68V. 16 different voltage levels should be provided including 0V and 4.68V.
	FANBOUT	Analog O (0~4.68V)	Fan speed control output. This pin is designed to control the speed of chassis and other fans.	Output voltage range from 0V to 4.68V. 16 different voltage levels should be provided including 0V and 4.68V.
	CLK	I TTL	System clock input	24Mhz is by default. 14,31818 Mhz and 48Mhz is also accepted but needs software configuration.

Trapping option:

Original pin	Trap pin	Description	Remark
TRAP1	I2C A0 trap	I2C address 1 trap pin for enhanced environment monitor. Connect to ground indicates a “0”.	Internal weak pull-up resistor (10K) set the default value to 1”

Original pin	Trap pin	Description	Remark
TRAP2	TXD1 trap	Thermal sense device connected to TXD1. Pull high (10K) indicates 3904/diode is applied as sensing device. Internal pull down selects default sensing device as thermister.	Internal weak pull-down resistor (100K) set the default value to 0" (thermister)
TRAP3	TXD2 trap	Thermal sense device connected to TXD2. Pull high (10K) indicates a transistor or diode is applied.	Internal weak pull-down resistor (100K) set the default value to 0" (thermister)
TRAP4	TXD3 trap	Thermal sense device connected to TXD3. Pull high (10K) indicates a transistor or diode is applied.	Internal weak pull-down resistor (100K) set the default value to 0" (thermister)

*** Can use FREE# because of its O.C. like design. ***

3. Register description

Register	Offset	Power on/Reset default value	Description
Configuration (LM78 compliant)	40h	00000001b	Configuration register <7>/RW= 1, reset the whole environment monitor sub-unit. <6:4>= Reserved <3>/RW= 1, Disable the SMI# output without affecting the contents of interrupt status registers. The AMU will stop monitoring. It will resume on clearing of this bit. <2>= Reserved <1>/RW= 1, Enable the SMI# output 0, Disable the SMI# output <0>/RW= 1, Enable the monitoring operation 0, Disable the monitoring operation
Interrupt Status 1 (refer to NOTE 1) (LM78 compliant)	41h	00000000b	Interrupt status 1 register <7>/RO= 1, indicates a High or Low limit on FAN2 has been exceeded. <6>/RO= 1, indicates a High or Low limit on FAN1 has been exceeded. <5>/RO= 1, indicates a High or Low limit on TXD2 temperature has been exceeded. <4>/RO= 1, indicates a High or Low limit on TXD1 temperature has been exceeded. <3>/RO= 1, indicates a High or Low limit on VIN3 has been exceeded. (+5V) <2>/RO= 1, indicates a High or Low limit on VIN2 has been exceeded. (+3V) <1>/RO= 1, indicates a High or Low limit on VIN1 has been exceeded. (Vcore2 or +1.5V or ..) <0>/RO= 1, indicates a High or Low limit on VIN0 has been exceeded. (Vcore1)

Register	Offset	Power on/Reset default value	Description
Interrupt Status 2 (LM78 compliant)	42h	00000000b	Interrupt status 2 register <7:6>= Reserved. <5>/RO= 1, indicates a High or Low limit on TXD3 temperature has been exceeded. <4>/RO= 1, indicates chassis intrusion has been detected. <3>/RO= 1, indicates a High or Low limit on FAN3 pin has been exceeded. <2>/RO= 1, indicates a High or Low limit on -VIN6 has been exceeded. (-5V) <1>/RO= 1, indicates a High or Low limit on -VIN5 has been exceeded. (-12V) <0>/RO= 1, indicates a High or Low limit on VIN4 has been exceeded. (+12V)
SMI# Mask 1 (LM78 compliant)	43h	00000000b	SMI# mask 1 register <7>/RW= 1, disable the FAN2 interrupt status bit to generate SMI# interrupt. <6>/RW= 1, disable the FAN1 interrupt status bit to generate SMI# interrupt. <5>/RW= 1, disable the TXD2 interrupt status bit to generate SMI# interrupt. <4>/RW= 1, disable the TXD1 interrupt status bit to generate SMI# interrupt. <3>/RW= 1, disable the VIN3 interrupt status bit to generate SMI# interrupt. <2>/RW= 1, disable the VIN2 interrupt status bit to generate SMI# interrupt. <1>/RW= 1, disable the VIN1 interrupt status bit to generate SMI# interrupt. <0>/RW= 1, disable the VIN0 interrupt status bit to generate SMI# interrupt.
SMI# Mask 2 (LM78 compliant)	44h	00000000b	SMI# mask 2 register <7:6>= Reserved <5>/RW= 1, disable the TXD3 interrupt status bit to generate SMI# interrupt. <4>/RW= 1, disable the chassis intrusion interrupt status bit to generate SMI# interrupt. <3>/RW= 1, disable the FAN3 interrupt status bit to generate SMI# interrupt. <2>/RW= 1, disable the –VIN6 interrupt status bit to generate SMI# interrupt. <1>/RW= 1, disable the –VIN5 interrupt status bit to generate SMI# interrupt. <0>/RW= 1, disable the VIN4 interrupt status bit to generate SMI# interrupt.

Register	Offset	Power on/Reset default value	Description
Intrusion reset	46h	00000000	Intrusion reset register <7>/RW= 1, a 20ms LOW pulse will be generated on the internal INTRUDE signal to clear the chassis intrusion Flip-Flop. This bit self clears after the pulse has been output. <6>/RW= 1, indicates an ASR SMI counter timeout occur. The ASR RESET count register begins to count down. This bit won be cleared through reset. Only power on or a software write can change its value. 0, No ASR SMI counter timeout occurs_ <5>/RW= 1, indicates an ASR RESET counter timeout occurs during last reboot. This bit won be cleared through reset. Only power on or a software write can change its value. 0, No ASR RESET counter timeout occurs since last reboot P.S.: Whenever the counter counts down to zero, the corresponding timeout flag will always be set to a "1" no matter whether the corresponding signal is enabled to be asserted or not. By writing a "0" to the bit 7 will deassert the SMI# signal if it is asserted. If the SMI# signal is not asserted (due to ASR SMI# output is disabled), the SMI# signal will be left as deasserted. <4:0>= Reserved
VID/Fan divisor (LM78 compliant)	47h	<7:4>=0101, <3:0>=VID3~0	VID/Fan divisor register <7:6>/RW= Fan 2 tachometer divisor. <5:4>/RW= Fan 1 tachometer divisor. 00 divide by 1 01 divide by 2 10 divide by 4 11 divide by 8 <3:0>/RO= The logic value of VID3~VID0 pins
Chip version and Voltage ID (W83781D compliant)	49h	<7:1>=0010000 <0>=VID4	Chip version and Voltage ID register <7:1>/RO= version number (1.0 initially) <0>/RO= The logic value of VID4 pin
LM75 serial address (W83781D compliant)	4Ah	00000001	LM75 serial address register <7>/RW= 1, Disable secondary LM75 thermal sensor; 0, Enable secondary LM75 thermal sensor. <6:4>/RW= I2C address of secondary Lm75 sensor. <3>/RW= 1, Disable primary LM75 thermal sensor; 0, Enable primary LM75 thermal sensor. <2:0>/RW= I2C address of primary Lm75 sensor.
Register	Offset	Power on/Reset default value	Description
Pin Control (W83781D compliant)	4Bh	01000100	Pin control register <7:6>/RW= Fan 3 tachometer divisor.

			00 divide by 1 01 divide by 2 10 divide by 4 11 divide by 8 <5:4>/RW = ADC clock input 00 No division 01 divided by 4 10 divided by 16 11 divided by 48 PS: Holtek won't implement this bit-field. <3:2>/RW = Clock input select 00 input clock is 14.31818Mhz 01 input clock is 24Mhz 10 input clock is 48Mhz 11 reserved <1:0>= Reserved
Power on voltage check	4Dh	00000000	Power on voltage check register <7>/RW= 1, Disable the power on voltage check with beeper alarm feature. 0, Enable the power on voltage check with beeper alarm feature. Note: Which voltages will be checked after power on can be controlled by the power_on_voltage_check_mask register with offset 5Eh/5Fh/Bank#0. Those registers should be kept by standby power plane such that once set, it can remember which voltages need to be checked after power on in the future. <6:4>/RW= target temperature tolerance for TXD3 (1 C precision) <3>= Reserved. <2:0>/RW= target temperature tolerance for TXD2 (1 C precision) Note: Once the power on voltage check finds some abnormal voltage, the beeper will start to beep after 5 second later for S/W a chance to disabled it without extra beep sound.
Bank select (W83781D compliant)	4Eh	10000000	Register Bank select register <7>/RW= 1, access register 4Fh high byte register 0, access register 4Fh low byte register <6:3>= Reserved <2:0>/RW= 000, select register bank 0 001~010 Reserved 011, select register bank 3 100~111 Reserved

Register	Offset	Power on/Reset default value	Description
Vendor ID (W83781D compliant)	4Fh	<15:0>=Vendor ID	Vendor ID register <7:0>/RO= High byte Vendor ID if bit_7 of Bank select register is "1" Low byte Vendor ID if bit_7 of Bank select register is "0"
Vendor reserved register	50~55h Bank#0	N.A.	Those registers are reserved for vendor to implement their own test registers which will only be used during manufacture stage. For normal operation, there should be N.A. to system H/W or S/W design.
BEEPER Mask 1 (W83781D compliant)	56h Bank#0	11111111b	BEEPER control 1 register <7>/RW= 1, disable the FAN2 beeper status bit to generate beeper output. <6>/RW= 1, disable the FAN1 beeper status bit to generate beeper output. <5>/RW= 1, disable the TXD2 beeper status bit to generate beeper output. <4>/RW= 1, disable the TXD1 beeper status bit to generate beeper output. <3>/RW= 1, disable the VIN3 beeper status bit to generate beeper output. <2>/RW= 1, disable the VIN2 beeper status bit to generate beeper output. <1>/RW= 1, disable the VIN1 beeper status bit to generate beeper output. <0>/RW= 1, disable the VIN0 beeper status bit to generate beeper output.
BEEPER Mask 2 (W83781D compliant)	57h Bank#0	11111111b	BEEPER control 2 register <7>/RW= 1, Enable the global beeper output. <6>= Reserved <5>/RW= 1, disable the TXD3 beeper status bit to generate beeper output. <4>/RW= 1, disable the Chassis intrusion beeper status bit to generate beeper output. <3>/RW,= 1, disable the FAN3 beeper status bit to generate beeper output. <2>/RW= 1, disable the –VIN6 beeper status bit to generate beeper output. <1>/RW= 1, disable the –VIN5 beeper status bit to generate beeper output. <0>/RW= 1, disable the VIN4 beeper status bit to generate beeper output.
Chip ID (W83781D compliant)	58h Bank#0	00110001	Chip ID register <7:4>/RO= Chip major ID number <3:0>/RO= Chip minor ID number

Register	Offset	Power on/Reset Default value	Description
Fan control A	59h Bank#0	10001111b	Fan control A register <7>/RW= 1, speed setting mode <6:4>= Reserved <3:0>/RW= speed grading 0000 Fan stop (FANAOUT = 0V) 0001 (FANAOUT=0.3125V) 0010 (FANAOUT=0.625V) 0011 (FANAOUT=0.9375V) 0100 (FANAOUT=1.25V) 0101 (FANAOUT=1.5625V) 0110 (FANAOUT=1.875V) 0111 (FANAOUT=2.1875V) 1000 (FANAOUT=2.5V) 1001 (FANAOUT=2.8125V) 1010 (FANAOUT=3.125V) 1011 (FANAOUT=3.4375V) 1100 (FANAOUT=3.75V) 1101 (FANAOUT=4.0625V) 1110 (FANAOUT=4.375V) 1111 (FANAOUT=4.68V) NOTE: When the speed grading is set to 0000 (stop the fan), the FANAOUT voltage won change until 60 seconds later. In orther words, the fan will keep running for 60 seconds after the speed grading is set to 0. --- <7>/RW= 0, temperature setting mode <6:0>/RW= Target temperature (1蚓 precision). AMU will automatically adjust the speed of fan to keep the sensing temperature within target temperature. TXD2 signal is used here as temperature sensing source. The value will be compared with primary LM75 temperature register bit_14:bit_8 to determine whether the measured temperature has matched the target temperature. NOTE: In order to avoid the fan speed threshing, a tolerance of plus/minus bit_2:bit_0 of Power_on_voltage_check register should be considered in designing this close-loop control mechanism. In other words, the fan can be kept in any speed when the detected temperature is within (target temperature - tolerance, target temperature + tolerance). In temperature setting mode, if the target temperature can ***not*** be achieved when fan speed has reached 100% for 3 minutes, bit_7 of interrupt status 3 register will be set. Also, if the target temperature is set too high, there may be no fan required. The fan will stop. Again, it is 60 seconds that the fan will really

			stop after the a fan stop command has been issued. Under this mode, the time interval of the voltage step incremented/ decremented is controlled by the fan_step_control register in offset 5Dh/Bank#3. NOTE: BIOS should turn off the FAN control interrupt when using temperature setting mode.

Register	Offset	Power on/Reset Default value	Description
Fan control B	5Ah Bank#0	10001111b	Fan control B register <7>/RW= 1, speed setting mode <6:4>= Reserved <3:0>/RW= speed grading 0000 Fan stop (FANBOUT = 0V) 0001 (FANBOUT=0.3125V) 0010 (FANBOUT=0.625V) 0011 (FANBOUT=0.9375V) 0100 (FANBOUT=1.25V) 0101 (FANBOUT=1.5625V) 0110 (FANBOUT=1.875V) 0111 (FANBOUT=2.1875V) 1000 (FANBOUT=2.5V) 1001 (FANBOUT=2.8125V) 1010 (FANBOUT=3.125V) 1011 (FANBOUT=3.4375V) 1100 (FANBOUT=3.75V) 1101 (FANBOUT=4.0625V) 1110 (FANBOUT=4.375V) 1111 (FANAOUT=4.68V) NOTE: When the speed grading is set to 0000 (stop the fan), the FANAOUT voltage won change until 60 seconds later. In orther words, the fan will keep running for 60 seconds after the speed grading is set to 0. _____ <7>/RW= 0, temperature setting mode <6:0>/RW= Target temperature (1蚓 precision). AMU will automatically adjust the speed of fan to keep the sensing temperature within target temperature. TXD3 signal is used here as temperature sensing source. The value will be compared with secondary LM75 temperature register bit_14:bit_8 to determine whether the measured temperature has matched the target temperature. NOTE: In order to avoid the fan speed threshing, a tolerance of plus/minus bit_6:bit_4 of Power_on_voltage_check register should be considered in designing this close-loop control mechanism. In other words, the fan can be kept in any speed when the detected temperature is within (target temperature - tolerance, target temperature + tolerance). In temperature setting mode, if the target temperature can ***not*** be achieved when fan

			speed has reached 100% for 3 minutes, bit_6 of interrupt status 3 register will be set. Also, if the target temperature is set too high, there may be no fan required. The fan will stop. Again, it is 60 seconds that the fan will really stop after the a fan stop command has been issued. Under this mode, the time interval of the voltage step incremented/ decremented is controlled by the fan_step_control register in offset 5Dh/Bank#3. NOTE: BIOS should turn off the FAN control interrupt when using temperature setting mode.
Thermal Sensor type	5Bh Bank#0	00x0y0z0 (x/y/z reflect the corresponding traping status: 1/ pull-high, 0/pull-down)	Thermal sensor type register <7:6>= Reserved. <5:4>/RW= type of TXD3 0x Thermister/10K,B=3435 10 3904 transistor 11 Intel thermal diode <3:2>/RW= type of TXD2 0x Thermister/10K,B=3435 10 3904 transistor 11 Intel thermal diode <1:0>/RW= type of TXD1 0x Thermister/10K,B=3435 10 3904 transistor 11 Intel thermal diode
NVRAM control	5Ch Bank#0	11100000	<7:3>/RW = NVRAM I2C address <2:1>=Reserved <0>/RW= NVRAM enable/disable control register. 1 represents enabled; 0, represents disabled.
Fan step control	5Dh Bank#0	01001000	Fan step control register <7:4>/RW= The time interval, two seconds as a unit, when FANxOUT voltage is incremented to increase the fan speed and reduce the temperature (Only when fan control is under temperature setting mode) <3:0>/RW= The time interval, two seconds as a unit, when FANxOUT voltage is decremented to decrease the fan speed (Only when fan control is under temperature setting mode)

Register	Offset	Power on/Reset Default value	Description
Power on Voltage check mask 1	5Eh Bank#0	11100010	Power on Voltage check mask 1 register <7>/RW= 1, VIN7 won't be check on power on. 0, VIN7 will be checked on power on. <6>/RW= 1, -VIN6 won't be check on power on. 0, -VIN6 will be checked on power on. <5>/RW= 1, -VIN5 won't be check on power on. 0, -VIN5 will be checked on power on. <4>/RW= 1, VIN4 won't be check on power on. 0, VIN4 will be checked on power on. <3>/RW= 1, VIN3 won't be check on power on. 0, VIN3 will be checked on power on. <2>/RW= 1, VIN2 won't be check on power on. 0, VIN2 will be checked on power on. <1>/RW= 1, VIN1 won't be check on power on. 0, VIN1 will be checked on power on. <0>/RW= 1, VIN0 won't be check on power on. 0, VIN0 will be checked on power on. PS. This register is powered by +5V standby voltage and won't be affected through system reset. It can only be reset by the RSMRST signal.
Power on Voltage check mask 2	5Fh Bank#0	00011111	Power on Voltage check mask 2 register <7:5>= Reserved <4>/RW= 1, VIN12 won't be check on power on. 0, VIN12 will be checked on power on. <3>/RW= 1, VIN11 won't be check on power on. 0, VIN11 will be checked on power on. <2>/RW= 1, VIN10 won't be check on power on. 0, VIN10 will be checked on power on. <1>/RW= 1, VIN9 won't be check on power on. 0, VIN9 will be checked on power on. <0>/RW= 1, VIN8 won't be check on power on. 0, VIN8 will be checked on power on. PS. This register is powered by +5V standby voltage and won't be affected through system reset. It can only be reset by the RSMRST signal.
Interrupt Status 3	00h Bank#3	00000000	Interrupt Status 3 register (read to clear) <7>/RO= 1, indicates TXD2 temperature sense can match the target temperature value in FAN control A register. <6>/RO= 1, indicates TXD1 temperature sense can match the target temperature value in the FAN control B register. <5>=Reserved <4>/ RO = 1, indicates a High or Low limit on VIN11 has been exceeded. <3>/ RO = 1, indicates a High or Low limit on VIN10 has been exceeded. <2>/ RO = 1, indicates a High or Low limit on VIN9 has been exceeded. <1>/ RO = 1, indicates a High or Low limit on VIN8 has been exceeded.

			<0>/ RO = 1, indicates a High or Low limit on VIN7 has been exceeded.
Register	Offset	Power on/Reset Default value	Description
Interrupt Status 4	01h Bank#3	00000000	Interrupt Status 4 register (read to clear) <7:1>=Reserved <0>/ RO = 1, indicates a High or Low limit on VIN12 has been exceeded.
SMI# Mask 3	02h Bank#3	11111111	SMI# mask3 register <7>/RW= 1, disable the TXD2 temperature sense can match the target temperature value in the FAN control A register to generate a SMI# <6>/RW= 1, disable the TXD1 temperature sense can match the target temperature value in the FAN control B register to generate a SMI#. <5>=Reserved <4>/RW= 1, disable the VIN11 interrupt status bit to generate SMI# interrupt <3>/RW= 1, disable the VIN10 interrupt status bit to generate SMI# interrupt <2>/RW= 1, disable the VIN9 interrupt status bit to generate SMI# interrupt <1>/RW= 1, disable the VIN8 interrupt status bit to generate SMI# interrupt <0>/RW= 1, disable the VIN7 interrupt status bit to generate SMI# interrupt
SMI# Mask 4	03h Bank#3	11111111	SMI# mask4 register <7:1>=Reserved <0>/RW= 1, disable the VIN12 interrupt status bit to generate SMI# interrupt
Beeper Status 1 (A read to this register will clear/reset all bit-field back to 0)	04h Bank#3	00000000	Beeper status 1 register (read to clear) <7>/RO= 1, indicates a High or Low limit on FAN2 has been exceeded. <6>/RO= 1, indicates a High or Low limit on FAN1 has been exceeded. <5>/RO= 1, indicates a High or Low limit on TXD2 temperature has been exceeded. <4>/RO= 1, indicates a High or Low limit on TXD1 temperature has been exceeded. <3>/RO= 1, indicates a High or Low limit on VIN3 has been exceeded. (+5V) <2>/RO= 1, indicates a High or Low limit on VIN2 has been exceeded. (+3V) <1>/RO= 1, indicates a High or Low limit on VIN1 has been exceeded. (Vcore2 or +1.5V or ..) <0>/RO= 1, indicates a High or Low limit on VIN0 has been exceeded. (Vcore1)

Register	Offset	Power on/Reset Default value	Description
Beeper Status 2 (A read to this register will clear/reset all bit-field back to 0)	05h Bank#3	00000000	Beeper status 2 register <7:6>= Reserved. <5>/RO= 1, indicates a High or Low limit on TXD3 temperature has been exceeded. <4>/RO= 1, indicates chassis intrusion has been detected. <3>/RO= 1, indicates a High or Low limit on FAN3 pin has been exceeded. <2>/RO= 1, indicates a High or Low limit on -VIN6 has been exceeded. (-5V) <1>/RO= 1, indicates a High or Low limit on -VIN5 has been exceeded. (-12V) <0>/RO= 1, indicates a High or Low limit on VIN4 has been exceeded. (+12V)
Beeper Status 3	06h Bank#3	00000000	Beeper Status 3 register (read to clear) <7>/RO= 1, indicates TXD2 temperature sense can match the target temperature value in FAN control A register. <6>/RO= 1, indicates TXD3 temperature sense can match the target temperature value in the FAN control B register. <5>=Reserved <4>/ RO = 1, indicates a High or Low limit on VIN11 has been exceeded. <3>/ RO = 1, indicates a High or Low limit on VIN10 has been exceeded. <2>/ RO = 1, indicates a High or Low limit on VIN9 has been exceeded. <1>/ RO = 1, indicates a High or Low limit on VIN8 has been exceeded. <0>/ RO = 1, indicates a High or Low limit on VIN7 has been exceeded.
Beeper Status 4	07h Bank#3	00000000	Beeper Status 4 register (read to clear) <7:1>=Reserved <0>/ RO = 1, indicates a High or Low limit on VIN12 has been exceeded.
Beeper Mask 3	08h Bank#3	11111111	Beeper mask3 register <7>/RW= 1, disable the TXD2 temperature sense can match the target temperature value in the FAN control A register to generate the beep tone. <6>/RW= 1, disable the TXD3 temperature sense can match the target temperature value in the FAN control B register to generate the beep tone. <5>=Reserved <4>/RW= 1, disable the VIN11 beeper status bit to generate the beep tone. <3>/RW= 1, disable the VIN10 beeper status bit to generate the beep tone. <2>/RW= 1, disable the VIN9 beeper status bit to generate the beep tone.

			<1>/RW= 1, disable the VIN8 beeper status bit to generate the beep tone. <0>/RW= 1, disable the VIN7 beeper status bit to generate the beep tone.
Beeper Mask 4	09h Bank#3	11111111	Beeper mask4 register <7:1>=Reserved <0>/RW= 1, disable the VIN12 beeper status bit to generate the beep tone.
Beeper Control	0Ah Bank#3	00000000	Beeper Control register <7:1>= Reserved <0>/RW = 1, BEEPER# pin output for visual identification. 0, BEEPER# pin output for audio identification.
Block read length	0Bh Bank#3	00000001	***Block read length register*** <7:6>= Reserved <5:0>/RW= NVRAM block read length - Reserved - 1 byte - 2 bytes - 3 bytes _. 1F- 31 bytes 20- 32 bytes 21:3F- Reserved
Temperature adjust 1	10h Bank#3	00000000	Temperature adjustment 1 register <7:5> = Reserved. <4:0>/RW = offset value for TXD3 read out 01111 +30 degree 01110 +28egree 01101 +26 degree 01100 +24 degree 01011 +22 degree 01010 +20 degree 01001 +18 degree 01000 +16 degree 00111 +14 degree 00110 +12 degree 00101 +10 degree 00100 +8 degree 00011 +6 degree 00010 +4 degree 00001 +2degree 00000 No adjustment 11111 -2 degree 11110 -4 degree 11101 -6 degree 11100 -8 degree 11011 -10 degree 11010 -12 degree 11001 -14 degree

			11000 -16 degree 10111 -18 degree 10110 -20 degree 10101 -22 degree 10100 -24 degree 10011 -26 degree 10010 -28 degree 10001 -30 degree 10000 -32 degree
Temperature adjust 2	11h Bank#3	00000000	Temperature adjustment 2 register <7:5> = Reserved. <4:0>/RW = offset value for TXD2 read out 01111 +30 degree 01110 +28egree 01101 +26 degree 01100 +24 degree 01011 +22 degree 01010 +20 degree 01001 +18 degree 01000 +16 degree 00111 +14 degree 00110 +12 degree 00101 +10 degree 00100 +8 degree 00011 +6 degree 00010 +4 degree 00001 +2degree 00000 No adjustment 11111 -2 degree 11110 -4 degree 11101 -6 degree 11100 -8 degree 11011 -10 degree 11010 -12 degree 11001 -14 degree 11000 -16 degree 10111 -18 degree 10110 -20 degree 10101 -22 degree 10100 -24 degree 10011 -26 degree 10010 -28 degree 10001 -30 degree 10000 -32 degree
Temperature adjust 3	12h Bank#3	00000000	Temperature adjustment 3 register <7:5> = Reserved. <4:0>/RW = offset value for TXD1 read out 01111 +30 degree 01110 +28egree

			01101	+26 degree
			01100	+24 degree
			01011	+22 degree
			01010	+20 degree
			01001	+18 degree
			01000	+16 degree
			00111	+14 degree
			00110	+12 degree
			00101	+10 degree
			00100	+8 degree
			00011	+6 degree
			00010	+4 degree
			00001	+2degree
			00000	No adjustment
			11111	-2 degree
			11110	-4 degree
			11101	-6 degree
			11100	-8 degree
			11011	-10 degree
			11010	-12 degree
			11001	-14 degree
			11000	-16 degree
			10111	-18 degree
			10110	-20 degree
			10101	-22 degree
			10100	-24 degree
			10011	-26 degree
			10010	-28 degree
			10001	-30 degree
			10000	-32 degree
ASR control (refer to NOTE 3)	20h Bank#3	<7>=0, <6:0>= 0000000	Automatic Server Restart control register <7>/RO= 1, Enable the ASR; 0, Disable the ASR <6:0>/RW= ASR enable/disable pattern field	
ASR SMI count (refer to NOTE 4)	21h Bank#3	00000000	Automatic Server Restart SMI count register <7:0>/RW= time out period left in minute, where 00000000 indicates that ASR is disabled.	
ASR RESET count (refer to NOTE 4)	22h Bank#3	00000000	Automatic Server Restart RESET count register <7:0>/RW= time out period left in minute, where 00000000 indicates that ASR is disabled.	

Register	Offset	Power on/Reset Default value	Description
ASR signal control	23h Bank#3	00000000	Automatic Server Restart signal control register <7:2>= Reserved. <1>/RW 1, Enable the assert/output of internal AMURSTOUT signal when ASR RESET counter counts down to zero. 0, Disable the output of internal AMURSTOUT signal when ASR RESET counter counts down to zero. The AMURSTOUT won be asserted until ASR is enabled through writing correct patterns into the ASR control register. <0>/RW= 1, Enable the assert/output of SMI# signal when ASR SMI counter counts down to zero. 0, Disable the output of SMI# signal when ASR SMI counter counts down to zero. . The SMI# won be asserted until ASR is enabled through writing correct patterns into the ASR control register.
CF1~CF4 register Value For winbond only.	80h Bank#3		<7:4>=Reserved. <3>=CF4, representing the register value of CF4. <2>=CF3, representing the register value of CF3. <1>=CF2, representing the register value of CF2. <0>=CF1, representing the register value of CF1.
100/66#, FS0~FS3 register value For winbond only.	81h Bank#3		<7:5>=Reserved. <4>=100/66#, representing the register value of 100/66# <3>=FS3, representing the register value of FS3. <2>=FS2, representing the register value of FS2.. <1>=FS1, representing the register value of FS1. <0>=FS0, representing the register value of FS0.
Value RAM	00h-3Fh		
Value RAM	60h-9Fh		

Note:

1. Reading the interrupt status register will output the content of the register, and reset the register.
2. Current registered vendor ID are:
   Winbond-5CA3 ,Holtek- 12C3
3. The ASR is disabled after power on or reset. The function can only be enabled by consecutively writing a pattern of 40h, 52h, 54h, 52h to this field. After the ASR is enabled, bit-7 of ASR control register will be set to “1”. To disable the ASR feature, a consecutive pattern of 4Eh, 55h, 44h, 51h should be written into this field. The bit-7 of this register will be reset to “0”.
4. Write to the ASR SMI/RESET count register will set the ASR time out period. After a non-zero value is written into ASR SMI count register, the SMI count register begins to count down no matter the ASR is enabled or disabled. When the register count down to zero (The bit_7 of the intrusion control register is set to reflect the fact that ASR SMI counter has count down to zero) and the SMI# output is enabled in the ASR signal control register, SMI# signal will be asserted. At the same time, the ASR RESET count register begins to count (as long as its value is not zero) no matter the SMI# assertion is enabled or disabled. When the ASR RESET count register also counts down to zero, the AMURSTOUT (once asserted, it will last for 30ms and then deasserted automatically) will be asserted to reset the system, if its assertion is enabled by the bit 1 of ASR signal control register, and bit_7 of the Intrusion Reset register will be set to a “1” to indicate there occurs ASR RESET count to zero. The design of ASR signal control register intends to provide the testing of those counter function. For normal operation, the ASR SMI count register must be updated periodically to prevent a

the ASR RESET counter to count down and thus to avoid a system reset. Those registers will count down no matter the ASR feature is enabled or disabled.

Value RAM- Address 00h~3Fh or 60h~9Fh (auto-increment)

Address	Address with Auto-increment	Description	Remark
20h	60h	VIN0 reading (Vcore1)	
21h	61h	VIN1 reading (Vcore2)	
22h	62h	VIN2 reading (+3V)	
23h	63h	VIN3 reading (+5V)	
24h	64h	VIN4 reading (+12V)	
25h	65h	-VIN5 reading (-12V)	
26h	66h	-VIN6 reading (-5V)	
27h	67h	Ambient temperature reading	If the thermister/transistor is not connected, the read out value should be FFh
28h	68h	Fan 1 speed reading	How to identify a failure fan or no fan???
29h	69h	Fan 2 speed reading	How to identify a failure fan or no fan???
2Ah	6Ah	Fan 3 speed reading	How to identify a failure fan or no fan???
2Bh	6Bh	VIN0 High limit	
2Ch	6Ch	VIN0 Low limit	
2Dh	6Dh	VIN1 High limit	
2Eh	6Eh	VIN1 Low limit	
2Fh	6Fh	VIN2 High limit	
30h	70h	VIN2 Low limit	
31h	71h	VIN3 High limit	
32h	72h	VIN3 Low limit	
33h	73h	VIN4 High limit	
34h	74h	VIN4 Low limit	
35h	75h	-VIN5 High limit	
36h	76h	-VIN5 Low limit	
37h	77h	-VIN6 High limit	
38h	78h	-VIN6 Low limit	
39h	79h	Ambient over temperature limit	
3Ah	7Ah	Ambient temperature Hysteresis limit	
3Bh	7Bh	Fan 1 fan count limit	
3Ch	7Ch	Fan 2 fan count limit	
3Dh	7Dh	Fan 3 fan count limit	
3E~3Fh	7E~7Fh	Reserved	
00h	80h	VIN7 reading (+5VSB)	
01h	81h	VIN8 reading (CMOS battery)	
02h	82h	VIN9 reading (+2.5V)	
03h	83h	VIN10 reading (+1.5V)	
04h	84h	VIN11 reading (NVRAM battery)	
05h	85h	VIN12 reading (+3VSB)	
06h	86h	Reserved	
07h	87h	VIN7 High limit	
08h	88h	VIN7 Low limit	
09h	89h	VIN8 High limit	
0Ah	8Ah	VIN8 Low limit	
Address	Address	Description	Remark

	with Auto-increment		
0Bh	8Bh	VIN9 High limit	
0Ch	8Ch	VIN9 Low limit	
0Dh	8Dh	VIN10 High limit	
0Eh	8Eh	VIN10 Low limit	
0Fh	8Fh	VIN11 High limit	
10h	90h	VIN11 Low limit	
11h	91h	VIN12 High limit	
12h	92h	VIN12 Low limit	
13h	93h	Reserved	
14h	94h	Reserved	

Appendix
LM75 register & ASUSTeK ASIC register extension

The standard LM75 contains 4 registers: TEMPERATURE register, CONFIGURE register, Thyst register, Tos register as defined below:

Register	Offset	Power on/reset default value	Description
Temperature	00h	-	Detected temperature register (RO) <15:7> Current measured temperature (0.5蚓 precision, 2 complement value) <6:0> Reserved NOTE: If there is no thermister/transistor connected, the readout value should be all "1"
Control	01h	<7:0>=00001000	Control register (R/W) <7:5> Reserved <4:3> Fault Queue- Number of faults necessary to detect before setting THERM# output to avoid false tripping due to noise 00 1 time 01 2 times 10 4 times 11 6 times <2> THERM# polarity- 1, active HIGH; 0, active LOW <1> Comparator/interrupt mode- 0, comparator mode; 1, interrupt mode. <0> Shutdown- A "1" will set the LM75 goes to low power shutdown mode.
Thyst	02h	<15:0>= 01001011_00000000 (75蚓)	Thyst register <15:7> Thyst value (0.5蚓 precision). This value is designed to de-asserted THERM# while it is asserted. The THERM# is asserted when LM75 detects a temperature higher than the value in Tos register. Thatan over temperature situation. However, The THERM# won be de-asserted until the detected temperature goes below the value of Thyst. <6:0> Reserved

Tos	03h	<15:0>= 01010000_00000000 (80蚓)	Tos register <15:7> Over temperature limit (0.5°C precision). The THERM# will be asserted while the detected temperature goes above the value of this register. <6:0> Reserved

Below contain the ASUSTeK ASIC register extension definition which should be implemented in the secondary LM75 (the one with default I2C address of 1001000b)

Register	Offset	Power on/reset default value	Description
General Purpose Output 1	80h	<7:0>=***1***000***1***000	General Purpose Output 1 register <7>/RW= 1, GPO8 is HIGH; 0, GPO8 is LOW <6>/RW= 1, GPO7 is HIGH; 0, GPO7 is LOW <5>/RW= 1, GPO6 is HIGH; 0, GPO6 is LOW <4>/RW= 1, GPO5 is HIGH; 0, GPO5 is LOW <3>/RW= 1, GPO4 is HIGH; 0, GPO4 is LOW <2>/RW= 1, GPO3 is HIGH; 0, GPO3 is LOW <1>/RW= 1, GPO2 is HIGH; 0, GPO2 is LOW <0>/RW= 1, GPO1 is HIGH; 0, GPO1 is LOW PS Powered by +5V VDD, ***reset by PWROK.***
General Purpose Output 2	81h	<7:0>=**00*X*10000**	General Purpose Output 2 register ***<7> Reserved.*** <6>=/RW, ***GPO1~13, and GPO15***, and CLKRST# software reset control register, active high, self-clear, default LOW. If a "1" is written to this register, then the above signals mentioned should be reset to its default value. *<5> Reserved.* <4>/RW= 1, CLKRST# is HIGH. 0, CLKRST# is LOW for 50ms and then return to 1/HIGH. In other words, a 50ms LOW pulse is asserted. <3>/RW= 1,GPO12 is HIGH; 0,GPO12 is LOW <2>/RW= 1, GPO11 is HIGH; 0, GPO11 is LOW <1>/RW= 1, GPO10 is HIGH; 0, GPO10 is LOW <0>/RW= 1, GPO9 is HIGH; 0, GPO9 is LOW Note: When bit 4 is programmed to "0", the CLKRST# signal will not be asserted as LOW until ***300*** ms later. Once asserted, the LOW level will be kept for 50ms and then de-asserted. PS Powered by +5V VDD, ***reset by PWROK.***
General Purpose Input 1	82h	<7:0>	General Purpose Input 1 register <7:2>= Reserved <1>/R= PWRLOSS_FLAG: 1, GPI2 is HIGH; 0, GPI2 is LOW <0>/R= NEWCPU_FLAG: 1, GPI1 is HIGH; 0, GPI1 is LOW PS Powered by +5V VDD

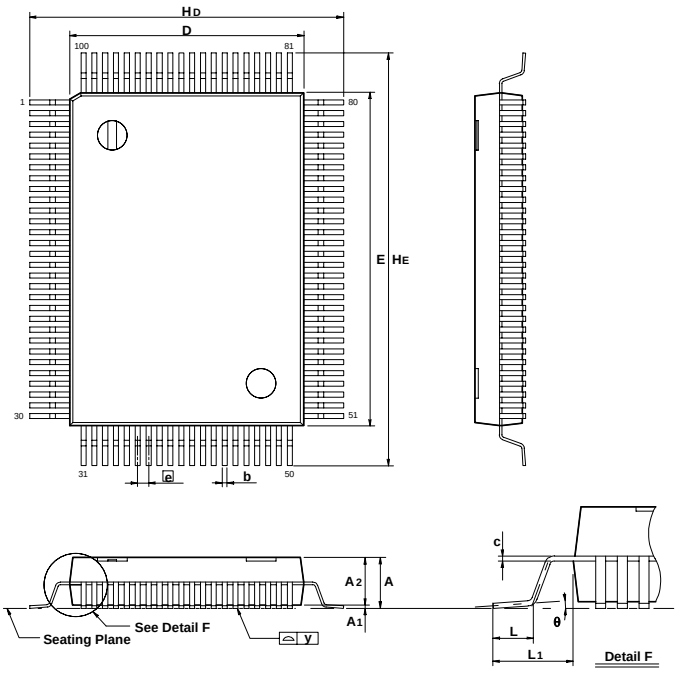
Register	Offset	Power on/reset default value	Description
General Purpose Output 3	83h	<7:0>=00000000	General Purpose Output 3 register <7:4>= Reserved ***<3>/RW=1, GPO 13 is HIGH, 0, GPO13 is LOW*** ***This bit is powered by +5VSB and can be reset by GRSMRST# and BATT power-on.*** ***<2>Reserved.*** ***<1>/RW= 1, GPO16 is HIGH. 0, GPO16 is LOW.*** ***This bit is powered by Battery voltage (VBAT), please be care of current leakage problem. This bit can be reset by battery power-on reset.*** ***<0>/RW= 1, GPO14 is HIGH. 0, GPO14 is LOW.*** ***This bit is powered by Battery voltage (VBAT), please be care of current leakage problem. This bit can be reset by battery and 5VSB power-on reset.***
General Purpose Input 2	84h	<7:0>=00000000	General Purpose Input 2 Register <7:1>=Reserved <0>/R=JEN status bit.
General Purpose Output 4	85h	<7:0>=00011111 VID output on bit <4:0>	General Purpose Output 4 register <7:6>= Reserved **<5>/RW=1, VID4~VID0 are output pins, and bit<4:0> control VID4~0 output values.** **0, VID4~0 are input pins and ignore bit<4:0>setting.** **<4>/RW=VID4 output when bit 5 is set.** **<3>/RW=VID3 output when bit 5 is set.** **<2>/RW=VID2 output when bit 5 is set.** **<1>/RW=VID1 output when bit 5 is set.** **<0>/RW=VID0 output when bit 5 is set.** PS Powered by +5VSB but output buffer driving by +5V. ***Reset by GRSMRST# and IN_NEWCPU#*.**
I2C address setting for security circuit I/F	86h	<7:0>=00101111	I2C address setting for security circuit interface.
General Purpose Output 5	87h	<7:0>=00000000	<7:1> Reserved. <0>/RW= 1, GPO15 is HIGH. 0, GPO15 is LOW. ***This bit can be cleared by PWROK and software reset(Reg 81h bit 6).***
General Purpose Input 2 For Holtek only.	88H	<7:0>	<7:4>Reserved.: <3>/R=CF4, representing the register value of CF4. <2>/R=CF3, representing the register value of CF3. <1>/R=CF2, representing the register value of CF2. <0>/R=CF1, representing the register value of CF1.
General Purpose Input 3 For Holtek only.	89H	<7:0>	<7:5>Reserved. <4>/R=100/66#, representing the register value of 100/66#. <3>/R=FS3, representing the register value of FS3. <2>/R=FS2, representing the register value of FS2. <1>/R=FS1, representing the register value of FS1. <0>/R=FS0, representing the register value of FS0.

Below contain the ASUSTeK ASIC register extension definition which should be implemented in the security circuit I/F (with default I2C address of 00101111b)

Test Register 1	D0h	<7:0>=00000000	Reserved.
Test Register 2	D1h	<7:0>=00000000	Reserved.
Test Register 3	D2h	<7:0>=00000000	Reserved.
Test Register 4	D3h	<7:0>=00000000	Reserved.
Test Register 5	D4h	<7:0>=00000000	Reserved.
Status Register	E0h	<7:0>=00000000	Security circuit interface status register <7>/R=1 seed code is ready for read. =0 seed code is not ready for read. <6>/R=1 Ready for host to write check code into register E8h~EBh. =0 Not ready for host to write check code into register E8h~EBh. <5>/R=1 security checking is already completed. =0 security checking is processing or not issued yet. <4>/R=1 security check OK. =0 security check failed. <3:0> Reserved.
Hour Register	E1h	<7:0>=00000000	<7:0>/RW written by host with RTC hour parameter.
Minute Register	E2h	<7:0>=00000000	<7:0>/RW written by host with RTC minute parameter.
Second Register	E3h	<7:0>=00000000	<7:0>/RW written by host with RTC second parameter.
Seed Register 1	E4h	<7:0>=00000000	<7:0>/R Seed<31:24>
Seed Register 2	E5h	<7:0>=00000000	<7:0>/R Seed<23:16>
Seed Register 3	E6h	<7:0>=00000000	<7:0>/R Seed<15:8>
Seed Register 4	E7h	<7:0>=00000000	<7:0>/R Seed<7:0>
Check code register 1	E8h	<7:0>=00000000	<7:0>/RW= Check code <31:24>
Check code register 2	E9h	<7:0>=00000000	<7:0>/RW= Check code <23:16>
Check code register 3	EAh	<7:0>=00000000	<7:0>/RW= Check code <15:8>
Check code register 4	EBh	<7:0>=00000000	<7:0>/RW= Check code <7:0>
Test Register 6	F6h	<7:0>=00000000	Reserved.
Test Register 7	F7h	<7:0>=00000000	Reserved.

PACKAGE DIMENSIONS

(100-pin QFP)



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.010	0.012	0.016	0.25	0.30	0.40
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.50	0.65	0.80
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	0.087	0.094	0.103	2.21	2.40	2.62
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.