VT82C570M

APOLLO MASTER

Green Pentium/P54C PCI/ISA System with Plug and Play and Master Mode PCI-IDE

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VIA TECHNOLOGIES, INC.

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VIA VT82C570M APOLLO MASTER PENTIUM/P54C PCI/ISA GREEN PC SYSTEMS WITH PLUG AND PLAY AND MASTER MODE PCI-IDE CONTROLLER

FEATURES

* PCI/ISA Green PC Ready

* High Integration

- **VT82C575M** system controller
- **VT82C576M** PCI bus controller
- Two instances of the **VT82C577M** data buffers
- Glueless interface to the **VT82C416** integrated clock generator, real time clock with extended CMOS, plug and play control and keyboard controller with PS/2™ mouse support
- Ten TTLs for a complete main board implementation

* Flexible CPU Interface

- 64-bit P54C™, Pentium™, K5™ and M1™ CPU interface
- 3.3v or 5v CPU and cache interface
- CPU external bus speed up to 66Mhz (internal 150Mhz and above)
- Supports CPU internal write-back cache
- Concurrent CPU/cache and PCI/DRAM operation
- System management interrupt, memory remap and STPCLK mechanism
- Cyrix M1 linear burst support
- CPU NA#/Address pipeline capability

* Advanced Cache Controller

- Direct map write back or write through secondary cache
- Burst Synchronous (Pipelined or non-pipelined), asynchronous SRAM and Cache Module support
- Eight-pin CWE# and GWE# control options
- Flexible cache size: 0K/128K/256K/512K/1M/2MB
- 32 byte line size to match the primary cache
- Integrated 10-bit tag comparator
- Interleaved SRAM access
- 3-1-1-1 read/write timing for Burst Synchronous SRAM access at 66Mhz
- 3-2-2-2 (read) and 4-2-2-2 (write) timing for interleaved asynchronous SRAM access at 66Mhz
- Data streaming for simultaneous primary and secondary cache line fill
- System and video BIOS cacheable and write-protect
- Programmable cacheable region and cache timing
- Optional combined tag and alter bit SRAM for write-back scheme

* Fast DRAM Controller

- Concurrent DRAM Writeback
- Four levels of CPU/cache to DRAM write buffer
- Standard Page Mode/EDO/Burst EDO-DRAM support in a flexible/mixed combination

- EDO-DRAM auto-detect
- Mixed 256K/512K/1M/2M/4M/8M/16MxN DRAMs
- 8 banks up to 512MB DRAMs
- Flexible row and column addresses
- 64 bit or 32 bit data width
- Burst read and write operation
- Programmable DRAM timing
- BIOS shadow at 16KB increment
- System management memory remapping
- Decoupled and burst DRAM refresh with staggered RAS timing
- CAS-before-RAS refresh timing

* Intelligent PCI Bus Controller

- 32 bit PCI interface
- PCI Master snoop ahead and snoop filtering
- Concurrent PCI master/CPU/IDE operations
- Synchronous Bus to CPU clock with divide-by-two from the CPU clock
- Multiple accelerated schemes for high bus throughput
- Automatic detection of data streaming burst cycles from CPU to the PCI bus
- Four level of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- PCI to system memory data streaming up to 110Mbyte/sec
- Four level of post write buffers from PCI masters to DRAM
- Four level of prefetch buffers from DRAM for access by PCI masters
- Zero wait state PCI master and slave burst transfer rate
- Complete steerable PCI interrupts
- IDE and ISA bus through peer PCI bus to avoid slower traffic blocking the regular PCI bus
- PCI-2.1 compliant

* Enhanced Master Mode PCI IDE Controller

- Dual channel master mode PCI supports four Enhanced IDE devices
- Mode 4 and Mode 5 transfer rate up to 22MB/sec
- Sixteen doubleword of prefetch and write buffers
- Interlaced commands between two channels
- Separate IDE data bus and control signals from the PCI and ISA bus to reduce loading and to enhance performance
- Bus master programming interface for ATA controllers SFF-8038 rev.1.0 compliant
- Full scatter and gather capability
- Support ATAPI compliant devices
- Support PCI native and ATA compatibility modes
- Complete software driver support

* Plug and Play Controller

- Dual interrupt and DMA signal steering with plug and play control
- Two programmable chip selects
- Microsoft Windows 95™ and plug and play BIOS compliant

* Sophisticated Power Management Unit

- Normal, doze, sleep, suspend and conserve modes
- System event monitoring with two event classes
- One idle timer, one peripheral timer and one general purpose timer
- More than ten general purpose Input/Output ports

- Six external event input ports with programmable SMI condition
- Complete leakage control when external component is in power off state
- Primary and secondary interrupt differentiation for individual channels
- Clock stretching, clock throttling and clock stop control
- Multiple internal and external SMI sources for flexible power management models
- APM 1.1 compliant

* **Synchronous ISA Bus Controller**
  - Synchronous ISA bus clock
  - Programmable wait state, command delay and IO recovery time
  - Bus conversion and data alignment
  - Hardware and software de-turbo control
  - Fast reset and Gate A20 operation
  - Integrated 82C206 peripheral controller
  - Edge trigger or level sensitive interrupt
  - Flash EPROM and combined BIOS support
* **Built-in nand-tree pin scan test capability**
* **0.6um mixed voltage, high speed and low power CMOS process**
* **208 pin PQFP for VT82C575M**
* **208 pin PQFP for VT82C576M**
* **100 pin PQFP for VT82C577M**
* **100 pin PQFP for VT82C416**

OVERVIEW

The VT82C570M ***Apollo Master*** is a high performance, cost-effective and energy efficient chip set for the implementation of PCI/ISA desktop and notebook personal computer systems based on the 64-bit P54C/Pentium/K5/M1 super-scalar processors. Either 3.3v or 5v CPU and cache interface is supported up to 66Mhz CPU external bus speed (with CPU internal speed up to 150Mhz and above). In either case, DRAM, PCI and ISA bus runs at 5v voltage level.

The VT82C570M chip set consists of the VT82C575M system controller, the VT82C576M PCI bus controller with integrated master mode Enhanced-IDE controller, and two instances of the VT82C577M data buffers. The CPU bus is minimally loaded with only the CPU, secondary cache and the chip set. The VT82C577M data buffers isolate the CPU bus from the DRAM, PCI and ISA bus so that CPU and cache operation may run reliably at the high frequencies demanded by today's processors. The chip set also interfaces directly with the VT82C416 integrated clock generator, real time clock with extended CMOS (128 byte) and keyboard controller with PS2 mouse support. A complete main board can be implemented with only ten TTLs. Please refer to Figure 1 for the system block diagram.

The VT82C570M supports eight banks of DRAMs up to 512MB. The DRAM controller supports Standard Page Mode DRAM, EDO-DRAM and Burst EDO-DRAM in a flexible mixed/match manner. The eight banks of DRAM are grouped into four pairs with an arbitrary mixture of 256K/512K/1M/2M/4M/8M/16MxN DRAMs. Zero, one or both banks may be populated in each pair with either 32bit or 64bit data width.

The secondary (L2) cache is based on Burst Synchronous (Pipelined or non-pipelined) SRAM, asynchronous SRAM or cache module from 128KB to 2MB. For burst synchronous SRAMs, 3-1-1-1 timing can be achieved for both read and write transactions at 66Mhz. For standard SRAMs, 3-2-2-2 and 4-2-2-2 timing can be achieved for interleaved read and write transactions at 66Mhz. Four levels of CPU/cache to DRAM write buffers with concurrent write-back capability are included in the VT82C577M data buffer chips to speed up the cache read and write miss cycles. For primary cache fill cycles that result in secondary cache misses, the primary and secondary caches are filled up concurrently to further enhance the performance.

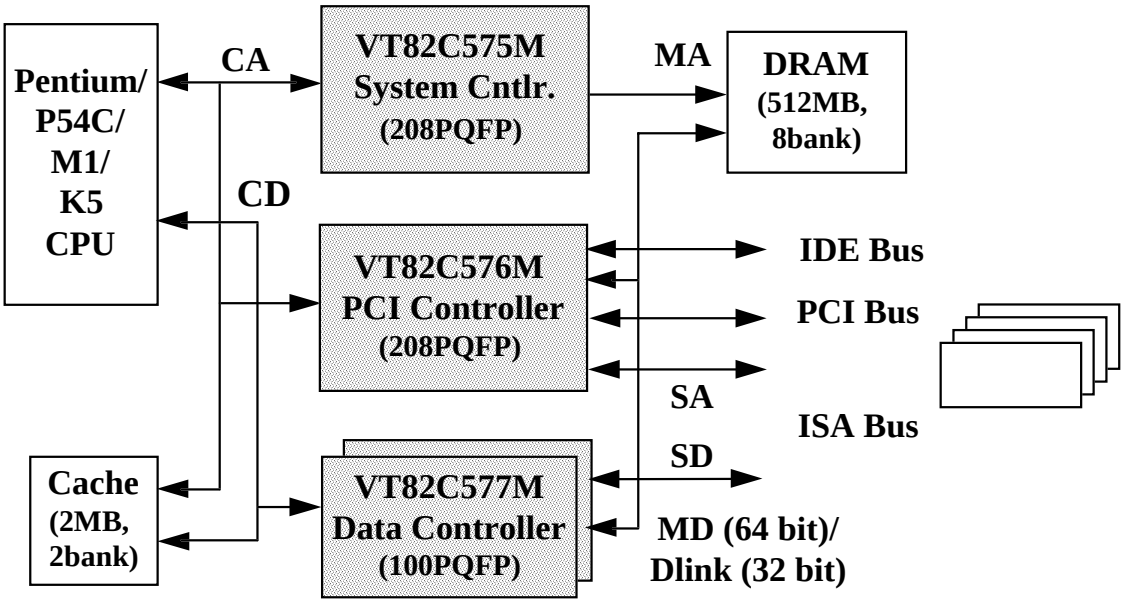

Figure 1. VT82C570M System Block Diagram

The VT82C570M supports the shadowing of the system, video and other BIOS to speed up the access. The video and system BIOS can also be write-protected and made cacheable. The unused portion of the DRAM can be relocated to increase the size of the overall system memory. Access cycles to either E or C segment can be programmed to be an on-board EPROM cycle to allow the combination of system and video BIOS for an all-in-one system board implementation. The VT82C570M can also be programmed to recognize write cycles as EPROM cycles to support field upgradability of flash EPROM BIOS.

The VT82C570M supports 32-bit PCI bus with 64-bit to 32-bit data conversion. Four levels of post write buffers are included to allow for concurrent CPU and PCI operation. Consecutive CPU addresses are converted into burst PCI cycles with byte merging capability for optimal CPU to PCI throughput. A 32-bit fast data link is established between the two VT82C577M data units and the VT82C576M PCI bus controller so that the address, data and command information for CPU to PCI bus transactions is contained in the same chip. This arrangement, unique to the VT82C570M chip set is crucial in achieving zero wait state buffer movement and implementing sophisticated and upgradable buffer management schemes such as the byte merging. For PCI master operation, four levels of post write buffers and four levels of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. Snoop Ahead and Snoop Filtering mechanisms are implemented to allow PCI bus master transfer rates greater than 110MB/s for typical applications. Furthermore, the ISA and IDE bus are steered through a peer PCI bus so that the slower traffic does not block the normal traffic of the regular PCI bus. The VT82C570M is PCI 2.1 compliant.

The integrated master mode IDE controller supports a dual channel/four device enhanced IDE bus with sixteen levels of double-word prefetch and write buffers. The data bus, control signals, write buffers and prefetch buffers are separated from those of the PCI bus so that performance and electrical loading are optimized. The command and recovery time of each IDE device can be individually programmed in units of PCI bus clock to achieve optimal speed of the device up to >22MB/s. Other features of the IDE controller include interlaced dual channel commands, full scatter and gather capability, bus master programming interface for ATA controllers SFF-8038 compliant and complete software driver support.

The VT82C570M provides two plug and play ports for converting non plug and play devices into plug and play devices on the main board. The configuration mechanism is compliant with the plug and play BIOS and the Microsoft Windows 95™ operating system.

The integrated power management unit offers the following modes: normal, doze, sleep, suspend and conserve. To determine the power management mode, the power management unit monitors IO events, interrupt, DMA and PCI master request signals to detect the status of system activity. Each event can be turned off or assigned to one of two event classes tracked by an idle timers, a peripheral timer and a general purpose timer. The system management interrupt (SMI) may be triggered by multiple sources including time-out of individual timers, occurrence of system activities, external input and software programming for flexible applications. Clock speed switching (or throttling), IO and power control are functions performed by the SMI routine. The power management unit is APM 1.1 compliant.

The VT82C577M data buffers separate the CPU/cache and PCI/DRAM bus so that the two busses may run concurrently. At the CPU side, the CPUs access cache without interfering with the PCI/DRAM bus unless a cache miss or non-cacheable cycle is encountered, in which case the write buffers with concurrent write back capability minimize the interface overhead. At the PCI/DRAM side, the PCI master devices access DRAM without interfering with the CPU/cache data bus unless a snoop hit occurs.

The VT82C570M is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook PCI/ISA computer systems.

FUNCTIONAL DESCRIPTION

1. Clock Logic

The VT82C570M supports 3.3v and 5v Pentium and compatible processors up to 66Mhz CPU external bus speed. The CPU interface, cache and DRAM controller runs at the same clock frequency as the CPU bus clock which may be fraction of the CPU internal frequency. Since the PCI bus runs at half the frequency of the CPU bus, the VT82C570M requires two clock inputs: one of the CPU frequency (CCLK) and the other of half the speed (PCLK). The companion VT82C416 supports both clocks, the frequency of which is controlled by bit 3-0 of internal register RX56h (CCLK).

0000 - 16Mhz	1000 - 8Mhz	0001 - 40Mhz	1001 - 20Mhz
0010 - 50Mhz	1010 - 25Mhz	0011 - 80Mhz	1011 - 40Mhz
0100 - 66Mhz	1100 - 33Mhz	0101 - 100Mhz	1101 - 50Mhz
0110 - 8Mhz	1110 - 4Mhz	0111 - 60Mhz	1111 - 30Mhz

At power on reset, the target CPU frequency is read in from the jumper setting of pins RAS#3-0. The frequency can be changed during CPU operation (with or without asserting STPCLK#) for power management purposes. The clock generator in the VT82C416 guarantees smooth frequency changes if the original and target frequencies fall in the same bank (same bit 3 of RX56h). The STPCLK# signal can be used for clock throttling to reduce the CPU power consumption.

The ISA bus clock can either be derived from the CCLK or be asynchronous according to the setting of bit 3-0 of RX11h.

0--- - CCLK/8	1000 - CCLK/3	1001 - CCLK/2
1010 - CCLK/4	1011 - CCLK/6	1100 - CCLK/5
1101 - CCLK/10	1110 - CCLK/12	1111 - OSC/2 (asynchronous)

2. CPU Interface

The VT82C570M responds to CPU generated bus cycles and activates the cache, DRAM, PCI and ISA state machines according to the command type and address range. The CACHE# input from the CPU is monitored to determine burst cycles and KEN# is returned to inform the CPU of the cacheability of the data. For memory cycles with inactive CACHE# signaling, the line is normally not cached into the secondary cache unless bit 2 of RX40h is set. The coherency of the CPU primary cache with the rest of the system is maintained by the KEN#, EADS# and HITM# pins. KEN# is normally active for a memory read cycle. If the CPU address lies outside the cacheable region, KEN# becomes inactive before the completion of the first burst transfer so that the data is not cached inside the CPU.

For DMA cycles, the CPU address is driven from the integrated DMA controller of the VT82C575M. For PCI or ISA master cycles, the CPU address is driven from the PCI or ISA bus through the integrated buffer inside the VT82C576M. The EADS# pin is asserted during DMA and master cycles to snoop the internal cache. If the HITM# signal is driven active by the CPU, then an altered internal cache line needs to be written back to the system before the intended memory access is performed. Snoop filtering and snoop ahead mechanism is implemented to minimize the snooping overhead during master accesses.

3. Advanced Cache Controller

3.1. Burst Synchronous and Asynchronous SRAMs

The VT82C570M supports direct-mapped cache systems with data size ranging from 128KB to 2MB. Burst synchronous, burst pipeline synchronous and asynchronous data SRAMs are supported to allow flexible system tradeoffs between cost and performance. The SRAM type is indicated in the following registers:

RX51h bit4	RX50h bit2	
1	-	Asynchronous SRAM
0	0	Non-pipelined Burst Synchronous SRAM
0	1	Pipelined Burst Synchronous SRAM

The VT82C570M also supports eight CWE# pins for each byte in addition to the global GWE# option (RX48h bit 6) which allows glueless interfacing with either discrete cache chips or cache modules.

3.2. Multiple Tag Options

The VT82C570M supports both write-back and write-through schemes with maximum flexibility in selecting the number of tag and alter bits (from eight to eleven bits). No valid bit is required in all cases since system data are maintained valid all the time after initialization.

The minimum number of tag plus alter bits is eight to fit the standard x8 SRAMs. Three schemes are supported under this configuration: write-through, write-back with alter bit and write-back without alter bit. To allow a larger cacheable region, more than one x8 SRAMs are required for wider combined tag plus alter bits. The VT82C570M supports tag bits up to ten in addition to the alter bit for the write-back scheme. Note that the alter bit cannot be used as the eleventh tag bit even if the alter bit is not used. Three register bits are used to distinguish different cache schemes as indicated in Table 1.

RX5Eh bit 6	RX50h bit 4	RX50h bit 3	write-thru/ write-back	tag-bits	alter-bit	total bits
0	0	0	write-back	8	0	8
0	0	1	write-back	7	1	8
0	1	0	write-back	8	1	9
0	1	1	write-back	10	1	11
1	-	0	write-thru	8	-	8
1	0	1	write-thru	7	-	N/A
1	1	1	write-thru	10	-	10

Table 1. Cache Schemes and Number of Tag/Alter Bits

3.3. Cache Timing

Cache read and write hit timing is 3-1-1-1 for burst (pipelined or standard) synchronous SRAMs. For asynchronous SRAMs, cache hit timing can be programmed to be either zero, one or two wait states in RX51h. The first read cycle, other read cycle (second to fourth cycle in a burst transfer), first write cycle and other write cycle can be programmed independently. The following table indicates the speed requirement of the tag and data SRAM for different CPU bus clock frequencies.

CPU Clock	Tag SRAM	Sync. SRAM	Read/write Timing (sync.)	Async. SRAM	Read/write Timing (async.)

50Mhz	-20	-20	3-1-1-1/3-1-1-1	-20	3-2-2-2/3-2-2-2
60Mhz	-15	-15	3-1-1-1/3-1-1-1	-20	3-2-2-2/4-2-2-2
66Mhz	-12	-12	3-1-1-1/3-1-1-1	-15	3-2-2-2/4-2-2-2

The following internal registers are associated with the cache controller:

RX50h: Cache access mode
- bit 7-6: cache mode. 0x: disabled.
  10: enabled 11: initialization
- bit 5: Cyrix CPU linear burst order: 0: disable
  1: enable
- bit 4-3: number of tag plus alter bits (see Table 1)
- bit 2: data synchronous SRAM type (if bit 4 of RX51h is 0):
  0: standard synchronous SRAM
  1: pipelined burst synchronous SRAM
- bit 1: cache read wait state for PCI masters (PCI clock)
  0: zero wait state (2-1-1-1)
  1: one wait state (3-2-2-2)
- bit 0: cache write wait state for PCI masters (PCI clock)
  0: zero wait state (2-1-1-1)
  1: one wait state (3-2-2-2)

RX51h: cache timing control
- bit 4: data SRAM type 0: synchronous SRAM (refer to bit2 of RX50h)
  1: asynchronous SRAM
- bit 7: read hit timing for the first cycle (CPU clock) for asynchronous SRAM:
  0: 1 wait state (3-x-x-x)
  1: 2 wait state (4-x-x-x)
- bit 6: write hit timing for the first cycle for asynchronous SRAM:
  0: 1 wait state (3-x-x-x)
  1: 2 wait state (4-x-x-x)
- bit 5: read hit timing for the second-fourth burst cycle for asynchronous SRAM:
  0: 1 wait state (x-2-2-2)
  1: 2 wait state (x-3-3-3)
  * write hit timing is always 1 wait state (x-2-2-2) for asynchronous SRAM
  * read hit and write hit timing is always 3-1-1-1 for synchronous SRAM
- bit 3: bank of data SRAM: 0: 1 bank 1: 2 banks
- bit 2-0: cache size 000: no cache 001: N/A
  010: N/A 011: 128KB
  100: 256KB 101: 512KB
  110: 1MB 111: 2MB

3.4. DRAM Post Write Buffers

The VT82C570M includes a four level DRAM post write buffer to optimize the performance of the L2 cache write miss and non-cacheable write operations. In this buffered arrangement, the fast CPU writes the data to the fast buffer and then terminates the cycle without any wait states. Once the cycle is terminated, the CPU may start a new operation and the DRAM controller concurrently writes the data from the buffer to the DRAM.

3.5. Concurrent DRAM Writeback

In order to bypass the performance penalty imposed by the DRAM during writeback operations, the VT82C570M supports Concurrent DRAM Writeback operation. During a cache read miss with

dirty line replacement, there are two operations necessary: the dirty line in the L2 cache must be written back to the DRAM first and then current data must be filled to the L2 cache. The Concurrent DRAM Writeback mechanism involves the use of two fast zero-wait FIFO data buffers. While the dirty line is read into the first FIFO, the new DRAM data is read into the second FIFO concurrently. After the end of the L2 to FIFO fill, the CPU then reads the data from the second FIFO along the L2 cache fill. Concurrently, the data in the first FIFO is written to the DRAM. Once the first data is read into CPU, the CPU can continue its operation without waiting for the completion of the L2 cache fill and the dirty line DRAM fill.

3.6. Cacheable Region

Only on-board DRAM can be made cacheable. The cacheable region is determined by the following factors:

- the cache size,
- the tag size,
- the on-board DRAM size,
- the setting of the programmable non-cacheable region (RX41h and RX42h), and
- the cacheability of video and system BIOS as determined by the setting of RX40h.

The normal cacheable region is the minimum of the on-board DRAM size and 256 (1024 if there are 10 tag bits) times the cache size. The decoding of the normal cacheable region is built inside the chip so that no register setting is required.

The upper memory region (A0000h to FFFFFh) is an exception to the normal case. Since this region corresponds to memory-mapped IO ports, it is defaulted to be non-cacheable. However, the video (C0000h to C7FFFh) and system (E0000h to EFFFFh and F0000h to FFFFFh) BIOS can be made cacheable and write-protect by programming RX40h.

One other memory region inside the normal cacheable space can be made non-cacheable by programming the internal register RX41h and RX42h. The size of the region is from 64KB to 4MB. The base address of the region must be an integral multiple of the size of the region.

The cacheable region is consistent between the primary and the secondary cache through the use of the KEN# and EADS# pins to the CPU.

4. Enhanced DRAM Controller

The VT82C570M supports eight banks of DRAMs up to 512MB. The eight banks are grouped into four pairs and each bank can be independently made of 256K, 512K 1M, 2M, 4M, 8M and 16MxN DRAMs. Zero, one or both banks of DRAMs may be populated in each pair. The DRAM controller can support standard page mode, EDO and Burst-EDO DRAMs with either 64bit or 32bit in flexible mixed combinations.

4.1. Standard Page Mode DRAM

The DRAM memory address generation is a function of the CPU and DRAM type. DRAM row and column addresses are multiplexed onto the same MA bus. When operating in non-page mode or on page misses, a row address followed by a column address is generated during the DRAM access. On page-hits, only a column address is generated during the DRAM access.

DRAM cycles normally operate in page mode. Each RAS# is held active after a DRAM access has finished and is precharged only when subsequent cycle to the same bank does not access the same DRAM page, or if an asynchronous event such as a RAS time-out.

For all CPU accesses, DRAM cycles are generated synchronously with the CPU clock. Critical DRAM timing parameters are individually programmable in RX22h to allow optimal matching between the DRAM and the CPU speed. The parameters include:

- bit 7-6: RAS# precharge time: 2-8 cycles,
- bit 5-4: RAS# pulse width: 4-10 cycles,
- bit 3-2: Read cycle CAS# pulse width: 1-4 cycles,
- bit 1: Write cycle CAS# pulse width: 1-2 cycles, and
- bit 0: RAS# to column address/column address to CAS#: 1-2 cycles.

The VT82C570M supports decoupled DRAM refresh (bit 0 of RX03h set) to allow on-board DRAM operation to continue before the slower ISA refresh is complete. Furthermore, CAS-to-RAS refresh (bit 3 of RX40h set) and slow refresh (bit 2 of RX5Eh set) are also supported to conserve power consumption and to allow more flexibility in selecting DRAMs with different refresh address requirement. In all cases, the RAS timing is staggered during refresh to minimize the power supply noise.

4.2. EDO and Burst EDO DRAM

The DRAM controller of VT82C575M supports both EDO and Burst EDO DRAMs in addition to standard page mode DRAMs. This feature enhances the DRAM read performance in comparison with a standard DRAM device by one and two CPU clocks, respectively. The composition of the eight bank DRAM can be of mixed EDO with standard DRAM modules in the bank bases. The DRAM controller will generate EDO, Burst EDO or standard cycle according to the type of DRAM in each bank.

A software/firmware mechanism that can automatically detect EDO DRAM device can be integrated into the BIOS so that user configuration effort may be reduced. Register RX47h indicates the DRAM type of each bank.

RX47: DRAM type -default (0)

7,3:	Bank 3	DRAM type
	00:	Standard DRAM
	01:	Burst EDO DRAM
	10:	EDO DRAM
	11:	Illegal
6,2:	Bank 2	
5,1:	Bank 1	
4,0:	Bank 0	

4.3. Other DRAM Parameters

The DRAM type, size and single/double bank information is indicated in the following registers:

RX43h: pair 0/1 DRAM size and configuration

- bit 7-5: bank-pair 0 DRAM size (x2 if double bank):

000: 1MB	001: 2MB
010: 4MB	011: 8MB
100: 16MB	101: 32MB
110: 64MB	111: 128MB

- bit 4: number of banks of pair 0

0: 1 bank	1: 2 banks

  (zero bank if bit 7-5 or RX20h is 0)
- bit 3-1: bank-pair 1 DRAM size
- bit 0: number of banks of pair 1 (zero bank if bit 3-1 of RX20h is 0)

RX44h: pair 2/3 DRAM size and configuration
- bit 7-5: bank-pair 2 DRAM size
- bit 4: number of banks of pair 2 (zero bank if bit 7-5 or RX21h is 0)
- bit 3-1: bank-pair 3 DRAM size
- bit 0: number of banks of pair 3 (zero bank if bit 3-1 of RX21h is 0)

RX20h: pair 0/1 row/column address
- bit 7-5: number of column address for pair 0

  000: disabled 001: 9 bit
  010: 10 bit 011: 11 bit
  100: 12 bit others: illegal
- bit 4: page mode operation

  0: disable 1: enable
- bit 3-1: number of column address for pair 1
- bit 0: DRAM bus width:

  0: 32 bit 1: 64 bit

RX21h: pair 2/3 row/column address
- bit 7-5: number of column address for pair 2
- bit 4: reserved
- bit 3-1: number of column address for pair 3
- bit 0: reserved

RX48h: 32/64bit width DRAM select for each bank
- bit7-4: reserved
- bit3-0: select 32/64bit width DRAM operation

  0: 32 bit 1: 64 bit

RX20<0>	RX48<3:0>	
0	X	;all banks are 32bit
1	0	;64bit operation for the corresponding DRAM bank
1	1	;32bit operation for the corresponding DRAM bank

5. Shadow RAM and ROM Decoding

The VT82C570M supports shadowing of system, video and other BIOS to speed up the access. The granularity is 16KB in address range C0000h to DFFFFh and 64KB in address range E0000h to FFFFFh. Read and write shadowing can be enabled or disabled independently in each region. Furthermore, read access to address range C0000h-C7FFFh and E0000h-FFFFFh can be programmed to be cacheable and write protected to further enhance the performance of video and system BIOS access.

If shadow RAM is not enabled, memory range A0000h to FFFFFh can be relocated to the top of the local DRAM so that the memory size is increased by 384KB. If only C (C0000h-CFFFFh) and/or F segments are used for shadowing, then the memory size is increased by 256KB. No DRAM can be relocated if either D or E segment is used as shadow memory. If the SMI capability is enabled, the memory range A0000h to BFFFFh is reserved for SM memory remap (RX5Bh bit 4 set) and cannot be relocated again. Therefore, the size of the increased memory reduces to 256KB and 128KB, respectively.

Accesses to either E or C segment can be programmed to be on-board ROM cycles. The E segment is used when the size of the system BIOS exceeds 64KB. The C segment is used when the video and system BIOS are combined into one single EPROM in an all-in-one system board implementation. A memory write cycle is typically not considered as a ROM cycle even if the address is decoded as such. To support flash EPROM which allows on-line modification of the memory content, the VT82C570M can be programmed to recognize such memory write cycles as ROM cycles (bit 6 of RX11h).

Furthermore, memory address range 15MB to 16MB can be programmed to be ISA cycles (instead of normal on-board DRAM cycles) if bit 2 of RX32h is set.

The following internal registers are associated with the shadow RAM and ROM decoding:

RX30h: C0000h-CFFFFh shadow control
- bit 7: CC000h-CFFFFh read shadow
  1- enable 0-disable
- bit 6: CC000h-CFFFFh write shadow
- bit 5-4: C8000h-CBFFFh read/write shadow
- bit 3-2: C4000h-C7FFFh read/write shadow
- bit 1-0: C0000h-C3FFFh read/write shadow

RX31h: D0000h-DFFFFh shadow control
- bit 7-6: DC000h-DFFFFh read/write shadow
- bit 5-4: D8000h-DBFFFh read/write shadow
- bit 3-2: D4000h-D7FFFh read/write shadow
- bit 1-0: D0000h-D3FFFh read/write shadow

RX32h: E0000h-FFFFFh shadow control
- bit 7-6: E0000h-EFFFFh read/write shadow
- bit 5-4: F0000h-FFFFFh read/write shadow
- bit 3: other usage
- bit 2: memory range F00000h-FFFFFFh always decoded as ISA cycle
- bit 1-0: other usage

RX33h: ROM decoding and memory relocation
- bit 7: C8000h-CFFFFh decoded as ROM cycle
  1 - enable 0 - disable
- bit 6: C0000h-C7FFFh decoded as ROM cycle
- bit 5: E8000h-EFFFFh decoded as ROM cycle
- bit 4: E0000h-E7FFFh decoded as ROM cycle
- bit 3-2: relocation 00 - disable 01 - illegal
  10 - 256K relocation 11 - 384K relocation
- bit 1-0: other

RX40h: ROM cacheable control
- bit 7: C0000h-C7FFFh cacheable and write-protect
  1 - enable 0 - disable
- bit 6: F0000h-FFFFFh cacheable and write-protect
- bit 5: E0000h-EFFFFh cacheable and write-protect
- bit 4-3: other usage
- bit 2: secondary cache fill for CACHE# inactive memory cycles

6. Intelligent PCI Bus Controller

The VT82C570M supports the 32-bit PCI bus synchronously at half the CPU frequency. The 64-bit to 32-bit data conversion and command regeneration are performed by the VT82C575M with minimum overhead. Four levels of post write buffers are included between the CPU and the PCI bus to allow for concurrent CPU and PCI operation. Consecutive CPU addresses are converted into burst PCI cycles with byte merging capability for optimal CPU to PCI throughput. A 32-bit fast data link is established between the two VT82C577M data units and the VT82C576M PCI bus controller so that the address, data and command information for CPU to PCI bus transactions is contained in the same chip. This arrangement, unique to the VT82C570M chip set, is crucial in achieving zero wait state buffer movement and also in implementing sophisticated and upgradable buffer management schemes such as the byte merging. For PCI master operation, four levels of post write buffers and four level of

prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. 2-1-1-1 cache hit and 2-1-2-1 cache miss timing is performed to achieve greater than 110MB/s PCI bus master transfer rate for typical applications. Furthermore, the ISA and IDE bus are steered through a peer PCI bus so that the slower traffic does not block the normal traffic of the regular PCI bus. The VT82C570M is PCI 2.1 compliant.

6.1. CPU to PCI Operation

The PCI bus controller contains four levels of post write buffers between the CPU and PCI bus. If the write-buffer is not full and the cycle belongs to the PCI bus, the cycle can be pushed into the write buffer. Note that both data and address information of the buffered cycles are contained in the same chip (VT82C576M) to achieve optimal buffer management. The PCI bus controller converts consecutive CPU accesses into burst cycles on the PCI bus. The controller also monitors address and byte enable signals and performs byte merge (when the situation permits) between the two consecutive CPU write cycles in the write buffers. Therefore, it reduces the number of PCI cycles and creates further bursting possibilities.

A single 64-bit cycle, if spread over both higher and lower double words is converted into two consecutive commands for the PCI bus controller with two PADS#. The CPU data is latched inside the VT82C577M data units and re-aligned to the 32-bit PCI bus controller.

The following registers control the operation of the PCI bus interface:

RX82h: buffer control
- bit 7: 1/0 = CPU to PCI write buffer enable/disable
- bit 6: 1/0 = PCI to memory write buffer enable/disable
- bit 5: reserved
- bit 4: 1/0 = PCI accessing memory prefetch buffer enable/disable
- bit 3: 1/0 = PCI accelerated decoding enable/disable
- bit 2: reserved
- bit 1: 1/0 = on-board memory burst write enable/disable
- bit 0: 1/0 = on-board memory burst read enable/disable

RX83h: data link control
- bit 7: 1/0 = data link write cycle at 0/1 wait state
- bit 6-4: reserved
- bit 3: 1/0 = on-board memory detection point for PCI master at first data phase/address phase
- bit 2-1: reserved
- bit 0: must be 0

RX84h: PCI interface timing
- bit 7: 1/0 = slave mode lock function enable/disable
- bit 6: 1/0 = retry count at 64 times/16 times
- bit 5: 1/0 = retry deadlock error reporting enable/disable
- bit 4: 1/0 = retry status occurred/not occurred (write 1 to reset)
- bit 3: 1/0 = CPU to PCI fast back to back enable/disable
- bit 2: 1/0 = fast FRAME# generation enable/disable
- bit 1-0: 11/10/01/00: DEVSEL# decoding is subtractive/slow/medium/fast

6.2. PCI to Memory Operation

The PCI bus controller contains four level of PCI to memory write buffers and four level of PCI from memory prefetch buffers to streamline the PCI and memory bus operation. On the memory bus side, the VT82C576M PCI bus controller requests the ownership of the memory bus to the VT82C575M system controller through the PREQ# pin. The PGNT# is granted to the PCI bus controller after arbitration with the CPU request. The address generated by the PCI bus controller is passed to the CPU bus to snoop the primary and secondary cache. If the address hits an altered line of

the primary cache, the altered line will be written back to the system (either DRAM or secondary cache) before the intended access can continue.

6.2.1. Snoop Ahead

CPUs with internal writeback cache systems need snoop operations to detect and compare the validity of the data in the cache in order to determine whether a writeback operation is required. The VT82C570M offers a snoop ahead feature to avoid the performance penalty of a normal snoop operation. The snoop ahead applies to the cycles of PCI master burst access to system memory or the L2 cache.

In a normal snoop operation, the DRAM/cache controller will discontinue burst operations when the master burst mode crosses the cache line. Then the controller will generate a snoop address to the CPU and wait one clock cycle for the CPU's response. If the CPU detects a non-coherence state between the L1 and system memory, the CPU would issue a HITM# signal. The HITM# signal instructs the PCI master to perform two operations: 1) back off from the memory bus and 2) initiate a L1 writeback cycle. If the CPU detects coherence between L1 and system memory, then the DRAM/cache controller would resume burst operations. In this normal snoop operation, the performance penalty is incurred when the controller waits one cycle for the CPU response.

In the VT82C570M snoop ahead feature, the main difference is that after the controller generates a snoop, the controller may continue burst operations without waiting one clock cycle for the CPU response. Since the cache line is sequentially incremented in the burst mode, the timing for the next cache line access can be predicted and the snoop address can be sent before the actual access. Consequently, by the time the physical access actually starts, the snoop address and the HITM# signal would already have been processed and the controller would not have to wait for the CPU response.

6.2.2. Concurrent CPU and PCI Master Operations

In typical systems, the operation of PCI master access to the bus is a bottleneck. When the PCI master issues a REQ# signal for control of the PCI bus, 1) the REQ# signal is sent to the PCI Arbitrator, 2) the PCI Arbitrator then sends a PREQ# signal to the CPU Arbitrator, 3) the CPU Arbitrator sends a HOLD signal to the CPU, 4) after the CPU completes its current cycle, it responds back to the CPU Arbitrator with a HLDA signal and allows the PCI master to see the CPU bus, 5) upon receiving HLDA, the CPU Arbitrator sends the PGNT# signal to the PCI Arbitrator, and 6) the PCI Arbitrator then sends a GNT# signal to the PCI master. Only after the PCI master receives the GNT# signal can the PCI master access the bus. Consequently, the long critical path of the signals imposes a large performance penalty whenever the PCI master tries to access the bus in typical systems.

This performance bottleneck is bypassed in the VT82C570M through the use of concurrent operations techniques. The PCI Arbitrator in the VT82C570M acts as a gate separating the CPU and PCI Master operations. When the PCI master issues a REQ# signal, the PCI Arbitrator will follow the PCI bus arbitration protocol and immediately grant the bus to the PCI master. The PCI Master can then access the slave device on the PCI bus and perform PCI master operations. During this time, the CPU and the CPU bus has not been interfered with. Consequently, the CPU and the CPU bus is left free to process other operations concurrently with the PCI master operations and the bottleneck is bypassed. However, if the PCI master needs to access an on-board device such as system memory or the L2 cache, then the PCI Arbitrator "gate" opens and a PREQ# signal is sent to the CPU Arbitrator (Note that PREQ# signal occurs after the PCI bus is granted to the PCI master).

6.3. PCI Arbitration and Interrupt Steering

The VT82C576M PCI bus controller arbitrates the ownership of the PCI bus between the four PCI masters and the controller itself. The arbitration is of rotational priority and provides the following register control in order to fine tune to specific application environments.

RX85h: PCI arbitration

- bit 7: 1/0 = fairness between CPU and PCI bus/priority on PCI bus

- bit 6: 1/0 = FRAME# based/REQ# based
- bit 5-4: 11/10/01/00 = CPU time slot in unit of 32/16/8/4 PCI clocks
- bit 3-0: PCI master bus time out
  0000: disable
  0001: 1 x 32 PCI clock
  0010: 2 x 32 PCI clocks
  .....
  1111: 15 x 32 PCI clocks

The interrupts signals from the PCI bus (INTA#-D#) along with those from the ISA bus and the two plug and play ports are completely steerable to the two 8259A compatible interrupt controllers inside the VT82C575M. Please refer to the "Plug and Play Controller" section for details.

6.4. PCI Configuration

The VT82C570M supports the standard PCI configuration mechanism #1 and #2 (determined by bit 7 of internal register RX86h, defaulted as mechanism #1). Under mechanism #1, IO address CF8h is used as the configuration address port and CFCh as the configuration data port. Both ports are 32-bit wide. If the VT82C570M detects a full double word write at address CF8h, the chip latches the value into it. Any other types of accesses to this address are treated as a normal IO access. The format of the configuration address is as follows:

- bit 31: configuration enable (this bit needs to be set to translate a configuration data access into a configuration cycle).
- bit 30-24: reserved
- bit 23-16: bus number (must be 0 to enable the configuration)
- bit 15-11: device number (00000 access the PCI bus controller internal registers, other values access other PCI devices)
- bit 10-8: function number (don't care for internal registers, but pass through to PCI bus for other PCI devices)
- bit 7-2: register number
- bit 1-0: always 00 (only type 0 format is supported)

Under mechanism #2, CPU IO read and write cycles to the C000-CFFFh address range are translated into PCI configuration read and write cycles, if configuration space enable register at address CF8h is enabled. The translation method carries the least significant 8 bits of the CPU address to the least significant 8 bits of the PCI address to select one of the 256 8-bit IO location in the PCI configuration space. Bits 8 to 11 of the CPU address are mapped to one of the 16 devices' IDSEL# input. These IDSEL# inputs of the PCI devices have to be hard-wired to one of the AD16-31 signals on the PCI bus. CA<11:8> being 0 accesses the internal configuration register of the VT82C570M and AD17-31 are available for other PCI devices.

Bus controller has both internal register and PCI configuration register. The internal configuration registers (RX80h to RXFFh) will not be able to access through either of the PCI configuration mechanism. It can be accessed through I/O ports A8 and A9 only.

The following PCI configuration registers are defined:

Configuration Register: Mandatory header field (or IDX00 and IDX04 based on the 32-bit IO port convention)

- IDX00<15:0> - Vendor ID = 1106h (read only)
- IDX00<31:16> - Device ID = 0576h (read only)
- IDX04<15:0> - Command register
  bit 0: IO space = 1 (read only)
  bit 1: memory space = 1 (read only)
  bit 2: bus master = 1 (read only)
  bit 3: special cycle monitoring = 0 (read only)
  bit 4: memory write and invalid command = 0 (read only)

bit 5: VGA palette snoop = 0 (read only)
bit 6: parity error response (read/write, default=0)
bit 7: address/data stepping = 0 (read only)
bit 8: SERR# enable (read/write, default=0)
bit 9: fast back-to-back cycle enable (read/write, default=0)
bit 15-10: reserved

- IDX04<31:16> - Status register (or IDX06<15:0>)
  bit 0-6: reserved
  bit 7: fast back-to-back: reserved
  bit 8: data parity detected: reserved
  bit 9-10: DEVSEL# timing: reserved
  bit 11: signaled target abort: reserved
  bit 12: received target abort (read only, write one to clear)
  bit 13: signaled master abort: reserved
  bit 14: signaled system error: reserved
  bit 15: detected parity error (write only, write one to clear)

7. Master Mode Enhanced IDE Controller

The VT82C570M has integrated a Master Mode IDE controller that supports dual channel/four device Enhanced-IDE bus (Enhanced-IDE specification such as mode-3 and mode-4 transfer rate and CD-ROM). The IDE controller has sixteen levels of double word prefetch and write buffers for the two channels to allow concurrent PCI bus and IDE drive operation. The data bus, control signals, write buffers and prefetch buffers are embedded in the VT82C570M and separated from those of the PCI and ISA bus so that performance is optimized and electrical loading is minimized. The command and recovery time of each IDE device can be individually programmed in units of PCI bus clock to achieve optimal speed of the device up to >22MB/s.

7.1. IDE Drive Interface Configuration

The IDE controller includes a variety of configuration registers for controlling the timing of individual IDE drives and different type of I/O access cycles. The format of configuration registers are compatible with the PCI configuration space specification and should be programmed by PCI configuration protocol.

Configuration register 4F/4E defined read/write command active pulse width and recovery time of non-1F0h port access for primary and secondary channels, respectively. One of sixteen selections, from one to sixteen PCI bus clocks, can be selected for each of the parameters. Register 4B/4Ah define the read and write access timing to the 1F0h port for the master and slave drives of the primary channel, respectively. Similarly, register 49/48h are used to control the master and slave drives of the secondary channel, respectively.

Register 4Ch determines the address setup time of for the 1F0h port access. For non-1F0h port access, the address setup time is always set to be 4 PCI bus cycles.

7.2. Prefetch and Post Write Buffers

The IDE controller supports sixteen levels of prefetch and write buffers for each of the two channels. These buffers provide concurrent operation for the IDE drives while the PCI bus may be performing other tasks.

Prefetch option may start after the following conditions are met:

1) the prefetch buffers are enabled;
2) the host has issued a Read_sector, or Read_multiple command into 1F7h command register; (Read-long in excluded)
3) a read to 1F0h data port is detected.

The IDE controller will read the subsequent 1F0h data after the first 1F0h data word is read from the IDE drive. Such a prefetch operation will be terminated when the 512th byte of the 1F0h data is read. Therefore, to avoid reading the incorrect data of the next sector which may be ready for host access, the prefetch operation does not continue through the sector boundary. The IDE controller also supports non-512th byte reading (e.g. 2352 for CD-ROM) according to the setting of internal registers (61/60h for the primary channel and 69/68h for the secondary channel).

If the post write buffer is enabled, the IDE controller will perform post-write operation for the host 1F0h write cycles. The CBE#3:0 status of the PCI bus command is latched to determine the active bytes for the drive interface. The IDE controller will terminate the bus cycle once the data is latched into the write buffer.

7.3. Operation Mode Selection

The IDE Controller can support both ATA compatible mode and PCI relocation mode for I/O port address configuration. Mode control is determined by PCI configuration register 42 bit <7..6>.

bit 7 0/1 ATA mode/PCI mode for 1st channel

bit 6 0/1 ATA Mode/PCI mode for 2nd channel

ATA Mode: The controller registers are hardwired to fixed IRQs and IO space as indicated in the following table:

Channel	Command Block Registers	Control Block Registers
Primary	1F0h - 1F7h	3F6h
Secondary	170h - 177h	376h

PCI Mode: The registers of the IDE channels are completely relocatable in IO space. Base Address registers at offset 10h, 14h, 18h and 1Ch in the VT82C576M's configuration space registers are used to map the IDE registers into IO space. Specific base address registers are used to map the different register blocks as defined in the following table:

Channel	Command Block Registers	Control Block Registers
Primary	Base Address at offset 10h	Base Address at offset 14h
Secondary	Base Address at offset 18h	Base Address at offset 1Ch

Base registers used to map Command Block registers must ask for 8 bytes of IO space. Base registers used to map Control Block registers must ask for 4 bytes of IO space. In this four byte allocation the byte at offset 02h is where the alternate status/device control byte is located. Other bytes in the four byte allocation (bytes at offsets 0,1 and 3) are unused.

7.4. Scatter and Gather and Bus Master Operation

The VT82C570M is compliant with the bus master programming interface for IDE ATA controllers SFF-8038 rev.1.0. Before the controller starts a master transfer, the IDE controller is given a pointer to a physical region descriptor (PRD) table (refer to Figure 2). This table contains some number of PRDs which describe areas of memory that are involved in the data transfer. Each PRD entry is 8 bytes in length. The first 4 bytes specify the byte address of a physical memory region. The next two bytes specify the count of the region in bytes. A value of zero indicates a 64KB size. Bit 7 of the last byte indicates the end of the table; bus master operation terminates when the last descriptor has been retired.

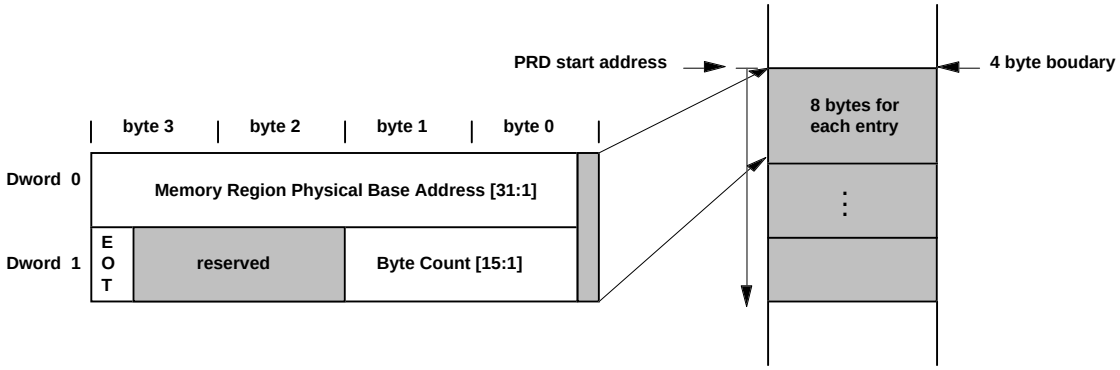

Figure 2: Physical Region Descriptor Table

The Scatter and Gather mechanism allows for larger transfer blocks to be scattered to or gathered from memory. This operation minimizes interrupts and CPU intervention. To initiate a bus master transfer between the system memory and the IDE device, the following steps are required:

1) Software prepares a PRD table in system memory.
2) Software determines the starting address on the PRD table by loading the PRD Table Pointer Register. The direction of the data transfer is determined by the Read/Write Control bit. Clear the Interrupt bit and Error bit in the Status register.
3) Software issues the appropriate DMA command to the IDE device.
4) Write "1" to the Start bit in the Bus Master IDE Command Register for the appropriate channel to engage bus master function.
5) The controller transfers data to/from memory responding to DMA requests from the IDE device.
6) At the end of the transfer the IDE device signals an interrupt.
7) In response to the interrupt, software resets the start/stop bit in the command register and reads the controller status and then the drive status to determine the success of the transfer.

8. Plug and Play Controller

The VT82C570M provides two plug and play ports for converting non plug and play devices into plug and play devices on the main board. Interrupts from the PCI bus (INTA# to INTD#), ISA bus and the plug and play ports can be directed to the individual channels of the two 8259A compatible interrupt controller under program control. Similarly, the DMA control signals from the ISA and the plug and play ports can be directed to the individual channels of the two 82C37A compatible DMA controller under program control. The configuration mechanism is compliant with the plug and play BIOS and the Microsoft Windows 95™ operating system. The VT82C570M also provides two general purpose programmable chip selects for reconfiguring IO address or for controlling non-intelligent IO devices. The following registers control the functionality of the plug and play ports:

RXFBh: Plug and play DRQ routing
- bit 7-6: reserved
- bit 5-3: PDRQ1 routing

  000: DRQ0 001: DRQ1 010: DRQ2 011: DRQ3
  100: reserved 101: DRQ5 110: DRQ6 111: DRQ7
- bit 2-0: PDRQ0 routing: same as PDRQ1 routing

RXFCh: PCI interrupt polarity
- bit 7-4: reserved
- bit 3 = 1/0: INTA# invert (edge)/non-invert (level)
- bit 2 = 1/0: INTB# invert (edge)/non-invert (level)

- bit 1 = 1/0: INTC# invert (edge)/non-invert (level)
- bit 0 = 1/0: INTD# invert (edge)/non-invert (level)

RXFDh: Plug and play IRQ routing
- bit 7-4: INTD# routing

0000: reserved	0001: IRQ1	0010: reserved	0011: IRQ3
0100: IRQ4	0101: IRQ5	0110: IRQ6	0111: IRQ7
1000: IRQ8	1001: IRQ9	1010: IRQ10	1011: IRQ11
1100: IRQ12	1101: reserved	1110: IRQ14	1111: IRQ15

- bit 3-0: PIRQ0 routing

RXFEh: PCI IRQ routing
- bit 7-4: INTA# routing: same as INTD# routing
- bit 3-0: INTB# routing: same as INTD# routing

RXFFh: PCI IRQ routing
- bit 7-4: INTC# routing: same as INTD# routing
- bit 3-0: PIRQ1 routing: same as INTD# routing

The routed IRQ and DRQ channels for the PCI and plug and play ports cannot be reused by the ISA bus (under plug and play BIOS or operating system control). The IRQ and DRQ channels of the two plug and play ports cannot overlap but the four PCI interrupts are level sensitive and thus can be shared.

9. ISA Bus Controller

The ISA bus state machine is included in the VT82C575M which controls and monitors all the ISA bus signals. To coordinate the bus operation with the VT82C576M PCI bus controller, the ISAREQ# signal is used. In particular, ISAREQ# is activated by the VT82C576M for CPU cycles that do not hit on-board memory and PCI devices to activate the ISA state machine. The ISA bus data is isolated form the CPU/cache and DRAM bus as a separate port form the VT82C577M data units.

The VT82C575M includes two 82C37A compatible DMA controllers, two 82C59A compatible interrupt controller, one 82C54 compatible timer and port B logic. The integrated DMA controller runs either at the same or half the speed of the ISA clock (bit 6 of RX10h). The DRQ and IRQ from the PCI bus, ISA bus and the two plug and play ports are steered and combined before delivering to the DMA and interrupt controllers. The integrated interrupt controller is extended to support level sensitive interrupts in addition to the 8259A compatible edge trigger interrupts (RX63-64h).

10. Power Management Unit

The integrated power management unit monitors IO events, interrupt, DMA and PCI master request signals to detect the status of system activity. Each event can be turned off or assigned to one of two event classes tracked by two independent idle timers. Two additional reloadable timers are provided for house-keeping or mode switching purposes. One of the timers can also be used to keep track the activity of specific peripheral devices. The system management interrupt (SMI) may be triggered by multiple sources including time-out of individual timers, occurrence of system activities, external input and software programming for flexible applications. The SMI routine checks the status and takes appropriate actions including clock speed switching (or throttling) and IO and power control. The power management unit is sophisticated enough to implement any power management model including the APM mechanism.

10.1. Idle Timers

The VT82C570M includes two idle timers to monitor primary and secondary system events. In addition to interrupts, the primary events are classified into the following eight categories (RX52h, RX53h):

- bit 7: keyboard access (IO port 60h),
- bit 6: serial port access (IO port 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, 2E8h-2EFh),
- bit 5: parallel port access (IO port 378h-37Fh, 278h-27Fh),
- bit 4: video access (IO port 3B0h-3DFh and memory A/B segments),
- bit 3: hard disk and floppy access (IO port 1F0h-1F7h and 3F5h),
- bit 2: IO port 100h-3FFh,
- bit 1: external input (Turbo pin scanned in through VT82C416),
- bit 0: DRQ/LREQ: DMA and local bus master requests.

Each category can be enabled as primary activities by setting the corresponding bit of RX52h to 1. Each occurrence of a primary activity reloads the idle timer with a value determined by bit 3-1 of RX59h.

000 - disable	001 - 1 sec	010 - 8 sec	011 - 32 sec
100 - 1 min.	101 - 8 min.	110 - 16 min.	111 - 32 min.

The cause of the timer reload is recorded in the corresponding bit of RX53h while the timer is reloaded. If no primary activity occurs during the time period, the idle timer will time out and the VT82C570M can be programmed to trigger an SMI to switch the system to a power down mode.

The idle timer distinguishes between two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary activities, the occurrence of a primary interrupt demands the system to return to its full processing capability. Secondary interrupts, however are typically used for house keeping tasks in the background and are unnoticeable to the user. The VT82C570M allows each channel of interrupt request to be declared as either primary or secondary in RX60h and RX61h.

- RX61h 1 - primary interrupt 0 - secondary interrupt

bit 7: IRQ15	bit 6: IRQ14	bit 5: IRQ13	bit 4: IRQ12
bit 3: IRQ11	bit 2: IRQ10	bit 1: IRQ9	bit 0: IRQ8

- RX60h

bit 7: IRQ7	bit 6: IRQ6	bit 5: IRQ5	bit 4: IRQ4
bit 3: IRQ3	bit 2: IRQ1	bit 1: IRQ0	

10.2. Handling of Secondary Events

If secondary IRQs occur and if the secondary events handler enable is defined in bit 1 of RX5fh (set to 1), then the secondary IRQ triggers the secondary events handler and services the interrupt request. After the interrupt is serviced (EOI, or "End of Interrupt") or after the secondary events counter runs out, the secondary events handler generates a SMI which will return the system back to the original mode. The EOI is defined in bit 1 of RX5Fh (set to 0) and the timer is found in bit 3-2 of RX5Fh:

00 - 2 ms	01 - 16 ms	10 - 64 ms	11 - EOI + .125ms

10.3. General Purpose and Peripheral Timers

The VT82C570M includes two reloadable timers to support various house keeping tasks. The two timers can be loaded by writing an 8-bit value into RX58h and RX67h, respectively. The time base for the two timers is determined by bit 7-6 of RX59h and bit 3-2 of RX66h, respectively:

00- disable	01 - 32.768Khz	10- 1 sec	11 - 1 min.

The time out of either timer can be programmed to trigger an SMI for proper system response. In addition to the house keeping function, the second reloadable timer also covers the functionality of a peripheral timer to monitor any combination of the following peripheral events (bit7-0 of RX65h):

- bit 7: keyboard access
- bit 6: serial port access
- bit 5: video access
- bit 4: hard disk and floppy access.
- bit 3: parallel port access
- bit 2: reserved
- bit 1: speaker access
- bit 0: reserved

10.4. System Management Interrupt

There are eight possible sources for triggering an SMI (RX54h and RX55h):

- bit 7: primary idle timer time-out,
- bit 6: general purpose timer (1st reloadable timer of 10.3) time-out,
- bit 5: primary activity occurrence,
- bit 4: primary interrupt occurrence,
- bit 3: external pin (Turbo) toggle,
- bit 2: DRQ/PREQ occurrence,
- bit 1: peripheral timer or secondary idle timer time-out,
- bit 0: software SMI.

The SMI action includes clock speed changing, clock throttling control and power/peripheral control by programming the following registers:

a. CPU clock frequency (bit 3-0 of RX56h)

0000 - 16Mhz	1000 - 8Mhz	0001 - 40Mhz	1001 - 20Mhz
0010 - 50Mhz	1010 - 25Mhz	0011 - 80Mhz	1011 - 40Mhz
0100 - 66Mhz	1100 - 33Mhz	0101 - 100Mhz	1101 - 50Mhz
0110 - 8Mhz	1110 - 4Mhz	0111 - 60Mhz	1111 - 30Mhz

The clock generator in the VT82C416 guarantees smooth frequency changes if the original and target frequencies fall in the same bank (same bit 3 of RX56h).

b. Clock throttling (bit 0 of RX5Bh): set the bit to 1 enables clock throttling. The STPCLK# period and duty cycle is controlled in RX02h.

- bit 4: STPCLK# throttling period: 1- 1.7ms * 16 0- 3.35us * 16,
- bit 3-0: duty cycle for STPCLK# 1/16 - 15/16.

c. Power/peripheral control (bit 7-4 of RX5Ah): More than ten general purpose output ports. Some of the ports are only available in notebook mode (eight CWE# pin reused as GPIO ports) and other ports need to be latched using external logic.

The setting of the above registers depends on the power management model and the cause of the SMI. Through this basic mechanism, the VT82C570M is capable of supporting many different power management models. For instance, BIOS routines are ready made to support the standard APM (Advanced Power Management protocols) for a cooperative power management among the application software, operating system, BIOS and the hardware. To illustrate the capability and flexibility of the VT82C570M, take a simple model that supports full-on, doze and sleep modes.

Bit 7 and bit 3 of RX54h are set and bit 5, 4 and 2 are not set during the full-on mode. Any occurrence of a primary activity reloads the idle timer without triggering an SMI so that no processing overhead is involved and the system performance is not degraded at all. The first SMI triggering happens when the idle timer is timed out or when the external pin is pushed by the user to force the

system into sleep. The SMI routine slows down the CPU clock and puts the system into the doze mode. Bit 7 of RX54h is now turned off and bit 2, 4, 5 are turned on to monitor the occurrence of a primary activity which will trigger an SMI to put the system back into the full-on mode.

By setting bit 6 of RX54h to 1, the time out of the general purpose timer will trigger an SMI which can switch the system from the doze mode to the sleep mode. If a primary activity occurs before the time-out of the general purpose timer, the system goes into the full-on mode and bit 6 of RX54h is turned off and the time-out of the general purpose timer will be ignored.

10.5. Conserve Mode

The conserve mode is a relatively straight-forward mode that monitor primary events and primary IRQs. The conserve mode is enabled by bit 5 of RX5Fh. The conserve mode generates no SMIs and it does not use a time base counter. Instead, the conserve mode offers two methods to conserve: clock throttling and clock division.

11. Multi-function X-Bus Peripherals

11.1. Scan Logic

The scan-in and scan-out logic uses the SCANIN and SCANOUT pins to communicate between the VT82C570M and the VT82C416. The signals to be scanned in to the VT82C570M from the VT82C416 through the SCANIN pin are indicated in Table 2:

scan order	signal name	scan order	signal name	scan order	signal name
0	DRQ0	8	IRQ4	16	IRQ14
1	DRQ1	9	IRQ5	17	IRQ15
2	DRQ2	10	IRQ6	18	IRQ1
3	DRQ3	11	IRQ7	19	IRQ12
4	DRQ5	12	IRQ#8	20	A20 Gate
5	DRQ6	13	IRQ9	21	KBRC#
6	DRQ7	14	IRQ10	22	Turbo
7	IRQ3	15	IRQ11	23	IOCHK#

Table 2. Scan-in Signal Sequence

On the other hand, the signals to be scanned out from the VT82C570M to the VT82C416 through the SCANOUT pin are listed in Table 3:

scan order	signal name	scan order	signal name
0	ClkSel0	5	MouseLock
1	ClkSel1	6	RP13
2	ClkSel2	7	RP14
3	ClkSel3	8	RP15
4	RPS2	9	RP16

Table 3. Scan-out Signal Sequence

Clksel0-3 reflect bit 3-0 of RX56h for the CCLK frequency. RP13-16 are the jumper setting of MA0-3 at power on reset. These four bits are transmitted to the keyboard controller inside the VT82C416. These four bits can also be read from bit 3-0 of RX64h.

There are twenty-four scan-in signals and ten scan-out signals. Both the VT82C570M and the VT82C416 use both edges of the OSC clock as the scan clock. After system reset, the two chips are initialized to the same scan order and the communication between the two chips runs forever.

11.2. The XD to SD buffer:

The available external pins are XD0-7, SD0-7, SD8-15, SDIR, SDOE# and XDIR. If the XDIR pin is high, the data flows from the SD0-7 to the XD0-7 bus. If the SDIR pin is high, the data flows from the XD0-7 to SD8-15. If the SDIR pin is low, then the data flows from SD8-15 to XD0-7. If SDOE# is low, it enables the internal data transfer between XD0-7 to the SD8-15 buffer. If the XDIR pin is low, the data flows from the XD0-7 to the SD0-7 bus. During the internal keyboard controller and RTC read cycles, the XD0-7 bus is driven by the VT82C416 independent of the XDIR value. If the XDIR pin is low, the data is also driven to the SD0-7 bus; otherwise, the SD0-7 bus is not driven by the chip. During the internal keyboard controller and RTC write cycles of even address bytes, the XDIR pin must be driven low for the XD0-7 bus to write into the internal peripherals write cycle of odd address byte, the SDIR and XDIR pin must be driven low for transferring SD8-15 to SD0-7.

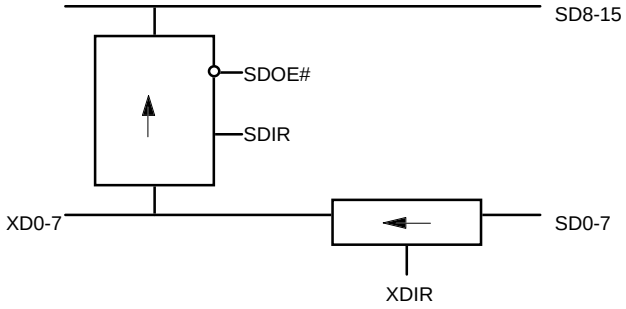

Figure 3. The XD to SD Block Diagram

11.3. Multi-clock generator:

The available external pins are RTCX1, RTCX2, CPUClk, 24Mhz, and OSC. The four clock selection pins are scanned in from the core logic chip through the SCANOUT pin. Note that the clock frequency changes smoothly if the original and target frequencies fall in the same bank (same Clksel3 of Table 3). The initial value of Clksel3 (before the scan circuitry is active) is determined by the condition of XD6 at reset.

The internal clock generator enabling is controlled by the condition of XD7 at reset. OSC is used as an output if the internal clock generator is enabled and as an input if disabled.

11.4. Keyboard controller

The available external pins are KBCS#, IOR#, IOW#, KBData, KBClk, MouseData, MouseClk, KBTurbo, KBLock and SA2. The IRQ1, IRQ12, KBRC# and A20Gate outputs from the internal keyboard controller are scanned in to the core logic chip through the SCANIN pin. The enabling of the internal keyboard controller is controlled by the condition of XD3 at reset (high to enable and low to disable). If the internal keyboard controller is disabled, then the KBData, KBClk, MouseData and MouseClk pins are not used; these pins are redefined to be KBRC#, A20Gate, IRQ1 and IRQ12 inputs from the external keyboard controller to be scanned into the core logic through the SCANIN pin.

11.5. Real time clock

The available external pins are RTCAS, RTCDS and VBat. The RTCRW pin is eliminated because the information is carried in the IOR# and IOW#. The IRQ#8 output from the internal real time clock is scanned in to the core logic through the SCANIN pin. The enabling of the internal real time clock is controlled by the condition of XD6 at reset (low for enable and high for disable). If the internal real time clock is disabled, the RTCDS pin is not used; this pin is redefined to be the IRQ#8 pin of the external real time clock to be scanned into the core logic through the SCANIN pin.

11.6. General Purpose Chipselect

Two programmable chipselect (A and B) are available in the VT82C570M. The addresses may be programmed at RX9Ch <7:0> and RX9Dh <1:0> for chipselect A and at RX9Eh <7:0> and RX9Dh <1:0> for chipselect B. The mask bits of RX9Dh <7:2> for channel A and RX9Fh <7:2> may define the address range that generate a chipselect.

11.7. Programmable Output Port

The VT82C570M provides eight general purpose output ports to control external devices through PC0-7. These pins are multi-function pins shared with MA <4:11>. When the output is not at a DRAM cycle, the output will be the value of RX7Eh <0:7> and it should be latched into the external device by PCWE#. Moreover, if the chipset is configured as the notebook mode (XD2 sampled low at reset), then additional eight output ports and eight general purpose input and output ports are available without any external logic (controlled by RX5A, 7B, 7C and 7Fh). The general purpose input and output ports can be programmed to support multiple SMI triggering conditions (RX68, 69, 6Ah).

12. Configuration Registers

Every internal register in the VT82C570M is assigned an 8-bit index. Two IO ports are used to access the register set: the index port at address A8 and the data port at A9 for register 00 to 9F and index A8 and data AC for register FB to FF. To access a register, first write the index into the index port and then read or write the data through the data port. For detail description of the configuration register, refer to application note "Configuration Registers for the VT82C570M."

The VT82C570M also supports PCI configuration as is presented in section 6.4. Other than mandatory header field required by the PCI specification, all PCI related configuration (RX80h-RXFFh) can be exercised through the standard PCI configuration mechanism.

The initial configuration of the VT82C570M chip set depends on the strapping condition of several bits of the XD bus during power on reset as indicated in Table 4.

VT82C575M Pins Only				
Signal	pin#	sampled low at reset	sample high at reset	pin definition affected
XD2	161	select notebook mode	select desktop mode	7-11, 31-32, 88-95, 189-190
VT82C416 Pins Only				
Signal	pin #	sampled low at reset	sample high at reset	pin definition affected
XD3	80	internal keyboard controller disabled	internal keyboard controller enabled	10, 11, 12, 13
XD4	79	N/A	strapped high	no
XD5	78	strapped low	N/A	no
XD7	76	internal clock generator and RTC enabled	internal clock generator disabled	69, 2
XD7 Sampled Low at Reset				
XD6	77	CPU clock freq. selection Clksel=1 at reset	CPU clock freq. selection S3=0 at reset	no
XD7 Sampled High at Reset				
XD6	77	internal real time clock enabled	internal real time clock disabled	2

Table 4. Configuration Options for the VT82C570M

VT82C575M PIN DESCRIPTION

Signal Name	Pin No.	3.3/5v	I/O	Signal Description
CLOCK CONTROL				
CCLK	79	VDD_CPU	I	CPU clock input from the VT82C416.
PCLK	121	5v	I	Clock input of half the CCLK frequency (from the VT82C416).
CLKSEL0-3/ RAS#0-3	118-115	5v	B	Multi-function pin: 1. At power on reset: CCLK frequency selection. 2. After power on reset: DRAM RAS# control.
SYSCLK	181	5v	O	ISA bus clock.
OSC	120	5v	I	14.318Mhz clock input from the VT82C416. This clock is used for timer control and scan-in and scan-out logic sequencing.
RESET CONTROL				
PWRGOOD	183	5v	I	System power good signal generated from the power supply.
RESET#	184	5v	O	Active low reset signal for the ISA system.
CPURESET	73	VDD_CPU	O	Reset for the CPU.
INIT	74	VDD_CPU	O	soft reset for the CPU.
CPU INTERFACE				
ADS#	2	VDD_CPU	I	Address Strobe.
MIO#	3	VDD_CPU	I	Memory/IO status.
WR#	5	VDD_CPU	B	Write/read status.
DC#	4	VDD_CPU	I	D/C# status indicator.
BE#0-7	87-80	VDD_CPU	B	byte enable.
CA3-31	66-62, 59-52, 23-16, 14-11,9-6	VDD_CPU	B	CPU bus address. If XD2 if sampled low at reset, CA27-30 is redefined as GPIO3-0 (general purpose IO).
A20M#	75	VDD_CPU	B	A20 mask output to the CPU.
BRDY#	76	VDD_CPU	O	Ready output to the CPU.
EADS#	71	VDD_CPU	O	External ADS output to the CPU to force an internal snoop cycle.
KEN#	68	VDD_CPU	O	Cache enable output to the CPU to indicate whether the current cycle is cacheable.
HITM#	67	VDD_CPU	I	Input from the CPU to indicate the snoop cycle hits a dirty internal cache line.
CACHE#	69	VDD_CPU	I	burst cycle indicator.
HOLD	29	VDD_CPU	O	Hold request to the CPU.
HLDA	28	VDD_CPU	I	Hold acknowledge from the CPU.
STPCLK#	26	VDD_CPU	O	STPCLK# output to the CPU to switch clock speed or to reduce the power consumption.
SMI#	24	VDD_CPU	B	SMI output to the CPU.
SMIACT#	25	VDD_CPU	I	SMI active input from the CPU.

FERR#	50	VDD_CPU	I	Input from pin FERR# of the CPU.
IGNNE#	51	VDD_CPU	O	Output to pin IGNNE# of the CPU.
INTR	27	VDD_CPU	O	Interrupt request to the CPU.
NMI	72	VDD_CPU	O	Non-maskable interrupt request to the CPU.
NA#	70	VDD_CPU	O	Input from pin NA# of the CPU
BOFF#	98	VDD_CPU	O	Output to pin BOFF# of the CPU
CACHE CONTROL				
CBOE#0-1	47, 46	VDD_CPU	O	Cache SRAM output enable for each bank.
CWE#0-1/ BWE#0-1	45, 44	VDD_CPU	O	Multi-function pins: 1. bit 5 of RX49h is 0: cache SRAM write enable for each bank. 2. bit 5 of RX49h is 1: cache SRAM byte write enable.
BWE#2-7/ GPO0-5	88-93	VDD_CPU	O	Multi-function pins: 1. XD2 sampled high at reset: cache SRAM byte write enable. 2. XD2 sampled low at reset: direct output ports.
CCS#1-0/ GPIO4-5	94,95	VDD_CPU	B	Multi-function pins: 1. XD2 sampled high at reset: cache SRAM chip select for each bank. 2. XD2 sampled low at reset: general purpose IO ports.
ADSC#, ADV#/ A4SEL0-1	49, 48	VDD_CPU	O	Multi-function pin: 1. Burst synchronous SRAM: ADSC# and ADV# control for the SRAM. 2. Two bank of asynchronous SRAMs: address A4 for each bank to allow bank interleaving. 2. One bank of asynchronous SRAM: address A3 and A4 for the SRAM.
CALE/ CE#1	106	VDD_CPU	O	Multi-function pin: 1. Asynchronous SRAM: CPU address latch enable. 2. Burst synchronous SRAM: Cache enable #1.
TA0-9	41-39, 37-31	VDD_CPU	B	Cache tag. If XD2 is sampled low at reset, TA8-9 is redefined as GPIO6-7.
ALT	30	VDD_CPU	B	Cache alter bit.
TAGWE#	42	VDD_CPU	O	Tag SRAM write enable.
DRAM CONTROL				
MA0-3/ P13-16	134-137	5v	B	Multi-function pin: 1. DRAM cycle: DRAM address 0-3. 2. Power-on reset: input port P13-P16 for the keyboard controller inside the VT82C416.
MA4-11/ PC0-7	138-141, 143-146	5v	O	Multi-function pin: 1. DRAM cycle: DRAM address 4-11. 2. Other cycle: power/peripheral control output to be latched by external latches (controlled by PCWE#).

RAS#0-3/ CLKSEL0-3	118-115	5v	O	Multi-function pin: 1. After power on reset: row address strobe for each bank (pair) of on-board DRAMs. For double bank pairs, BHSEL# and BLSEL# signals are used to distinguish between the two banks. 2. At power on reset: frequency select for the clock generator.
CAS#0-7	125-132	5v	O	Column address strobe for each byte of DRAMs.
LWE#	107	5v	O	Low DWORD write enable
MWE#	148	5v	O	DRAM write enable.
BLSEL#, BHSEL#/ DPC0-1	189,190	5v	O	Multi-function pins: 1. XD2 sampled high at reset: DRAM high/low bank select for double-side DRAMs. 2. XD2 sampled low at reset: Direct power control pins.
ON-BOARD PERIPHERALS				
XD0-7	163-156	5v	B	8-bit data bus for communication between the VT82C570M and on-board peripherals.
XDIR	179	5v	O	Directional control for XD0-7 to SD0-7 external buffer.
SDIR	168	5v	O	Directional control for XD0-7 to SD8-15 buffer.
SDOE#	169	5v	O	Output enable for the XD0-7 to SD8-15 external buffer.
ROMCS#	155	5v	B	ROM chip select.
SPEAKER	186	5v	O	Speaker output.
PCWE#	113	5v	O	Write enable for PC0-3 latches.
VT82C576M INTERFACE				
ISAREQ#	150	5v	I	ISA bus cycle indicator between the VT82C575M and VT82C576M.
PRDY#	99	5v	B	Ready indicator from the VT82C576M.
PBLAST#	110	5v	B	Burst last indicator from the VT82C576M.
PREQ#	108	5v	I	Input from the PCI bus controller to request the CPU and DRAM bus.
PGNT#	109	5v	O	Output to the PCI bus controller to grant the bus ownership.
PA2	105	5v	B	Fast address A2.
PBE#0-3	104-101	5v	B	Byte enable for the data link.
PBOFF#	100	5v	O	Backoff request from the PCI bus controller.
WBACK#	172	5v	O	Cache write back indicator
VT82C416 INTERFACE				
SCANIN	187	5v	I	Scan input from the VT82C416.
SCANOUT	188	5v	O	Scan output to the VT82C416.
REGCS#	171	5v	O	Register select for the VT82C416.
KBCS#	154	5v	O	Keyboard controller chip select for IO cycles.
RTCAS	152	5v	O	Address strobe for the real time clock.
RTCCS#	153	5v	O	Data select for the real time clock.
DACEN	185	5v	O	DACK# control to the VT82C416.
ISA BUS CONTROL				
SA0-7	199-196, 194-191	5v	B	System address for the ISA bus.

SBHE#	166	5v	B	System byte high enable.
IOR#	206	5v	B	ISA bus IO read command.
IOW#	207	5v	B	ISA bus IO write command.
MEMR#	202	5v	B	ISA bus memory read command.
MEMW#	203	5v	B	ISA bus memory write command.
SMEMR#	204	5v	B	ISA bus memory read below 1MB address range.
SMEMW#	205	5v	B	ISA bus memory write below 1MB address range.
BALE	167	5v	O	Buffered address latch enable.
IO16#	174	5v	I	IO cycle 16-bit select indicator.
MS16#	175	5v	I	Memory cycle 16-bit select indicator.
MASTER16#	173	5v	I	Master cycle indicator.
IOCHRDY#	176	5v	I	IO channel ready.
REFRESH#	178	5v	B	System DRAM refresh control.
AEN	177	5v	O	Address enable indicator for DMA cycles.
TC	180	5v	O	DMA terminal count.
VT82C577M CONTROL				
MDIR	122	5v	O	Direction control for CD to MD data buffers.
MDOE#	123	5v	O	Output enable for CD to MD data buffers.
MDLE	124	5v	O	Latch enable for CD to MD data buffers.
FIFOC#	208	5v	O	The 4-level write-buffer and Burst EDO FIFO controller connects to VT82C577M pin #23.
CBREF	111	5v	O	CAS before RAS refresh indicator.
CDSEL	151	5v	O	Data select during 64-bit to 32-bit conversion.
PSEL#	112	5v	O	Data Link bus select;
BA2	170	5v	O	Bus address 2, for CD to SD conversion
General Purpose IO ports				
GPIO0-7	7-11, 94, 95, 32, 31	VDD_CPU	B	Available only if XD2 is sampled low at reset (notebook mode).
GPO0-5	88-93	VDD_CPU	O	Available only if XD2 is sampled low at reset.
DPC0-1	189,190	5v	O	Available only if XD2 is sampled low at reset.
PC0-7/ MA4-11	138-141, 143-146	5v	O	Multi-function pin: 1. No-DRAM cycle: power/peripheral control output to be latched by external latches (controlled by PCWE#). 2. DRAM cycle: DRAM address.
POWER AND GROUND				
VDD_5v	114, 147, 165, 201	5v	I	Power supply of 4.5v to 5.5v
VDD_CPU	10, 43, 61, 78, 97	3.3/5v	I	Power supply for the CPU bus.
VSS	1, 15, 38, 60, 77, 96, 119, 133, 142, 164, 182, 195, 200	0v	I	Ground

VT82C575M PIN OUT IN NUMERICAL ORDER

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	VSS	53	CA14	105	PA2	157	XD6
2	ADS#	54	CA13	106	CALE/CE1#	158	XD5
3	MIO#	55	CA12	107	LWE#	159	XD4
4	DC#	56	CA11	108	PREQ#	160	XD3
5	WR#	57	CA10	109	PGNT#	161	XD2
6	CA31	58	CA9	110	PBLAST#	162	XD1
7	CA30	59	CA8	111	CBREF	163	XD0
8	CA29	60	VSS	112	PSEL#	164	VSS
9	CA28	61	VDD_CPU	113	PCWE#	165	VDD_5v
10	VDD_CPU	62	CA7	114	VDD_5v	166	SBHE#
11	CA27	63	CA6	115	RAS#3	167	BALE
12	CA26	64	CA5	116	RAS#2	168	SDIR
13	CA25	65	CA4	117	RAS#1	169	SDOE#
14	CA24	66	CA3	118	RAS#0	170	BA2
15	VSS	67	HITM#	119	VSS	171	REGCS#
16	CA23	68	KEN#	120	OSC	172	WBACK#
17	CA22	69	CACHE#	121	PCLK	173	MASTER16#
18	CA21	70	NA#	122	MDIR	174	IO16#
19	CA20	71	EADS#	123	MDOE#	175	MS16#
20	CA19	72	NMI	124	MDLE	176	IOCHRDY#
21	CA18	73	CPURESET	125	CAS#0	177	AEN
22	CA17	74	INIT	126	CAS#1	178	REFRESH#
23	CA16	75	A20M#	127	CAS#2	179	XDIR
24	SMI#	76	BRDY#	128	CAS#3	180	TC
25	SMIACT#	77	VSS	129	CAS#4	181	SYSCLK
26	STPCLK#	78	VDD_CPU	130	CAS#5	182	VSS
27	INTR	79	CCLK	131	CAS#6	183	PWRGOOD
28	HLDA	80	BE#7	132	CAS#7	184	RESET#
29	HOLD	81	BE#6	133	VSS	185	DACEN
30	ALT	82	BE#5	134	MA0	186	SPEAKER
31	TA9	83	BE#4	135	MA1	187	SCANIN
32	TA8	84	BE#3	136	MA2	188	SCANOUT
33	TA7	85	BE#2	137	MA3	189	BLSEL#
34	TA6	86	BE#1	138	MA4	190	BHSEL#
35	TA5	87	BE#0	139	MA5	191	SA7
36	TA4	88	BWE#2	140	MA6	192	SA6
37	TA3	89	BWE#3	141	MA7	193	SA5
38	VSS	90	BWE#4	142	VSS	194	SA4
39	TA2	91	BWE#5	143	MA8	195	VSS
40	TA1	92	BWE#6	144	MA9	196	SA3
41	TA0	93	BWE#7	145	MA10	197	SA2
42	TAGWE#	94	CCS#1	146	MA11	198	SA1
43	VDD_CPU	95	CCS#0	147	VDD_5v	199	SA0
44	BWE_1#	96	VSS	148	MWE#	200	VSS
45	BWE_0#	97	VDD_CPU	149	NC	201	VDD_5v
46	CBOE#1	98	BOFF#	150	ISAREQ#	202	MEMR#
47	CBOE#0	99	PRDY#	151	CDSEL	203	MEMW#
48	A4SEL1/ADV#	100	PBOFF#	152	RTCAS	204	SMEMR#
49	A4SEL0/ADSC#	101	PBE#3	153	RTCCS#	205	SMEMW#
50	FERR#	102	PBE#2	154	KBCS#	206	IOR#
51	IGNNE#	103	PBE#1	155	ROMCS#	207	IOW#
52	CA15	104	PBE#0	156	XD7	208	FIFOC#

VT82C575M PIN DIAGRAM

VT82C576M PIN DESCRIPTION

Signal Name	Pin No.	3.3/5v	I/O	Signal Description
PCI Bus Interface				
PCLK	84	5v	O	PCI bus clock output
FRAME#	193	5v	B	PCI cycle frame.
AD0-31	56-59, 62-65, 92-95, 98-101,128-131, 133-136, 160-163, 166-169	5v	B	Multiplexed PCI address and data
C/BE#0-3	34-37	5v	B	Multiplexed PCI command and byte enable
IRDY#	194	5v	B	Initiator ready.
TRDY#	39	5v	B	Target ready.
STOP#	42	5v	B	Stop signal.
DEVSEL#	41	5v	B	Device select.
PAR	195	5v	B	Data parity.
PERR#	32	5v	B	Parity error.
LOCK#	40	5v	B	Lock signal.
REQ#0-3	115-118	5v	I	PCI bus request from other PCI masters.
GNT#0-3	172-175	5v	O	PCI bus grant to other PCI masters.
CPU Interface				
ADS#	11	VDD_CPU	B	Address strobe.
MIO#	12	VDD_CPU	B	Memory/IO indicator.
WR#	13	VDD_CPU	B	Write/read indicator.
DC#	14	VDD_CPU	B	Data/control indicator.
CA3-31	202-208,2-8, 16-23, 25-31	VDD_CPU	B	CPU address.
BRDY#	9	VDD_CPU	B	Ready output to the CPU.
VT82C575M Interface				
PA2	171	5v	B	Fast address A2.
PBE#0-3	85-88	5v	B	Byte enable of the data link.
ISAREQ#	178	5v	O	ISA bus cycle indicator between the VT82C575M and the VT82C576M.
PRDY#	177	5v	O	Ready indicator to the VT82C575M.
PREQ#	176	5v	O	CPU/DRAM bus request to the VT82C575M.
PGNT#	198	5v	I	bus grant from the VT82C575M.
WBACK#	89	5v	I	Write snoop control from the VT82C575M.
PBOFF#	33	5v	O	Backoff request to the VT82C575M.
PBLAST#	91	5v	B	Burst last indicator to the VT82C575M.
VT82C577M Interface				
BCD0-31	44-51,66-73, 106-113, 120-127	5v	B	Buffered and latched (pipelined) CPU data.

Enhanced IDE Interface				
DD0-15	52-55,74-77, 79-82, 102-105	5v	B	IDE drive data bus.
DCS1#A	148	5v	O	Drive chip select 1 for the IDE channel A.
DCS3#A	149	5v	O	Drive chip select 3 for the IDE channel A.
DCS1#B	150	5v	O	Drive chip select 1 for the IDE channel B.
DCS3#B	151	5v	O	Drive chip select 3 for the IDE channel B.
DIOR#A	155	5v	O	DIOR command strobe for IDE channel A.
DIOR#B	158	5v	O	DIOR command strobe for IDE channel B.
DIOW#A	156	5v	O	DIOW command strobe for IDE channel A.
DIOW#B	159	5v	O	DIOW command strobe for IDE channel B.
DA0-2	152-154	5v	O	IDE drive address.
DRDY#	157	5v	I	IDE drive ready indicator.
DREQA	189	5v	I	DMA request from IDE channel A.
DREQB	190	5v	I	DMA request from IDE channel B.
DACKA#	191	5v	O	DMA acknowledge to IDE channel A.
DACKB#	192	5v	O	DMA acknowledge to IDE channel B.
System Interface				
CCLK	199	5v	I	CPU clock
RESET#	196	5v	I	active low reset input from the VT82C575M.
IOCHK#/ NMI	90	5v	O	IO channel check (bit 5 of RX93h = 0) or NMI (bit 5 of RX93h=1) to signify the parity or system error at the PCI bus.
SA8-23	138-141, 143-146, 179-182, 184-187	5v	B	ISA address
MASTER16#	170	5v	I	Master cycle indicator to control the address buffer direction.
PCS#0-1	188, 137	5v	O	Two general purpose chip selects.
Power and Ground				
VDD	43, 61, 97, 114, 147, 165	5v	I	power supply of 4.5 to 5.5V.
VSS	1, 15, 24, 38, 60, 78, 83, 96, 119, 132, 142, 164, 183, 197,200	0v	I	the ground
VDD_CPU	10, 201	3.3/5v	I	CPU voltage, 3 or 5 volts

VT82C576M PIN OUT IN NUMERICAL ORDER

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	VSS	53	DD1	105	DD15	157	DRDY#
2	CA10	54	DD2	106	BCD16	158	DIOR#B
3	CA11	55	DD3	107	BCD17	159	DIOW#B
4	CA12	56	AD0	108	BCD18	160	AD24
5	CA13	57	AD1	109	BCD19	161	AD25
6	CA14	58	AD2	110	BCD20	162	AD26
7	CA15	59	AD3	111	BCD21	163	AD27
8	CA16	60	VSS	112	BCD22	164	VSS
9	BRDY#	61	VDD	113	BCD23	165	VDD
10	VDD_CPU	62	AD4	114	VDD	166	AD28
11	ADS#	63	AD5	115	REQ#0	167	AD29
12	MIO#	64	AD6	116	REQ#1	168	AD30
13	WR#	65	AD7	117	REQ#2	169	AD31
14	DC#	66	BCD8	118	REQ#3	170	MASTER16#
15	VSS	67	BCD9	119	VSS	171	PA2
16	CA17	68	BCD10	120	BCD24	172	GNT#0
17	CA18	69	BCD11	121	BCD25	173	GNT#1
18	CA19	70	BCD12	122	BCD26	174	GNT#2
19	CA20	71	BCD13	123	BCD27	175	GNT#3
20	CA21	72	BCD14	124	BCD28	176	PREQ#
21	CA22	73	BCD15	125	BCD29	177	PRDY#
22	CA23	74	DD4	126	BCD30	178	ISAREQ#
23	CA24	75	DD5	127	BCD31	179	SA16
24	VSS	76	DD6	128	AD16	180	SA17
25	CA25	77	DD7	129	AD17	181	SA18
26	CA26	78	VSS	130	AD18	182	SA19
27	CA27	79	DD8	131	AD19	183	VSS
28	CA28	80	DD9	132	VSS	184	SA20
29	CA29	81	DD10	133	AD20	185	SA21
30	CA30	82	DD11	134	AD21	186	SA22
31	CA31	83	VSS	135	AD22	187	SA23
32	PERR#	84	PCLK	136	AD23	188	PCS#0
33	PBOFF#	85	PBE#0	137	PCS#1	189	DREQA
34	C/BE#0	86	PBE#1	138	SA8	190	DREQB
35	C/BE#1	87	PBE#2	139	SA9	191	DACKA#
36	C/BE#2	88	PBE#3	140	SA10	192	DACKB#
37	C/BE#3	89	WBACK#	141	SA11	193	FRAME#
38	VSS	90	IOCHK#/NMI	142	VSS	194	IRDY#
39	TRDY#	91	PBLAST#	143	SA12	195	PAR
40	LOCK#	92	AD8	144	SA13	196	RESET#
41	DEVSEL#	93	AD9	145	SA14	197	VSS
42	STOP#	94	AD10	146	SA15	198	PGNT#
43	VDD	95	AD11	147	VDD	199	CCLK
44	BCD0	96	VSS	148	DCS1#A	200	VSS
45	BCD1	97	VDD	149	DCS3#A	201	VDD_CPU
46	BCD2	98	AD12	150	DCS1#B	202	CA3
47	BCD3	99	AD13	151	DCS3#B	203	CA4
48	BCD4	100	AD14	152	DA0	204	CA5
49	BCD5	101	AD15	153	DA1	205	CA6
50	BCD6	102	DD12	154	DA2	206	CA7
51	BCD7	103	DD13	155	DIOR#	207	CA8
52	DD0	104	DD14	156	DIOW#	208	CA9

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VT82C576M PIN DIAGRAM

VT82C577M PIN DESCRIPTION

Signal Name	Pin No.	3.3/5v	I/O	Signal Description
CPU Data Port				
CD0-7/ CD8-15	82-89	VDD_CPU	B	CD0-7 for VT82C577M#1 and CD8-15 for VT82C577M#2.
CD16-23/ CD24-31	92-99	VDD_CPU	B	CD16-23 for VT82C577M#1 and CD24-31 for VT82C577M#2.
CD32-39/ CD40-47	57-64	VDD_CPU	B	CD32-39 for VT82C577M#1 and CD40-47 for VT82C577M#2.
CD48-55/ CD56-63	67-74	VDD_CPU	B	CD48-55 for VT82C577M#1 and CD56-63 for VT82C577M#2.
DRAM/PCI Data Port				
MD0-7/ MD8-15	29-32, 34-37	5v	B	MD0-7 for VT82C577M#1 and MD8-15 for VT82C577M#2.
MD16-23/ MD24-31	38, 46-50, 52-53	5v	B	MD16-23 for VT82C577M#1 and MD24-31 for VT82C577M#2.
MD32-39/ MD40-47	54-56, 75-79	5v	B	MD32-39 for VT82C577M#1 and MD40-47 for VT82C577M#2.
MD48-55/ MD56-63	81, 100, 13, 14, 17-20	5v	B	MD48-55 for VT82C577M#1 and MD56-63 for VT82C577M#2.
ISA Data Port				
XD0-7/ SD8-15	42-45, 6-9	5v	B	XD0-7 for VT82C577M#1 and SD8-15 for VT82C577M#2.
Clock and Misc. Control				
CCLK	39	5v	I	CPU clock.
PCLK	2	5v	I	Clock at half the CPU frequency.
PSEL#	21	5v	I	Select for VT82C576M.
SA0-1, BCA2	3-5	5v	I	SA0-2 for CD to SD data conversion.
MDIR	10	5v	I	CD to MD buffer direction control.
MDOE#	11	5v	I	CD to MD buffer output enable.
MDLE	12	5v	I	CD to MD buffer latch enable.
CDSEL	28	5v	I	CD to MD data select (64 bit to 32 bit conversion).
DBSEL	27	5v	I	Dip-switch: pull-up for odd VTT82C577M, pull-down for even VT82C577M
FIFOC#	23	5v	I	Connects to FIFOC# of VT82C575M pin #208
CBREF	26	5v	I	CAS before RAS refresh indicator from VT82C575M.
CAS#	22	5v	I	Connects to DRAM CAS signal. It is sync. with DRAM CAS. It is recommended to maintain same skew among the 8 CAS of DRAM for pipeline burst EDO operation.
Power and Ground				
VDD_5v	16, 41	5v	I	Power supply of 4.5 to 5.5V.
VDD_CPU	65, 91	3.3/5v	I	Power supply for the CPU bus (3.3v or 5v).
VSS	1, 15, 33, 40, 51, 66, 80,90	0v	I	Ground

VT82C577M PIN OUT IN NUMERICAL ORDER

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	31	MD2	51	VSS	81	MD48
2	PCLK	32	MD3	52	MD22	82	CD0
3	SA0	33	VSS	53	MD23	83	CD1
4	SA1	34	MD4	54	MD32	84	CD2
5	BCA2	35	MD5	55	MD33	85	CD3
6	XD4	36	MD6	56	MD34	86	CD4
7	XD5	37	MD7	57	CD32	87	CD5
8	XD6	38	MD16	58	CD33	88	CD6
9	XD7	39	CCLK	59	CD34	89	CD7
10	MDIR	40	VSS	60	CD35	90	VSS
11	MDOE#	41	VDD_5v	61	CD36	91	VDD_CPU
12	MDLE	42	XD0	62	CD37	92	CD16
13	MD50	43	XD1	63	CD38	93	CD17
14	MD51	44	XD2	64	CD39	94	CD18
15	VSS	45	XD3	65	VDD_CPU	95	CD19
16	VDD_5v	46	MD17	66	VSS	96	CD20
17	MD52	47	MD18	67	CD48	97	CD21
18	MD53	48	MD19	68	CD49	98	CD22
19	MD54	49	MD20	69	CD50	99	CD23
20	MD55	50	MD21	70	CD51	100	MD49
21	PSEL#			71	CD52		
22	CAS#			72	CD53		
23	FIFOC#			73	CD54		
24	NC			74	CD55		
25	NC			75	MD35		
26	CBREF			76	MD36		
27	DBSEL			77	MD37		
28	CDSEL			78	MD38		
29	MD0			79	MD39		
30	MD1			80	VSS		

VT82C577M PIN DIAGRAM

VT82C416 PIN DESCRIPTION

Signal Name	Pin No.	3/5v	I/O	Signal Description
Clock Generator				
RTCX1	99	5v	I	32.768Khz crystal or oscillator input
RTCX2	100	5v	O	the other end of the 32.768Khz crystal. Left unconnected if an oscillator is used.
PD	95	5v	O	phase detector for the clock generator. A 1000pF capacitor to ground should be connected from this pin to form the loop filter.
OSC	69	5v	B	multi-function pin: 1. 14.318Mhz OSC output: internal clock generator is enabled (XD7 sampled low during reset). 2. 14.318Mhz OSC input: internal clock generator is disabled (XD7 sampled high during reset).
CLK	93	5v	O	CPU clock output with one of sixteen available frequencies.
CLK_2	94	5v	O	Clock with half the frequency of CLK.
24Mhz	38	5v	O	24Mhz clock output.
Keyboard Controller				
KBCS#/ CALE	3	5v	I	Keyboard controller chip select for IO cycles. CPU address latch enable for memory cycles.
KBLOCK	8	5v	I	keyboard lock.
KBTURBO	9	5v	B	keyboard turbo indicator.
SA2	63	5v	B	SA2 to select between keyboard command and data.
The definition of the following four pins depends on if the internal keyboard controller is enabled. - enabled: XD3 is sampled high during reset. - disabled: XD3 is sampled low during reset In this case, the four pins are inputs for the scan-in logic for the core logic chip.				
KBCLK/ A20Gate	10	5v	B	multi-function pin: 1. clock to the keyboard interface: internal KBC enabled. 2. A20 gate input: internal KBC disabled.
KBDATA/ KBRC#	11	5v	B	multi-function pin: 1. keyboard data: internal KBC enabled. 2. keyboard warm reset input: internal KBC disabled.
MSCLK/ IRQ1	12	5v	B	multi-function pin: 1. mouse clock: internal KBC enabled. 2. IRQ1: internal KBC disabled.
MSDATA/ IRQ12	13	5v	B	multi-function pin: 1. mouse data: internal KBC enabled. 2. IRQ12: internal KBC disabled.
Real Time Clock				
RTCAS	90	5v	I	RTC address strobe.

RTCCS#/ IRQ#8	2	5v	I	multi-function pin: 1. RTC data select: internal RTC enabled (XD6 or XD7 low at reset). 2. IRQ#8: internal RTC disabled (XD7 and XD6 high at reset).
VBAT	97	5v	I	RTC battery.
ISA Bus Signals				
XD0-7	83-76	5v	B	ISA utility XD bus.
SD0-15	88-84, 55, 54, 46-42, 17-14	5v	B	ISA data bus.
IOR#	91	5v	I	ISA bus IO read strobe.
IOW#	92	5v	I	ISA bus IO write strobe.
IOCHK#	34	5v	I	ISA IO channel check.
RESET#	6	5v	I	active low reset.
Interrupt/DMA Steering and Plug and Play				
IRQ3-7, 9-11, 14, 15	18-21, 47-50, 52, 53	5v	I	ISA interrupts.
INT#A-D	28, 29, 32, 33	5v	I	PCI interrupts.
PIRQ1-0	22, 23	5v	I	Plug and play port interrupts.
DRQ0-3, 5-7	75-73, 67-64	5v	I	ISA DMA request signals.
DACK#0-3, 5-7	62-56	5v	O	ISA DMA acknowledgments.
DACEN	40	5v	I	ISA DACK decoder latching and output enable.
PDRQ1-0	24, 25	5v	I	Plug and play port DMA requests.
PDAK#1-0	26, 27	5v	O	Plug and play port DMA acknowledgements.
VT82C575M Interface				
SCANIN	4	5v	O	Scan input to the VT82C575M.
SCANOUT	7	5v	I	Scan output from the VT82C575M.
REGCS#	35	5v	I	Internal register chip select.
XDIR	36	5v	I	Direction control of the internal XD0-7 to SD0-7 buffer.
SDIR	70	5v	I	Direction control of the internal XD0-7 to SD8-15 buffer.
SDOE#	71	5v	I	Output enable of the internal XD0-7 to SD8-15 buffer.
Power and Ground				
VDD	5, 41, 31, 72	5v	I	Power supply of 4.5 to 5.5v
VDD_RTC	98	5v	I	Power supply for the internal real time clock.
VSS	1, 30, 51, 68, 89, 96	0v	I	Ground.
NC	37, 39			Not Connected

VT82C416 PIN OUT IN NUMERICAL ORDER

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	31	VDD	51	VSS	81	XD2
2	RTCCS#	32	INTC#	52	IRQ14	82	XD1
3	KBCS#	33	INTD#	53	IRQ15	83	XD0
4	SCANIN	34	IOCHK#	54	SD6	84	SD4
5	VDD	35	REGCS#	55	SD5	85	SD3
6	RESET#	36	XDIR	56	DACK#7	86	SD2
7	SCANOUT	37	NC	57	DACK#6	87	SD1
8	KBLOCK	38	24Mhz	58	DACK#5	88	SD0
9	KBTURBO	39	NC	59	DACK#3	89	VSS
10	KBCLK	40	DACEN	60	DACK#2	90	RTCAS
11	KBDATA	41	VDD	61	DACK#1	91	IOR#
12	MSCLK	42	SD11	62	DACK#0	92	IOW#
13	MSDATA	43	SD10	63	SA2	93	CLK
14	SD15	44	SD9	64	DRQ7	94	CLK_2
15	SD14	45	SD8	65	DRQ6	95	PD
16	SD13	46	SD7	66	DRQ5	96	VSS
17	SD12	47	IRQ7	67	DRQ3	97	VBAT
18	IRQ3	48	IRQ9	68	VSS	98	VDD_RTC
19	IRQ4	49	IRQ10	69	OSC	99	RTCX1
20	IRQ5	50	IRQ11	70	SDIR	100	RTCX2
21	IRQ6			71	SDOE#		
22	PIRQ1			72	VDD		
23	PIRQ0			73	DRQ2		
24	PDRQ1			74	DRQ1		
25	PDRQ0			75	DRQ0		
26	PDAK#1			76	XD7		
27	PDAK#0			77	XD6		
28	INTA#			78	XD5		
29	INTB#			79	XD4		
30	VSS			80	XD3		

VT82C416 PIN DIAGRAM

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storate temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	Voltage
Output voltage (V_{DD} = 5V)	-0.5	5.5	Voltage
Output voltage (V_{DD} = 3.1 - 3.6V)	-0.5	V_{DD} + 0.5	Voltage

Note :

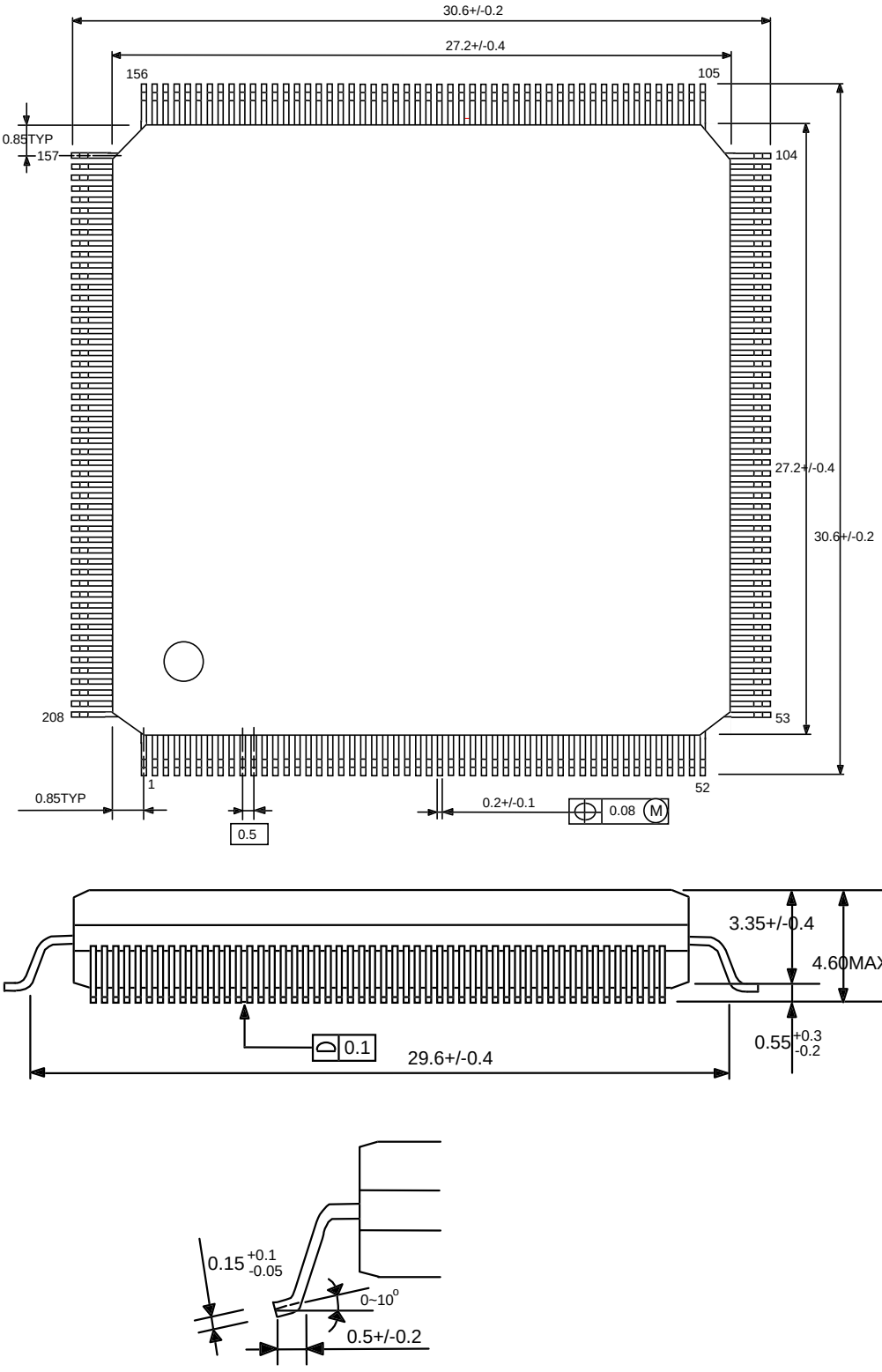
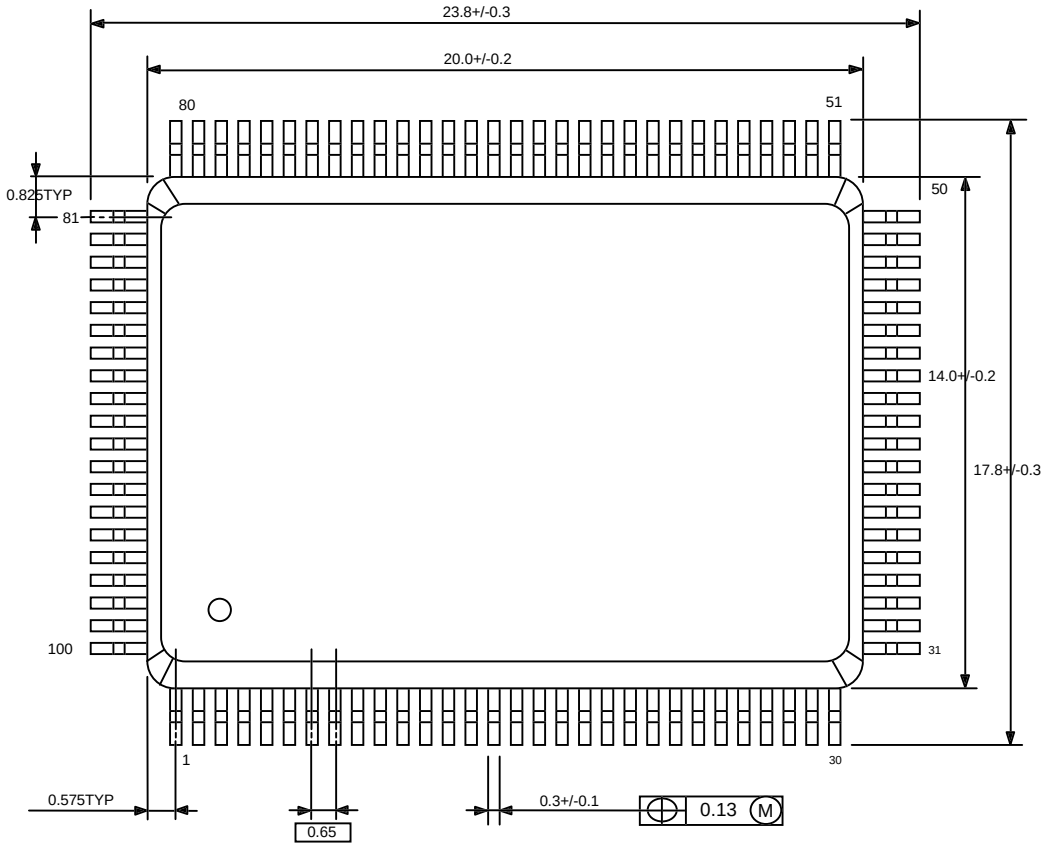
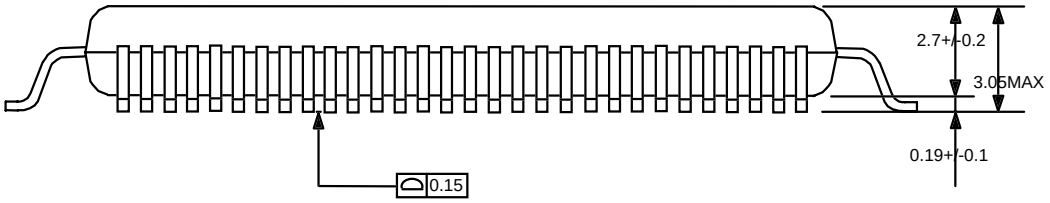
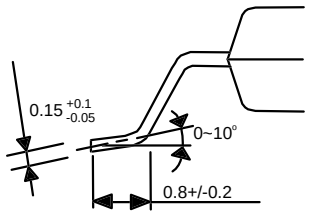
Stress above these listed cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{o}C, V_{DD}=5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
VIL	Input low voltage	-.50	0.8	V	
VIH	Imput high voltage	2.0	V_{DD}+0.5	V	
VOL	Output low voltage	-	0.45	V	I_{OL}=4.0mA
VOH	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
IIL	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
IOZ	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
ICC	Power supply current	-	80	mA	

208-PIN PLASTIC FLAT PACKAGE



100-PIN PLASTIC RECTANGULAR FLAT PACKAGE