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Configuration Register of VT82C570M

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VT82C575M

Two ports are provided for the access of configuration registers, first by write 8 bit index to port A8H and then by read or write 8 bit from/to data port A9H.

- RX00: Chip and revision ID (read only)
  bit 7-4 = Chip ID = 1000
  bit 3-0 = Revision ID

- RX01: XD bus switch register
  Bit 0-1 reflects XD bus XD0-1 power-on jumper setting, 1 reflects pull high, 0 reflects pull low.
  bit 7 = 1/0 : disable/enable parity check.
  bit 6 = reserved.
  bit 5 = reserved, must be 1.
  bit 4 -3 = reserved
  bit 2 = Desktop/Notebook mode
  bit 1-0: reserved.

- RX02: Slow counter. Pulse width of STPCLK# throttling is controlled by bit 6-0.
  bit 7-5 = reserved.
  ..bit 4 = set throttling clock time base.
  1: 1.7 msec
  0: 3.35 usec.
  bit 3-0 = STPCLK# duty cycle. (from 1/16 to 15/16, default is 4/16, 0 means disable.)

- RX03: ISA bus control (default is 00H)
  bit 7 = 1/0 : extra/normal ISA command delay.
  bit 6 = 1/0 : 0/1 ROM wait state.
  bit 5 = 1/0 : 5/4 ISA slave wait state.
  bit 4 = 1/0 : 4/2 chipset register wait state.
  bit 3 = 1/0 : enable/disable I/O recovery time.
  bit 2 = 1/0 : enable/disable extend BALE.
  bit 1 = 1/0 : reserved, must be 0.
  bit 0 = 1/0 : enable/disable decouple refresh.

- RX04: ISA bus control (default is 00H)
  bit 7 = reserved, must be 0.
  bit 6 = 1/0 : enable/disable internal XRDY when slow down CPU clock.
  bit 5 = 1/0 : enable/disable Port 92H fast reset.
  bit 4 = reserved, must be 0.
  bit 3 = reserved, must be 0.
  bit 2 = reserved, must be 0.
  bit 1 = 1/0 : enable/disable parity check of ISA master and DMA cycle.

bit 0 = 1/0 : enable/disable PCI controller (82C576MV)

- RX10: DMA clock
  bit 7 = reserved
  bit 6 = 1/0 :DMA clock = ISA bus clock/half ISA bus clock.
  bit 5 = 1/0 disable/enable Latch IO16# at 1st conversion cycle
  bit 3 = 1/0 Enable/disable IOCHK#
  bit 2-0 = reserved

- RX11: ISA bus clock rate (default is 00H)
  bit 7 = 1/0 : enable/disable SA16 reversal for FLASH EPROM.
  bit 6 = 1/0 : enable/disable ROM write for FLASH ROM.
  bit 5 = 1/0 : enable/disable PS/2 mouse lock.
  bit 4 = 1/0 : enable/disable PS2 mouse enable
  bit 3 = 1/0 : enable/disable ISA CLK selection of bit 2-0. If disabled, ISA CLK=CCLK/8.
  bit 2-0 = 000 : CLKIN/3
  001 : CCLK/2
  010 : CCLK/4
  011 : CCLK/6
  100 : CCLK/5
  101 : CCLK/10
  110 : CCLK/12
  111 : OSC/2 (14.318MHz/2=7.159MHz)
  Note : Procedure for ISA bus clock switching.
  1. Set bit 3 = 0.
  2. Change value of bit 2-0.
  3. Set bit 3 = 1.

- RX20: DRAM configuration (default is 31H), also refer to RX44 and RX47-48.
  bit 7-5 = Bank 0 number of column address
  000 : disable
  001 : 9-bit (256K-bit DRAM)
  010 : 10-bit (1M-bit DRAM)
  011 : 11 bit (4M-bit DRAM)
  100 : 12 bit (16M-bit DRAM)
  others: illegal
  bit 4 = 1/0 : enable/ disable DRAM page mode
  bit 3-1 = Bank 1 number of column address
  000 : disable
  001 : 9-bit (256K-bit DRAM)
  010 : 10-bit (1M-bit DRAM)
  011 : 11 bit (4M-bit DRAM)
  100 : 12 bit (16M-bit DRAM)
  others: illegal
  bit 0 = 1/0 : DRAM 64/32 bit width.

- RX21: DRAM configuration (default is 0EH)
  bit 7-5 = Bank 2 number of column address
  000 : disable
  001 : 9-bit (256K-bit DRAM)
  010 : 10-bit (1M-bit DRAM)
  011 : 11 bit (4M-bit DRAM)
  100 : 12 bit (16M-bit DRAM)
  others: illegal

bit 4 = 1/0 : enable/disable ISA master write delay by 1 cycle.
bit 3-1 = Bank 3 number of column address
000 : disable
001 : 9-bit (256K-bit DRAM)
010 : 10-bit (1M-bit DRAM)
011 : 11 bit (4M-bit DRAM)
100 : 12 bit (16M-bit DRAM)
others: illegal
bit 0 = reserved

- RX22: DRAM timing (default is 44H)
bit 7-6 = RAS# precharge width
00 : 2 cycles
01 : 4 cycles
10 : 6 cycles
11 : 8 cycles
bit 5-4 = RAS# pulse width
00 : 4 cycle
01 : 6 cycles
10 : 8 cycles
11 : 10 cycles
bit 3-2 = Read cycle CAS# pulse width
00 : 1 cycle
01 : 2 cycles
10 : 3 cycles
11 : 4 cycles
bit 1 = Write cycle CAS# pulse width
0 : 1 cycle
1 : 2 cycles
bit 0 = RAS# to column address and column address to CAS#
0 : 1 cycle
1 : 2 cycles

- RX30: C segment shadow control (default is 00H)
bit 7 = 1/0 : enable/disable CC000-CFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable CC000-CFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable C8000-CBFFF shadow area read operation.
bit 4 = 1/0 : enable/disable C8000-CBFFF shadow area write operation.
bit 3 = 1/0 : enable/disable C4000-C7FFF shadow area read operation.
bit 2 = 1/0 : enable/disable C4000-C7FFF shadow area write operation.
bit 1 = 1/0 : enable/disable C0000-C3FFF shadow area read operation.
bit 0 = 1/0 : enable/disable C0000-C3FFF shadow area write operation.

- RX31: D segment shadow control (default is 00H)
bit 7 = 1/0 : enable/disable DC000-DFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable DC000-DFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable D8000-DBFFF shadow area read operation.
bit 4 = 1/0 : enable/disable D8000-DBFFF shadow area write operation.
bit 3 = 1/0 : enable/disable D4000-D7FFF shadow area read operation.
bit 2 = 1/0 : enable/disable D4000-D7FFF shadow area write operation.
bit 1 = 1/0 : enable/disable D0000-D3FFF shadow area read operation.
bit 0 = 1/0 : enable/disable D0000-D3FFF shadow area write operation.

- RX32 E/F segment shadow and DRAM burst control (default is 00H)

bit 7 = 1/0 : enable/disable E0000-EFFFF shadow area read operation.
bit 6 = 1/0 : enable/disable E0000-EFFFF shadow area write operation.
bit 5 = 1/0 : enable/disable F0000-FFFFF shadow area read operation.
bit 4 = 1/0 : enable/disable F0000-FFFFF shadow area write operation.
bit 3 = 1/0 : enable/disable 1 wait delay of high double word access.
bit 2 = 1/0 : enable/disable 1MB hole at top of 16MB, start from 0F00000H.
bit 1 = 1/0 : reserved
bit 0 = 1/0 : reserved

- RX33: ROM decoding and DRAM relocation (default is 00H).
  bit 7 = 1/0 : C8000-CFFFF is decoded as ROM/ISA cycle.
  bit 6 = 1/0 : C0000-C7FFF is decoded as ROM/ISA cycle.
  bit 5 = 1/0 : E8000-EFFFF is decoded as ROM/ISA cycle.
  bit 4 = 1/0 : E0000-E8FFF is decoded as ROM/ISA cycle.
  bit 3-2 = 256K/384K relocation
  00 : no relocation
  01 : illegal
  10 : 256K relocation
  11 : 384K relocation
  bit 1 = reserved, must be 0.
  bit 0 = reserved, must be 0.

- RX40: ROM cacheable (default is 00H)
  bit 7 = 1/0 : enable/disable C0000-C7FFF to be cacheable and write protect.
  bit 6 = 1/0 : enable/disable F0000-FFFFF to be cacheable and write protect.
  bit 5 = 1/0 : enable/disable E0000-EFFFF to be cacheable and write protect.
  bit 4 = reserved.
  bit 3 = 1/0 : enable/disable CAS before RAS refresh.
  bit 2 = 1/0 : enable/disable 2nd level cache line fill, even CACHE# is deasserted.
  bit 1 = 1/0 : enable/disable delay CAS# by 1 clock for DATA LINK BUS master write.
  bit 0 = 1/0 : enable/disable delay CAS# by 1/2 clock for DRAM burst write.

- RX41: Non-cacheable area base address
  bit 7-0 = A28-A21

- RX42: Non-cacheable area base address/size (default is 00H)
  bit 7-3 = A20-A16
  bit 2-0 = non-cacheable area size
  000 : disable
  001 : 64KB
  010 : 128KB
  011 : 256KB
  100 : 512KB
  101 : 1MB
  110 : 2MB
  111 : 4MB

- RX43: DRAM size and SIMM type
  bit 7-5 = DRAM size of bank 0
  000 : 1MB
  001 : 2MB
  010 : 4MB
  011 : 8MB
  100 : 16MB

101 : 32MB
110 : 64MB
111 : 128MB
bit 4 = 1/0 : double/single side SIMM for bank 0
bit 3-1 = DRAM size of bank 1
000 : 1MB
001 : 2MB
010 : 4MB
011 : 8MB
100 : 16MB
101 : 32MB
110 : 64MB
111 : 128MB
bit 0 = 1/0 : double/single side SIMM for bank 1

- RX44: DRAM size and SIMM type
bit 7-5 = DRAM size of bank 2
000 : 1MB
001 : 2MB
010 : 4MB
011 : 8MB
100 : 16MB
101 : 32MB
110 : 64MB
111 : 128MB
bit 4 = 1/0 : double/single side SIMM for bank 2
bit 3-1 = DRAM size of bank 3
000 : 1MB
001 : 2MB
010 : 4MB
011 : 8MB
100 : 16MB
101 : 32MB
110 : 64MB
111 : 128MB
bit 0 = 1/0 : double/single side SIMM for bank 3

- RX47: DRAM type select
bit 7,3 = 00/01/10 : Standard/Burst EDO/EDO DRAM for bank 3
bit 6,2 = 00/01/10 : Standard/Burst EDO/EDO DRAM for bank 2
bit 5,1 = 00/01/10 : Standard/Burst EDO/EDO DRAM for bank 1
bit 4,0 = 00/01/10 : Standard/Burst EDO/EDO DRAM for bank 0

- RX48: 32 bit DRAM select
bit 7 = 1/0 DRAM start at T2/T1
bit 6 = 1/0 Burst SRAM GWE mechanism is used/un-used
bit 5 = 1/0 enable EDO DRAM test mode
bit 4 = 1/0 1ws for MD to CD pop
bit 3 = 1/0 32/64 bit DRAM for bank 3
bit 2 = 1/0 32/64 bit DRAM for bank 2
bit 1 = 1/0 32/64 bit DRAM for bank 1
bit 0 = 1/0 32/64 bit DRAM for bank 0

- RX49: Misc. control

bit 7 = snoop ahead and unlimited burst
bit 6 = PCI master access DRAM at rate of 2-1-2-1 ...
bit 5 = 8 CWE option
bit 4 = DRAM post write enable
bit 3 = CPU pipeline enable
bit 2 = Burst EDO programming mode enable
bit 1 = concurrent write back enable
bit 0 = Burst EDO cycle latency

- RX4A: 570M MISC. controll
  bit 7 = add 1WS for master access Burst EDO.
  bit 6 = allow single write posted
  bit 5 = force RAS pre-charge after DRAM burst access
  bit 4 = Burst EDO burst write supported
  bit 3 = CAS pre-charge 2T for DRAM burst write
  bit 2 = RAS pre-charge 2T when DRAM bank switched
  bit 1 = delay CAS by 1/2 CCLK for min-CAS requirement.
  bit 0 = reserved

- RX50 : Cache access mode (default is 00H)
  bit 7 = 1/0 : enable/disable second level cache.
  bit 6 = 1/0 : enable/disable cache initialization mode.
  bit 5 = 1/0 : enable/disable linear burst order for Cyrix CPU.
  bit 4-3 = tag and dirty bit configuration
  00 : 8 bit tag, no dirty.
  01 : 7 bit tag with dirty bit.
  10 : 8 bit tag with dirty bit.
  11 : 10 bit tag with dirty bit.
  bit 2 = burst synchronous SRAM type
  0: non-pipelined burst synchronous SRAM
  1: pipelined burst synchronous SRAM
  bit 1 = Data link bus master cache read timing.
  0 : 2-1-1-1
  1 : 3-2-2-2
  bit 0 = Data link bus master cache write timing.
  0 : 2-1-1-1
  1 : 3-2-2-2
- RX51 : Cache timing control (default is 00H)
  bit 4: data SRAM type 0: synchronous SRAM
  1: asynchronous SRAM
  bit 7: read hit timing for the first cycle (CPU clock) for asynchronous SRAM:
  0: 1 wait state (3-x-x-x)
  1: 2 wait state (4-x-x-x)
  bit 6: write hit timing for the first cycle for asynchronous SRAM:
  0: 1 wait state (3-x-x-x)
  1: 2 wait state (4-x-x-x)
  bit 5: read hit timing for the second-fourth burst cycle for asynchronous SRAM:
  0: 1 wait state (x-2-2-2)
  1: 2 wait state (x-3-3-3)
  * write hit timing is always 1 wait state (x-2-2-2) for asynchronous SRAM
  * read hit and write hit timing is always 3-1-1-1 for synchronous SRAM
  bit 3 = 1/0 : 2 banks/ 1 bank cache SRAM.
  bit 2-0 = cache size
  000 : no cache

001 : reserved
010 : 64KB
011 : 128KB
100 : 256KB
101 : 512KB
110 : 1MB
111 : 2MB

- RX52 : Primary activity detector control (reload idle timer)
  bit 7 = 1/0 : enable/disable detection of keyboard access, R/W port 60H.
  bit 6 = 1/0 : enable/disable detection of serial port, R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF.
  bit 5 = 1/0 : enable/disable detection of parallel port, R/W port 378-37F, 278-27F.
  bit 4 = 1/0 : enable/disable detection of video access, R/W port 3B0-3DF, memory A and B segment.
  bit 3 = 1/0 : enable/disable detection of IDE and floppy access. R/W port 1F0-1F7, 3F5.
  bit 2 = reserved.
  bit 1 = 1/0 : enable/disable detection of Turbo pin, positive and negative edge.
  bit 0 = 1/0 : enable/disable detection of DRQ/PREQ#, positive edge for DRQ, negative edge for PREQ#.
  Note : RX52 is used with RX54 bit 5 to control the source of power management interrupt.

- RX53 : Primary activity status
  bit 7 = 1/0 : keyboard activity exist/not exist, (R/W port 60H).
  bit 6 = 1/0 : serial port activity exist/not exist, (R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF).
  bit 5 = 1/0 : parallel port activity exist/not exist, (R/W port 378-37F, 278-27F).
  bit 4 = 1/0 : video activity exist/not exist, (R/W port 3B0-3DF, memory A and B segment).
  bit 3 = 1/0 : IDE and floppy activity exist/not exist, (R/W port 1F0-1F7, 3F7).
  bit 2 = reserved.
  bit 1 = 1/0 : Turbo pin activity exist/not exist, (positive and negative edge).
  bit 0 = 1/0 : DRQ/PREQ# activity exist/not exist, (positive edge for DRQ, negative edge for PREQ#.
  Note :
  1. RX53 is not controlled by RX52, it will be latched with or without enable RX52.
  2. But RX53 is also used to generate power management interrupt if RX54 bit 5 is enabled. The status of primary activities can only be cleared by write 1 to individual bit, and it is recommended to clear RX53 before enable RX52 and RX54 bit 5.

- RX54 : Power management interrupt (PMI) event control
  bit 7 = 1/0 : enable/disable idle timer time out to trigger PMI.
  bit 6 = 1/0 : enable/disable GP timer time out to trigger PMI.
  bit 5 = 1/0 : enable/disable primary activity to trigger PMI.
  bit 4 = 1/0 : enable/disable positive IRQ edge to trigger PMI.
  Note : Each IRQ can be individually controlled to trigger PMI, please refer to RX60 and RX61.
  bit 3 = 1/0 : enable/disable turbo pin to trigger PMI.
  bit 2 = 1/0 : enable/disable DRQ/PREQ# to trigger PMI.
  bit 1 = 1/0 : enable/disable peripheral or secondary event timer time out to trigger PMI.
  bit 0 = write 1 to this bit generates a software PMI.

Note : RX53 is used to generate power management interrupt if RX54 bit 5 is enabled. The status of primary activities can only be cleared by write 1 to individual bit, and it is recommended to clear RX53 before enable RX52 or RX54 bit 5.

- RX55 : Power management interrupt (PMI) status
  bit 7 = idle timer time out.
  bit 6 = GP timer time out.
  bit 5 = primary activity.
  bit 4 = positive IRQ edge.
  bit 3 = turbo pin.
  bit 2 = DRQ/PREQ# pulse.
  bit 1 = perripheral or secondary event timer time out.
  bit 0 = software PMI.
  Note : The status of power management interrupt can only be cleared by write 1 to individual bit.

- RX56 : CPU clock control
  bit 7-5 = reserved
  bit 4 = reserved.
  bit 3-0 = clock generator selection of 82C416MV

bit 2	bit 1	bit 0	bit 3=1	bit 3=0
0	0	0	8Mhz	16Mhz
0	0	1	20Mhz	40Mhz
0	1	0	25Mhz	50Mhz
0	1	1	40Mhz	80Mhz
1	0	0	33.3Mhz	66.6Mhz
1	0	1	50Mhz	100Mhz
1	1	0	4Mhz	8Mhz
1	1	1	30Mhz	60Mhz

Note : Procedure to change clock.
1. Write clock selection value to RX56 bit 7-5.
2. Set RX5D bit 7 to 1.

- RX58 : General purpose timer (time base is bit7-6 of RX59h)

- RX59 : GP timer and Idle time control
  bit 7-6 = GP timer clock selection.
  00 : disable
  01 : 32.768K
  10 : 1 second
  11 : 1 minute
  bit 5-4 = STPCLK# recovery time or auto stop grant delay time

bit5,4	STPCLK# recovery time (RX5D bit 3 = 0)	Auto stop grant delay time (RX5D bit 3 = 1)
00	immediately	immediately
01	1ms	0.5ms
10	0.375 ms	0.1875ms
11	0.125 ms	0.0625ms

bit 3-1= Idle timer
000 : disable

001 : 2 second
010 : 8 second
011 : 32 second
100 : 2 minute
101 : 8 minute
110 : 16 minute
111 : 32 minute

Note : Idle timer time out is not re-triggerable, the correct procedure to use idle timer is:

1. Load idle timer value into RX59 bit 3-1.
2. Set RX54 bit 7 to 1, start counting.
3. After time out, reload idle timer value (RX59 bit 3-1) and set RX54 bit 7 again.

bit 0 = reserved

- RX5A : General purpose output ports. (Please refer to demo schematics VT5035.)
  bit 7-2 = reserved
  bit 1 = DPC1 value in notebook mode (pin #190)
  bit 0 = DPC0 value in notebook mode (pin #189)

- RX5B : SMM control
  bit 7 = 1/0 : enable/disable power management mode.
  bit 6-5 = reserved
  bit 4 = 1/0 : enable/disable SMI access redirected to a000h-bffffh
  bit 3 = 1/0 : enable/disable to access DRAM A0000-BFFFF.
  bit 2 = reserved
  bit 1 = 1/0 : enable/disable force SMM mode, which forces access of 30000-4FFFF remap to A0000-BFFFF.
  bit 0 = 1/0 : enable/disable STPCLK# throttling mode, the STPCLK# will periodically be asserted to reduce power consumption of CPU. STPCLK# pulse width is controlled by RX02.

- RX5C : STPCLK control
  bit 7 = wait for HALT cycle to start clock change.
  0 : immediately
  1 : wait for HALT
  bit 6 = 1/0 enable/disable wait for STPCLK acknowledge
  bit 5 = 1/0 used STPCLK# protocol for changing the CPU clock, must be set to 1
  bit 4-3 = reserved
  bit 2 = reserved, must be 0.
  bit 1 = reserved.
  bit 0 = reserved

- RX5D : Leakage control
  bit 7 = write 1 to start change CPU clock operation.
  bit 6 = 1/0 : enable/disable PMI to automatically wakeup clock.
  bit 5 = reserved.
  bit 4 = 1/0 : enable/disable turbo pin to be used as keyboard lock, (low active).
  bit 3 = reserved
  bit 2 = 1/0 : enable/disable CPU interface leakage control when power-down.
  bit 1 = 1/0 : enable/disable DRAM interface leakage control when power-down
  bit 0 = 1/0 : enable/disable power-down in zero clock

- RX5E : Misc.

bit 7 = 1/0 : enable/disable Write-Back CPU mode.
bit 6 = 1/0 : write through/write back second level cache mode.
Note : Second level cache write through mode can only be used with burst write disabled.
bit 5-3 = reserved.
bit 2 = 1/0 : enable/disable two times longer slow refresh.
bit 1 = 1/0 : enable/disable high word parity check.
bit 0 = write 1 to this bit asserts STPCLK# signal and force CPU goes into suspend without change clock.

- RX5F: Conserve and secondary event mode control (default: 00H)
  bit 7-6 = conserve mode time out value
  00 : 1/16 sec
  01 : 1/8 sec
  10 : 1 second
  11 : 1 minute
  Note : This value is the time elapsed to go into conserve mode if there is no primary activity.
  bit 5 = 1/0 : enable/disable conserve mode.(write)
  : status of conserve mode. (read)
  bit 4 = conserve mode clock select
  0 : CLKIN/2
  1 : CLKIN/4
  bit 3-2 = secondary event timer value
  00 : 2 ms
  01 : 16 ms
  10 : 64 ms
  11 : after EOI (IO write to port 20H) plus 0.125ms
  Note : System will wake up (go to secondary event mode) when secondary event is coming, andthen automatically exit from secondary event mode after this time value is elapsed.
  bit 1 = 1/0 : enable/disable secondary event mode. (write)
  : status of secondary event mode. (read)
  bit 0 = secondary event mode clock select
  0 : CLKIN (full speed)
  1 : CLKIN/2

- RX60 : Interrupt event detection control
  bit 7 = 1/0 : set IRQ7 as primary event.
  bit 6 = 1/0 : set IRQ6 as primary event.
  bit 5 = 1/0 : set IRQ5 as primary event.
  bit 4 = 1/0 : set IRQ4 as primary event.
  bit 3 = 1/0 : set IRQ3 as primary event.
  bit 2 = 1/0 : set IRQ1 as primary event.
  bit 1 = 1/0 : set IRQ0 as primary event.
  bit 0 = 1/0 : enable/disable IRQ to reload idle timer. (default is 0)
  Note :
  1. Primary event can be used to reload idle timer or generate PMI.
  2. RX60 bit 0 must be used with RX60 bit 7-1 and RX61 bit 7-0 to control IRQ reload idle timer.
  3. RX54 bit 4 must be used with RX60 bit 7-1 and RX61 bit 7-0 to control IRQ positive edge to trigger PMI.

- RX61 : Interrupt event detection control

bit 7 = 1/0 : set IRQ15 as primary event.
bit 6 = 1/0 : set IRQ14 as primary event.
bit 5 = 1/0 : set IRQ13 as primary event.
bit 4 = 1/0 : set IRQ12 as primary event.
bit 3 = 1/0 : set IRQ11 as primary event.
bit 2 = 1/0 : set IRQ10 as primary event.
bit 1 = 1/0 : set IRQ9 as primary event.
bit 0 = 1/0 : set IRQ8 as primary event.

- RX62 : Level trigger interrupt control
  bit 7 = 1/0 : enable/disable IRQ7 as a level trigger interrupt. (default is 0)
  bit 6 = 1/0 : enable/disable IRQ6 as a level trigger interrupt. (default is 0)
  bit 5 = 1/0 : enable/disable IRQ5 as a level trigger interrupt. (default is 0)
  bit 4 = 1/0 : enable/disable IRQ4 as a level trigger interrupt. (default is 0)
  bit 3 = 1/0 : enable/disable IRQ3 as a level trigger interrupt. (default is 0)
  bit 2 = 1/0 : reserved.
  bit 1 = 1/0 : reserved.
  bit 0 = 1/0 : enable/disable level trigger interrupt.(default is 0)
  Note : RX62 bit 0 must be used with RX62 bit 7-3 and RX63 to control level trigger interrupt.

- RX63 : Level trigger interrupt control
  bit 7 = 1/0 : enable/disable IRQ15 as a level trigger interrupt. (default is 0)
  bit 6 = 1/0 : enable/disable IRQ14 as a level trigger interrupt. (default is 0)
  bit 5 = reserved.
  bit 4 = 1/0 : enable/disable IRQ12 as a level trigger interrupt. (default is 0)
  bit 3 = 1/0 : enable/disable IRQ11 as a level trigger interrupt. (default is 0)
  bit 2 = 1/0 : enable/disable IRQ10 as a level trigger interrupt. (default is 0)
  bit 1 = 1/0 : enable/disable IRQ9 as a level trigger interrupt. (default is 0)
  bit 0 = reserved

- RX64: Power on switch setting.
  bit 7 = 1/0 : disable/enable 1 clock BRDY# delay for burst write cycle.
  bit 6 = 1/0 : enable/disable EADS# asserted at the beginning of SMI#
  bit 5 = 1/0 : enable/disable DRAM burst write.
  bit 4 = 1/0 : enable/disable always return READY# in SMI# cycle, for AMD and UMC CPU.
  bit 3 = switch setting of MA3.
  bit 2 = switch setting of MA2.
  bit 1 = switch setting of MA1.
  bit 0 = switch setting of MA0.

- RX65: Peripheral and secondary event timer control
  bit 7 = 1/0 : enable/disable keyboard access to reload the peripheral timer, R/W port 60H.
  bit 6 = 1/0 : enable/disable serial port to reload the peripheral timer, R/W port 3F8-3FF, 2F8-2FF, 3E8-3EF, 2E8-2EF.
  bit 5 = 1/0 : enable/disable video access to reload the peripheral timer, R/W port 3B0-3DF, memory A and B segment.
  bit 4 = 1/0 : enable/disable IDE and floppy access to reload the peripheral timer, R/W port 1F0-1F7, 170-177, 3F5.
  bit 3 = 1/0 : enable/disable parallel port access to reload the peripheral timer, R/W port 378-37F, 278-27F.
  bit 2 = reserved.

bit 1 = 1/0 : enable/disable speaker/sound port access to reload the peripheral timer, R/W port 43 and 220.
bit 0 = reserved.

- RX66: Peripheral timer control
  bit 7-4 : reserved
  bit 3-2 = peripheral timer select
  00 : disable
  01 : 32.768K
  10 : 1 second
  11 : 1 minute
  bit 1-0 : reserved.

- RX67: Peripheral timer count value (time base is bit 3-2 of RX66h).

- RX68: External PMI signal falling enable (default: 00H)
  bit 7 = enable PMI for GPIO5 (pin 95) falling
  bit 6 = enable PMI for GPIO4 (pin 94) falling
  bit 5 = reserved.
  bit 4 = enable PMI for GPIO0 (pin 7) falling
  bit 3 = enable PMI for GPIO1 (pin 8) falling
  bit 2 = enable PMI for GPIO6 (pin 32) falling
  bit 1 = enable PMI for GPIO7 (pin 31) falling
  bit 0 = reserved.

- RX69: External PMI signal rising enable (default: 00H)
  bit 7 = enable PMI for GPIO5 (pin 95) rising
  bit 6 = enable PMI for GPIO4 (pin 94) rising
  bit 5 = reserved.
  bit 4 = enable PMI for GPIO0 (pin 7) rising
  bit 3 = enable PMI for GPIO1 (pin 8) rising
  bit 2 = enable PMI for GPIO6 (pin 32) rising
  bit 1 = enable PMI for GPIO7 (pin 31) rising
  bit 0 = reserved.

- RX6A: External PMI status (write 1 to clear)
  bit 7 : GPIO5 (pin 95) triggered PMI
  bit 6 : GPIO4 (pin 94) triggered PMI
  bit 5 : reserved
  bit 4 : GPIO0 (pin 7) triggered PMI
  bit 3 : GPIO1 (pin 8) triggered PMI
  bit 2 : GPIO6 (pin 32) triggered PMI
  bit 1 : GPIO7 (pin 31) triggered PMI
  bit 0 : reserved.

- RX6B: Extended PMI enable (default: 00H)
  bit 7 = 1/0 : disable/enable RESETCPU in power down mode.
  bit 6 = 1/0 : disable/enable RESDRV in power down mode.
  bit 5 = 1/0 : debounce clock select: 512ms/8ms.
  bit 4 = 1/0 : Conserve mode based on clock throttling/stretching.
  bit 3 : reserved
  bit 2 = 1/0 : enable/disable the peripheral timer time out to trigger PMI
  bit 1 = 1/0 : enable/disable secondary event timer time out to trigger PMI
  bit 0 = 1/0 : enable/disable external PMI pin to trigger PMI

- RX6C: Extended PMI status
  bit 7-3 : reserved
  bit 2 : peripheral timer time out
  bit 1 : secondary event timer time out
  bit 0 : external PMI pin triggering

- RX70 : Port 70h shadow register

- RX7B : General I/O ports control
  bit 7-0 : 0/1 intput/ouput general I/O port direction

- RX7C : GPIO7-0 (pin 31, 32, 95, 94, 11-7) port value
  bit 7-0 : I/O port value

- RX7E : General output port PC7-0 (shared pin with MA[11,4], external latch required)
  bit7-0 : output value for PC7-0.

- RX7F : General output port GPO5-0 (direct output in notebook mode, pin 93-88)
  bit7-6 : reserved
  bit5-0 : output value for GPO5-0.

VT82C576M

Two ports are provided for the access of VT82C576M internal configuration registers, first by write 8 bit index to port A8H and then by read or write 8 bit from/to data port A9H.

- RX80h: ID register(default is 02h)

- RX81h: on-board memory size: <CA27-20> (default is 01h)
  Note: Which is used with RX98h to select from CA32 to CA20.

- RX82h: buffer control (default is 00h)
  bit 7 = 1/0: CPU to PCI write buffer enable/disable
  bit 6 = 1/0: PCI to CPU write buffer enable/disable
  bit 5: reserved
  bit 4 = 1/0: PCI accessing CPU prefetch buffer enable/disable
  bit 3 = 1/0: PCI dynamic acceleration decoding enable/disable
  Note: The dynamic acceleration decoding window is 1K size.
  bit 2 : reserved
  bit 1 = 1/0: Enable/disable linear write; PCI master write on-board memory with CPU burst cycle.
  bit 0 = 1/0: Enable/disable linear read; PCI master read on-board memory with CPU burst cycle.

- RX83h: Data link bus interface timing (default is 00h)
  bit 7-4 = reserved
  bit 6 = reserved
  bit 5 = reserved
  bit 4 = reserved
  bit 3 = 1/0: on-board memory detection point (DEVSEL# asserted) for PCI master at first data phase/address phase
  bit 2 = must be 0.
  bit 1 = reserved
  bit 0 = must be 0

- RX84h: PCI interface timing (default is 03h)
  bit 7 = 1/0: slave mode lock function enable/disable
  bit 6 = 1/0: retry count at 64 times/16 times
  bit 5 = 1/0: retry deadlock error reporting (PERR# and NMI) enable/disable
  bit 4 = 1/0: retry status occurred/no occurred (write a 1 to reset)
  bit 3 = 1/0: CPU to PCI fast back to back enable/disable
  bit 2 = 1/0 Fast/normal Frame
  bit 1-0 = 11/10/01/00: DEVSEL# decoding time subtractive/slow/medium/fast
  Note: Bit 1,0 are used to determine when to terminate PCI and start ISA cycle.

- RX85h: PCI arbitration (default is 00h)
  bit 7 = 1: arbitration mechanism based on fairness between CPU and PCI
  0: arbitration mechanism based on PCI priority only
  bit 6 = 1: arbitration mode using FRAME# based (arbitrate at each FRAME#)
  0: arbitration mode using REQ# based (arbitrate at end of REQ#)
  bit 5-4 = 11/10/01/00: CPU time slot at 32/16/8/4 PCI clock
  Note: Bit 7,bit5-4 are only available for FRAME# based arbitration.
  bit 3-0: PCI master bus time out
  0000: disable

0001: 1x32 PCI clock
0010: 2x32 PCI clock
.....
1111: 15x32 PCI clock
Note: Bit 3-0 are only available for REQ# based arbitration.

- RX86h: configuration mechanism and misc. control (default is 00h)
  bit 7 = 1/0: PCI configuration register mechanism #2/#1
  Mechanism #1: Accessed by index CF8h and data CFCh.
  Mechanism #2: Accessed by Cx00h to CxFFh.
  bit 6,5 = reserved
  bit 4 = 1/0: must be 0
  bit 3 = 1/0: enable/disable SERR# to generate NMI
  bit 2 = 1/0: SERR# generation status (writing a 1 clears status)
  bit 1 = 1/0: PCI master BROKE timer enable/disable (16 clocks)
  bit 0 = reserved

- RX93h: misc. control (default is 40h)
  bit 4,7,6: HIADDR address
  000: CA26 above
  001: CA27 above
  010: CA28 above
  011: CA29 above
  100: CA30 above
  101: CA31 above set this value for 570
  111: disable
  bit 5 = 1/0: IOCHCK#/NMI multi-function pin definition
  Note: This pin is floating before RX93h is written.
  bit 3 = reserved
  bit 2 = reserved
  bit 1 = reserved
  bit 0 = 1/0 On board IO accelerated ISA decoding enable/disable (port 00h-FFh)

- RX96h: Miscellaneous (default is 00h)
  bit 7 =0: dynamic decoding on both memory read and write
  1: dynamic decoding on memory write
  bit 6: Retry time out action
  0 no action taken except record status and retry forever
  1 take action to flush buffer, return FFFFFFFF and retry 16/64 times depend on RX84
  bit 5 = 1: dynamic decoding buffer reset and disable
  0: dynamic decoding enable
  bit 4 = enable PCI controller
  bit 3 = reserved
  bit 2 = reserved
  bit 1 = 1/0: PCI master 1/0 wait state write
  bit 0 = reserved.

- RX98h: On board memory ending address(default is 00h)
  bit 4-0: On board memory ending address <32:28>

- RX99h: Miscellaneous(default is 00h)
  bit 7 = 1/0: enable/disable byte merge capability
  bit 6 = 1/0: enable/disable enhanced byte merge

bit 5 = 1/0: enable/disable PCI dynamic bursting
bit 4 = 1/0: enable/disable retry fail pop data out only
bit 3 = 1/0: enable/disable 2-way dynamic decoding
bit 2-0 = reserved

- RX9A - internal IDE controller ID - (00001)
  bit 7 = 1/0 enable/disable IDE enable - IDEEN
  bit 6-5 = reserved
  bit 4-0 = IDE configuration IDSEL decoding - IDEID[4:0]
  map to CFGADDR[15:11] in mech #1
  map to CA[11:8] in mech #2 (IDEID4 is dont care)

- RX9B -
  bit 7-3 = reserved
  bit 2 = 1/0 enable/disable dual CPU mode
  bit 1= 1/0 linear order/intel order on CPU side
  bit 0 = Reserved.

- RX9C - Programmable IO chipselect A. High Address
  bit 7-0 = programmable I/O address A<7:0>

- RX9D - Programmable I/O Chipselect A. Low Address
  bit 7-2 = 1/0 compare/not compare. Programmable I/O address compare mask for A<5:0>
  bit 1-0 = programmable I/O address A<9:8>

- RX9E - Programmable IO chipselect B. High Address
  bit 7-0 = programmable I/O address B<7:0>

- RX9F - Programmable I/O Chipselect B. Low Address
  bit 7-2 = 1/0 compare/not compare. Programmable I/O address compare mask for B<5:0>
  bit 1-0 = programmable I/O address B<9:8>

- RXA0
  bit 7 = 1/0 enable/disable PCI master concurrent mode
  bit 6 = 1/0 enable/disable IDE master concurrent mode
  bit 1 = 1/0 enable/disable read backoff when PCI read retry fail
  bit 0 = 1/0 enable/disable master cycle snoop ahead

VT82C416

Two ports are provided for the access of configuration registers, first by write 8 bit index to port A8H and then by read or write 8 bit from/to data port ACH.

- RXFBh: Plug and play DRQ routing
  bit 7-6: reserved
  bit 5-3: PDRQ1 routing

000: DRQ0	001: DRQ1	010: DRQ2	011: DRQ3
100: reserved	101: DRQ5	110: DRQ6	111: DRQ7

  bit 2-0: PDRQ0 routing: same as PDRQ1 routing

- RXFCh: PCI interrupt polarity
  bit 7-4: reserved
  bit 3 = 1/0: INTA# invert (edge)/non-invert (level)
  bit 2 = 1/0: INTB# invert (edge)/non-invert (level)
  bit 1 = 1/0: INTC# invert (edge)/non-invert (level)
  bit 0 = 1/0: INTD# invert (edge)/non-invert (level)

- RXFDh: Plug and play IRQ routing
  bit 7-4: INTD# routing

0000: reserved	0001: IRQ1	0010: reserved	0011: IRQ3
0100: IRQ4	0101: IRQ5	0110: IRQ6	0111: IRQ7
1000: IRQ8	1001: IRQ9	1010: IRQ10	1011: IRQ11
1100: IRQ12	1101: reserved	1110: IRQ14	1111: IRQ15

  bit 3-0: PIRQ0 routing:

0000: reserved	0001: IRQ1	0010: reserved	0011: IRQ3
0100: IRQ4	0101: reserved	0110: IRQ6	0111: IRQ7
1000: IRQ8	1001: IRQ9	1010: IRQ10	1011: IRQ11
1100: IRQ12	1101: reserved	1110: IRQ14	1111: IRQ15

- RXFEh: PCI IRQ routing
  bit 7-4: INTA# routing: same as INTD routing
  bit 3-0: INTB# routing: same as INTD routing

- RXFFh: PCI IRQ routing
  bit 7-4: INTC# routing: same as INTD routing
  bit 3-0: PIRQ1 routing: same as INTD routing

PCI Configuration Register: The access method is controlled by RX86h bit7. Please refer to PCI specification.

Bus Controller:

Mandatory header field (or IDX00 and IDX04 based on the 32-bit IO port convention)

ID Function
- 1,0 - Vendor ID = 1106h (read only)
- 3,2 - Device ID = 0576h (read only)
- 5,4 - Command register
  - bit 0: IO space = 1 (read only)
  - bit 1: memory space = 1 (read only)
  - bit 2: bus master = 1 (read only)
  - bit 3: special cycle monitoring = 0 (read only)
  - bit 4: memory write and invalid command = 0 (read only)
  - bit 5: VGA palette snoop = 0 (read only)
  - bit 6: parity error response (read/write, default=0)
  - bit 7: address/data stepping = 0 (read only)
  - bit 8: SERR# enable (read/write, default=0)
  - bit 9: fast back-to-back cycle enable (read/write, default=0)
  - bit 15-10: reserved
- 7,6 - Status register (or IDX06<15:0>)
  - bit 0-6: reserved
  - bit 7: fast back-to-back: reserved
  - bit 8: data parity detected: reserved
  - bit 9-10: DEVSEL# timing: reserved
  - bit 11: signaled target abort: reserved
  - bit 12: received target abort (read only, write one to clear)
  - bit 13: signaled master abort: reserved
  - bit 14: signaled system error: reserved
  - bit 15: detected parity error (write only, write one to clear)
- 08 - Revision I.D. _____
- 09 - Program Interface = 00h
- 0A - Sub class code = 00h
- 0B - Class code = 06h

IDE Controller

Port	Function
1,0	Vendor ID : 1106h
3,2	Device ID : 1571h
5,4	Command bit 9 fast back to back cycles, default: disabled bit 8 SERR# enable, default: disabled bit 7 (address stepping), default: enabled bit 6 parity error response, default: disabled bit 5 fixed at 0 (VGA palette snoop) bit 4 fixed at 0 (memory write and invalidate) bit 3 fixed at 0 (special cycles) bit 2 bus master, default: disabled

S/G operation can be issued only when bus master is enabled.
bit 1 memory space, default: disabled
bit 0 I/O space, default: disabled
Memory map I/O operation: when I/O space is disabled, the device will not respond to any I/O address for both compatible and native mode and will tristate its interrrupt output (ie, /IRQ15/INTA#/INTB#).

7,6 Status
bit 15 detected parity error
bit 14 signaled system error
bit 13 received master abort
bit 12 received target abort
bit 11 fixed at 0 (signaled target abort)
bit 10,9 DEVSEL# timing, default : medium
bit 8 data parity detected
bit 7 fixed at 0 (fast back to back)

8 Revision ID.

9 Programming interface
bit 7 Master IDE capability supported.
bit 6-4 fixed at 0
- When DA0 is strapped at 0 to be compliant with PCI SIG specification
bit 3 fixed at 1 (secondary channel capable of supporting both compatible and native modes)
bit 2 secondary channel mode indicator, default: strapped from pin DA1
bit 1 fixed at 1 (primary channel capable of supporting both compatible and native modes)
bit 0 primary channel mode indicator, default: strapped from pin DA1
- When DA0 is strapped at 1 to support glueless conversion mode
bit 3-0 fixed at 0

B-A Base class and sub-class code: 01h-01h

C fixed at 0

D Latency timer

E-F fixed at 0

13-10 Primary data/command base address
an 8 byte IO address space, default: 1F0h
bit 31-16 : must be 0
bit 15-3 : port address
bit 2-0 : 001b

17-14 Primary control/status base address
a 4 byte IO space, default 3F4h (only the third byte is active, ie: 3F6h)
bit 31-16: must be 0
bit 15-2 : port address
bit 1-0 : 01b

1B-18 Secondary data/command base address, default: 170h

1F-1C Secondary control/status base address, default 374h

23-20 Base address for bus master control registers
a 16 byte IO address space, detailed in the previous section
bit 31-16: must be 0
bit 15-4 : port address
bit 3-0 : 0001b

27-24 Memory base address (8KB) for memory mapped I/O of the two channels
bit 31-13: port address
bit 12-0 : must be 0

2C-2D Sub-System vendor ID
If EEPROM interface is enabled, the first two bytes of EEPROM is read after reset as the sub-system vendor ID.

33-30 Expansion ROM base address
An optional 64K byte expansion ROM space
bit 31-16: ROM base address
bit 15-4 : Port address
bit 3-0 : Address decode enable

3C Interrupt line: default, 0Eh

3D Interrupt pin: read/only;
01h for native mode interrupt routing,
00h for legacy mode interrupt routing.

3E min_gnt

3F max_lat

40 Chip enable register
bit 7-4 chip ID (r/o): inverted from the strapped value of DCS3A#, DCS1A#, DCS3B# and DCS1B# (00h-0Fh)
bit 3 R/W. reserved
bit 2 R/W. reserved
bit 1 primary channel enable, default: disabled
bit 0 secondary channel enable, default: disabled

41 IDE configuration
bit 7 primary IDE read prefetch buffer enable, default: disabled
bit 6 primary IDE post write buffer enable, default: disabled
bit 5 secondary IDE read prefetch buffer enable, default: disabled
bit 4 secondary IDE post write buffer enable, default: disabled
bit 3 status for PERR# response enable, default: disabled
bit 2 alternative native secondary channel interrupt
bit 1 DCS16# source:
1: Decode from BE[3:0]#
0: From input pin DCS16#
bit 0 status for SERR# response enable, default: disabled

42 Misc. control
bit 7 native/compatible IO base for the primary channel (default: DA1)
1: native mode, need relocation

0: compatible mode, fixed IO

bit 6 native/compatible IO base for the secondary channel (default: DA1)
1: native mode, need relocation
0: compatible mode, fixed IO

bit 5 fixed at 0

bit 4 fixed at 0

bit 3 R/W. reserved.

bit 2 monitor IDE command to start master action. Default: disabled

bit 1 R/W. reserved.

bit 0 DEVSEL# timing (also reflected in register 7)

43 FIFO configuration

bit 7 R/W. reserved

bit 6-5 FIFO configuration between the two channels

bit(6:5)	primary	secondary	
00	16	0	
01	8	8	(default)
10	8	8	
11	0	16	

bit 4 R/W. reserved.

bit 3-2 threshold for the primary channel

bit 1-0 threshold for the secondary channel
00 : 1 01: 3/4
10: 1/2 11: 1/4

44

bit 7 reserved

bit 6 Master read cycle IRDY wait state. 1: one wait (default)
0: zero wait

bit 5 Master write cycle IRDY wait state.1: one wait (default)
0: zero wait

bit 4 1/0 enable/disable (default) FIFO output data 1/2 clock advance.

bit 3 1/0 enable (default)/disable Retry Bus Master IDE status register read when master write operation for DMA read is not complete.

bit 2-0 R/W. reserved.

45

bit 7 R/W. reserved.

bit 6 Swap the interrupt steering of the two channels. default:disabled.

bit 5-2 Set to 0.

bit 1-0 R/W. reserved.

46

bit 7 1/0 enable (default)/disable FIFO flush for Read DMA when interrupt asserts primary channel.

bit 6 1/0 enable (default)/disable FIFO flush for Read DMA when interrupt asserts secondary channel.

bit 5 1/0 enable/disable (default) FIFO flush at the end of each sector for the primary channel.

bit 4 1/0 enable/disable (default) FIFO flush at the end of each sector for the secondary channel.

bit 3-2 Set to 0.

bit 1-0 Maximum DRDY pulse width after the cycle ocunt. Command will deassert inspite of DRDY status to avoid system ready hang.

00	no limitation	~
01	64 Tcycles	~1920 ns
10	128 cycles	~3840 ns

11 192 cycles ~5760 ns

48 Secondary IDE drive #1 timing control (default: A8h, ie: mode 0 timing, cycle time/active time ≅ 600/330 ns)
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

49 Secondary IDE drive #0 timing control
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

4A Primary IDE drive #1 timing control
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

4B Secondary IDE drive #0 timing control
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

4C Address setup time
- bit 7-6: primary drive #0
  - 00: 1T
  - 01: 2T
  - 10: 3T
  - 11: 4T (default)
- bit 5-4: primary drive #1
- bit 3-2: secondary drive #0
- bit 1-0: secondary drive #1

4D 1/2 Clock Control
- bit 7-6 Primary drive #0
- bit 5-4 Primary drive #1
- bit 3-2 Secondary drive #0
- bit 1-0 Secondary drive #1

If the number in bit 7-4 of register 4B to 48 is ***m***, then tthe number is bit 3-0 of register 4B-48 is ***n***. The Active /Recovery cycle with respect to register 4D becomes:

	Active	Recovery
00:	***m***+1	***n***+1
01	***m***+1	***n***+0.5
10	***m***+0.5	***n***+1
11	***m***+0.5	***n***+1.5

4E Secondary IDE drive non-1F0 port access timing (default: 0FFh)
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

4F Primary IDE drive non-1F0 port access timing (default: 0FFh)
- bit 7-4 DIOR#/DIOW# active pulse width
- bit 3-0 DIOR#/DIOW# recovery time

61-60 Sector size for the primary IDE
- bit 11-0 default: 200h (512 bytes)

69-68 Sector size for the secondary IDE
- default: 200h (512 bytes)

70 Primary IDE Status
- bit 7 fixed at 0
- bit 6 prefetch operation status
- bit 5 post write operation status
- bit 4 DMA read operation status
- bit 3 DMA write operation status
- bit 2 S/G operation in progress
- bit 1 FIFO empty
- bit 0 DMA request input status

71 Primary Interrupt Gating
- bit 0 Interrupt gating. When enabled, interrupt output will be asserted only when FIFO is empty. Default: disabled.

74 Primary IDE command
- bit 7 reload sector size after last command register write
- bit 6-0 reserved

75 Primary IDE command
- bit 7 start IDE slave read prefetch
- bit 6 start IDE slave post write
- bit 5 start IDE master DMA read
- bit 4 start IDE master DMA write
- bit 3 stop S/G bus master
- bit 2-0 reserved

78 Secondary IDE Status
- bit 7 fixed at 0
- bit 6 prefetch operation status
- bit 5 post write operation status
- bit 4 DMA read operation status
- bit 3 DMA write operation status
- bit 2 S/G operation in progress
- bit 1 FIFO empty
- bit 0 DMA request input status

79 Secondary Interrupt Gating
- bit 0 Interrupt gating. When enabled, interrupt output will be asserted only when FIFO is empty. Default: disabled.

7C Secondary IDE command
- bit 7 reload sector size after last command register write
- bit 6-0 reserved

7D Secondary IDE command
- bit 7 start IDE slave read prefetch
- bit 6 start IDE slave post write
- bit 5 start IDE master DMA read
- bit 4 start IDE master DMA write
- bit 3 stop S/G bus master
- bit 2-0 reserved

83-80 Primary channel PRD (physical region descriptor) table address pointer (alias with offset 4-7 of the PCI SIG defined bus master IDE registers).

8B-88 Secondary channel PRD table address pointer (alias with offset 4-7 of the PCI SIG defined bus master IDE registers).

C0 Test register, should be set to 00h.