Table 5-2. Definition of PD[23:0] at the Rising Edge of the Reset Signal

CR Bits	PD Bits	Value	Function
	System Bus Select		
CR36_1-0	1-0	00	Reserved
		01	VESA local bus
		10	PCI local bus
		11	Reserved
	Memory Page Mode Select		
CR36_3-2	3-2	00	Reserved
		01	Reserved
		10	Extended data out (EDO) mode
		11	Fast page mode
	Enable Video BIOS (VL-Bus)		
CR36_4	4	0	Disable video BIOS access (system BIOS contains video BIOS)
		1	Enable video BIOS access
	Display Memory Size		
CR36_7-5	7-5	000	4 MBytes (Trio64 only - reserved for Trio32)
		001	Reserved
		010	Reserved
		011	Reserved
		100	2 MBytes
		101	Reserved
		110	1 MByte
		111	0.5 MByte (Trio32 only)
	Enable Trio32/Trio64 (VL-Bus)		
CR37_0	8	0	Disable Trio32/Trio64 except for Video BIOS accesses
		1	Enable Trio32/Trio64
	Test Mode		
CR37_1	9	0	All outputs tri-stated and all bi-directional pins become inputs
		1	Normal operation. Certain outputs required for the reset process are not tri-stated during reset
	Video BIOS ROM Size (VL-Bus)		
CR37_2	10	0	64-KByte video BIOS
		1	32-KByte video BIOS
	Clock Select		
CR37_3	11	0	Use external DCLK on XIN pin and external MCLK on $\overline{\text{STRD}}$ pin (test purposes only)
		1	Use internal DCLK, MCLK
	RAMDAC Write Snooping (VL-Bus)		
CR37_4	12	0	Disable $\overline{\text{LOCA}}/\overline{\text{SRDY}}$ for RAMDAC writes
		1	Enable $\overline{\text{LOCA}}/\overline{\text{SRDY}}$ for RAMDAC writes