Appendix D

OEM Modifications for 168-Pin CPGA

This appendix describes the potential modifications an OEM needs to implement on an existing 486SX/DX motherboard to take advantage of the TI486SXL 168-pin CPGA. This package offers OEMs added flexibility in implementing solutions that support various 486 CPUs with the same motherboard.

The pinout of the TI486SXL 168-pin CPGA is nearly identical to the Intel™ or AMD™ 486SX CPGA pinout. The NC pins on the TI486SXL package that match signal pins on the 486SX have no internal connection and can be left connected to the 486SX signal pins when the board is configured as a TI486SXL board. This greatly simplifies the interface for the OEM. The classes of board designs covered are listed in the topic index below.

The board design requires the use of system logic that supports the Intel/Advanced Micro Devices 486 interface and the TI486SXL interface. Since board modifications for TI486SXL support are system-logic dependent, the implementation details are left to the board designer.The design examples show both *required* and *optional* jumper connections that **can** be made if the functions associated with them are needed. None of the optional signals require termination if not used.

Subsection D.5, *Power Planes for 3.3-V and 3.3-V/5-V Systems Using TI486SXL or 486DX4* on page D-9, shows a system implementation for a 3.3-V system that supports a 5-V ISA and a 3.3-V VL bus and another implementation for a mixed 3.3-V/5-V system that supports a 5-V ISA and a 5-V VL bus. In both implementations the microprocessor runs at 3.3 V.

The final responsibility for verifying designs incorporating any version of a TI486SXL microprocessor rests with the customer originating the motherboard design.

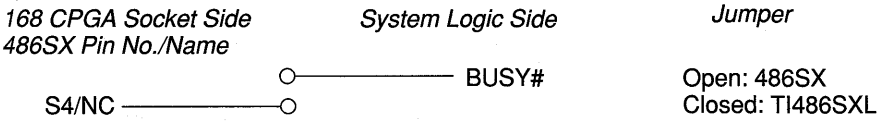
Topic **Page**

D.1 Boards Supporting TI486SXL and Intel

Pin names and assigned locations are provided in Chapter 6, *Mechanical Specifications.*

❑ **Function: Connect BUSY# to S4 (Required)**

BUSY# is required for coprocessor and self test. If neither is used, BUSY# can be left open as it has an internal pullup resistor.



❑ **Function: Hardware Cache Flush Support**

■ **CASE 1: Systems with no level-2 or parallel cache (optional)**

Hardware flush support for the TI486SXL is optional as this function may be implemented in software by setting bit 5 in TI486SXL Configuration Control register 0 (CCR0). However, the software implementation may negatively impact the performance of certain designs. To achieve maximum system performance, a hardware implementation is recommended as illustrated in Figure D–1. Also, see Appendix C, *Design Considerations and Cache Flush*, for more information.

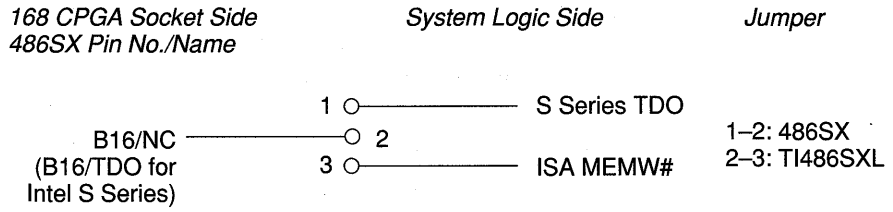
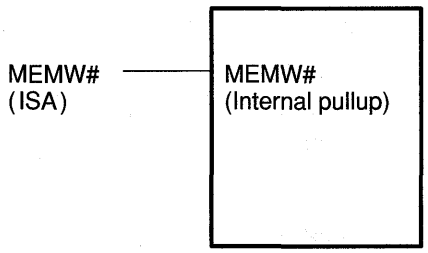


Figure D–1.FLUSH# for 144-Pin and 168-Pin TI486SXL



Note: The external flush logic is incorporated on the 144-pin and 168-pin TI486SXL chip.

Or

■ **CASE 2: Systems with a level-2 serial cache that do not hold the CPU during all DMA/Master cycles (required)**

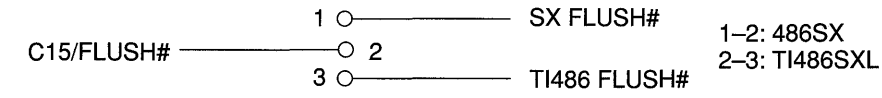
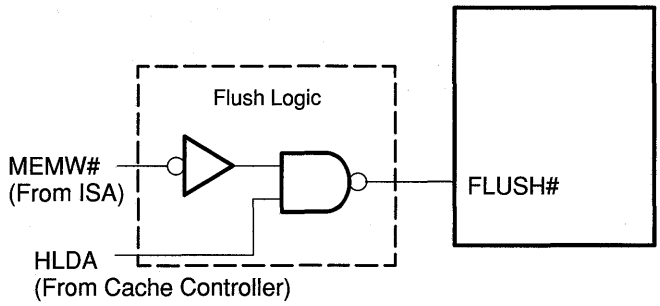
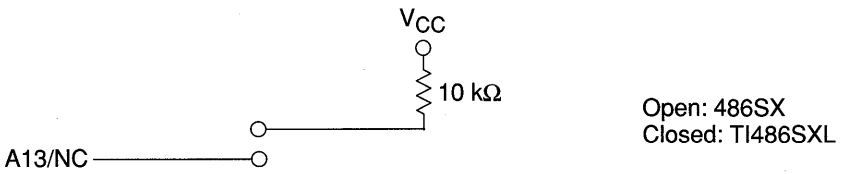


Figure D–2. FLUSH# Logic With Level-2 Serial Cache

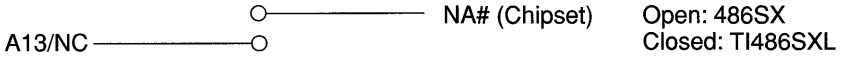


❑ Function: Pipeline Support (Required)

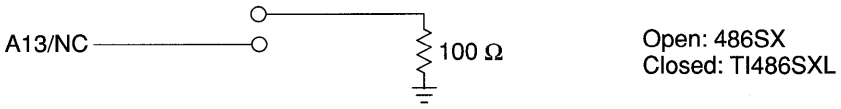
■ CASE 1: Chipset does not support pipelining.



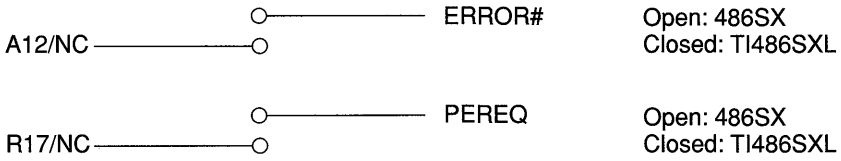
■ CASE 2: Chipset supports pipelining and drives NA#.



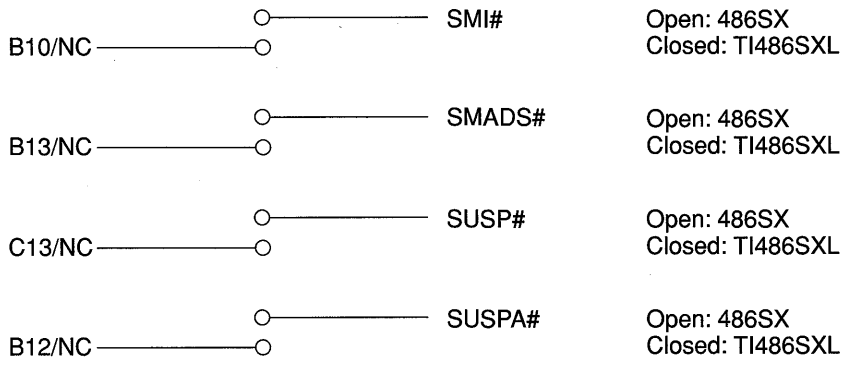
■ CASE 3: Chipset supports pipelining but does not drive NA#.



❑ Function: FPU Support (Optional)



❑ Function: Power Management Support (Optional)



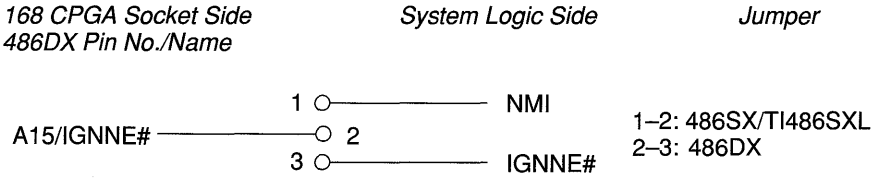
D.2 Boards Supporting TI486SXL and a 486DX

Pin names and assigned locations are provided in Chapter 6, *Mechanical Specifications.*

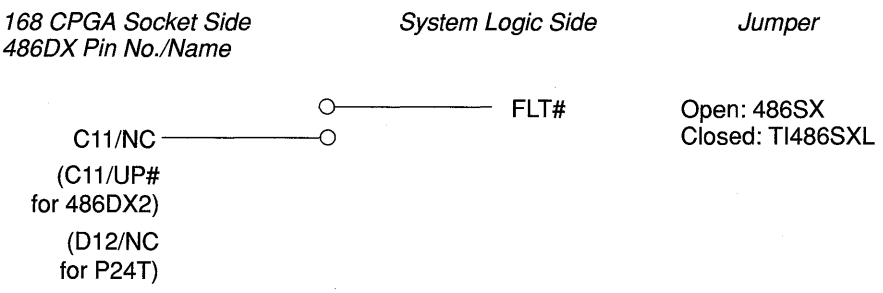
❑ Function: 486DX Support (Required)

Note:

For the 486DX to be supported in the same design, the following jumper is required in addition to those shown in Section D.1, *Boards Supporting TI486SXL, Intel, and AMD 486SX*, and any other differences in Intel/AMD supported pinouts.



❑ Function: 486DX2, P24T Upgrade Socket Support (Optional)



D.3 Boards Supporting TI486SXL and a 486DX4

Pin names and assigned locations are provided in Chapter 6, *Mechanical Specifications.*

❑ Function: 486DX4 PEREQ and CLKMUL (Required)

Note:

For the TI486SXL and the 486DX4 to be supported in the same design, the following jumpers are required in addition to any other differences in Intel/AMD supported pinouts. See subsections D.4, *Boards Supporting the VL Bus* on page D-7, and D.5, *Power Planes for 3.3-V and 3.3-V/5-V Systems Using TI486SXL or 486DX4* on page D-9.

168 CPGA Socket Side 486DX4 Pin No./Name	*System Logic Side*	*Jumper*
R17/CLKMUL — 1 / 2 / 3	1 — PEREQ 3 — CLKMUL	1–2: TI486SXL 2–3: 486DX4

❑ Function: Voltage Detect (Required)

168 CPGA Socket Side 486DX4 Pin No./Name	*System Logic Side*	*Jumper*
S4/VOLDET — 1 / 2 / 3	1 — BUSY# 3 — VOLDET	1–2: TI486SXL 2–3: 486DX4

❑ Function: Burst Mode (Required)

168 CPGA Socket Side 486DX4 Pin No./Name	*System Logic Side*	*Jumper*
R16/BLAST# — 3 10 kΩ between 1 and 2	1 — V_{SS} 2 — BLAST# (VL slot)	1–2: TI486SXL 2–3: 486DX4

D.4 Boards Supporting the VL Bus

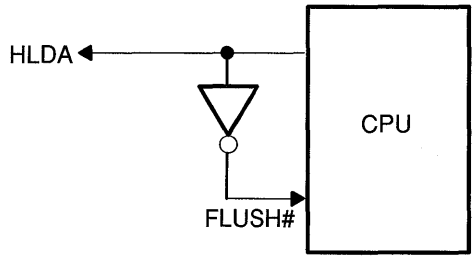
In order to support the VESA VL bus™ 2.0p Proposal, the following design guidelines should be considered.

D.4.1 Cache Snooping

In a VL-bus design, it is the function of the local bus controller to resolve arbitration between the CPU and the VL-bus master. For this architecture, the CPU can be forced to relenquish the host bus by asserting HOLD. There are two options for maintaining cache coherence:

- Use the BARB bit in Configuration Control register 0 (CCR0) to flush the internal cache.
- Use the inverted HLDA output of the CPU to perform a hardware FLUSH# to the CPU. See Figure D–3. The FLUSH# pin must be enabled by using bit 4 of CCR0.

Figure D–3.Hardware Flush



Note: Pin names and assigned locations are provided in Chapter 6, *Mechanical Specifications.*

These methods can be used only if the system logic supports the CPU HOLD arbitration scheme.

D.4.2 VL-Bus Clock

The VL-bus clock signal is a 1X clock that is in phase with the 486-type CPU and is driven by either the system logic or the local-bus controller. The VESA speciification allows for a frequency range of up to 66 MHz and dynamic clock scaling. The specification limits the low-to-high level skew from the CPU clock to LCLK as shown in Table D–1.

Table D–1. VL-Bus Skew

LCLK Max Frequency	Unit	Max Skew	Unit
33	MHz	3	ns
40		2.5	
50		2	

Systems that currently support a 1X and a 2X clock source should supply the 2X clock source to the CLK2 input of the TI486SXL and the 1X clock source to the VL-bus LCLK signal.

Systems that currently support only a 2X clock source can consider the addition of a PLL or clock divider to generate the 1X VL-bus clock.

D.4.3 VL-Bus Slot ID Settings

The VL-bus slot ID settings are shown in Table D–2.

Table D–2. VL-Bus Slot ID Settings

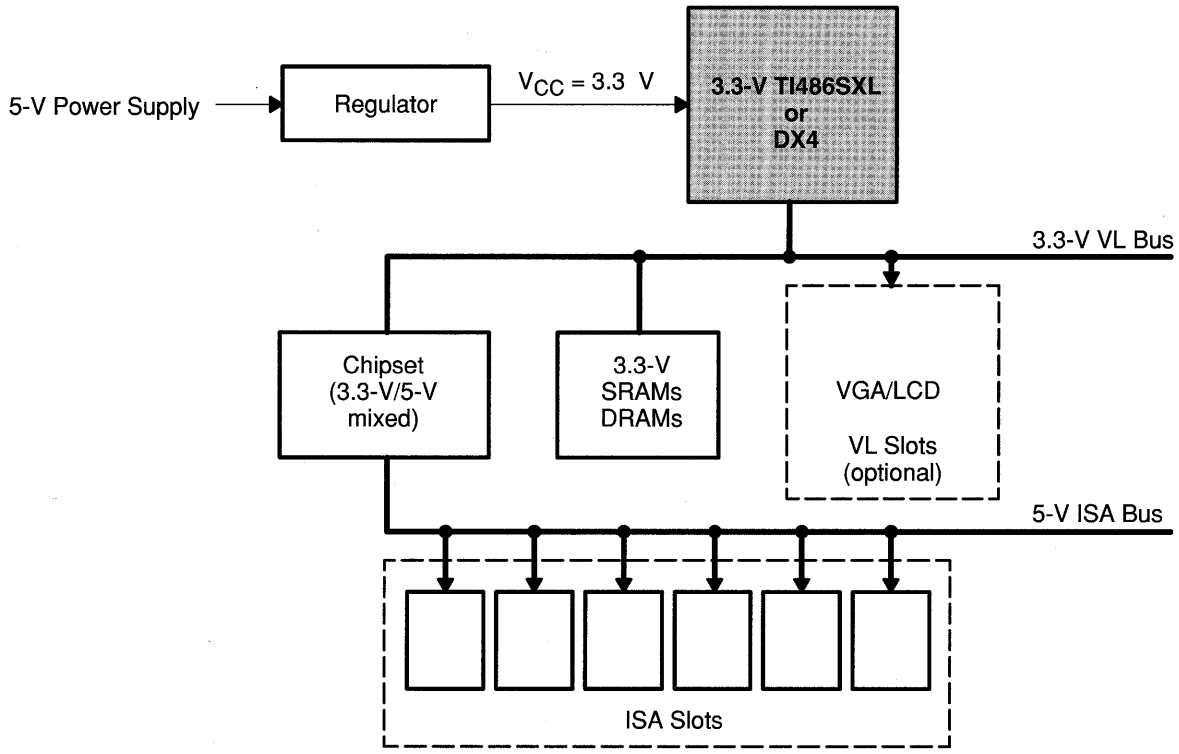
Slot ID	Setting	Comments
ID0	1	TI486SXL Mode
ID1	0	TI486SXL Mode
ID2	0 or 1	0: Minimum one wait state for writes 1: Zero wait states for writes
ID3	0 or 1	0: >33 MHz CPU clock speed 1: < 33 MHz CPU clock speed
ID4	0	Burst transfer not supported

D.5 Power Planes for 3.3-V and 3.3-V/5-V Systems Using TI486SXL or 486DX4

D.5.1 Power Planes for 3.3-V Systems

Figure D–4 shows the implementation of a 3.3-V system that supports use of either the TI486SXL or a 486DX4 microprocessor. This implementation yields a 5-V ISA bus and a 3.3-V VL bus with the microprocessor running at 3.3 V.

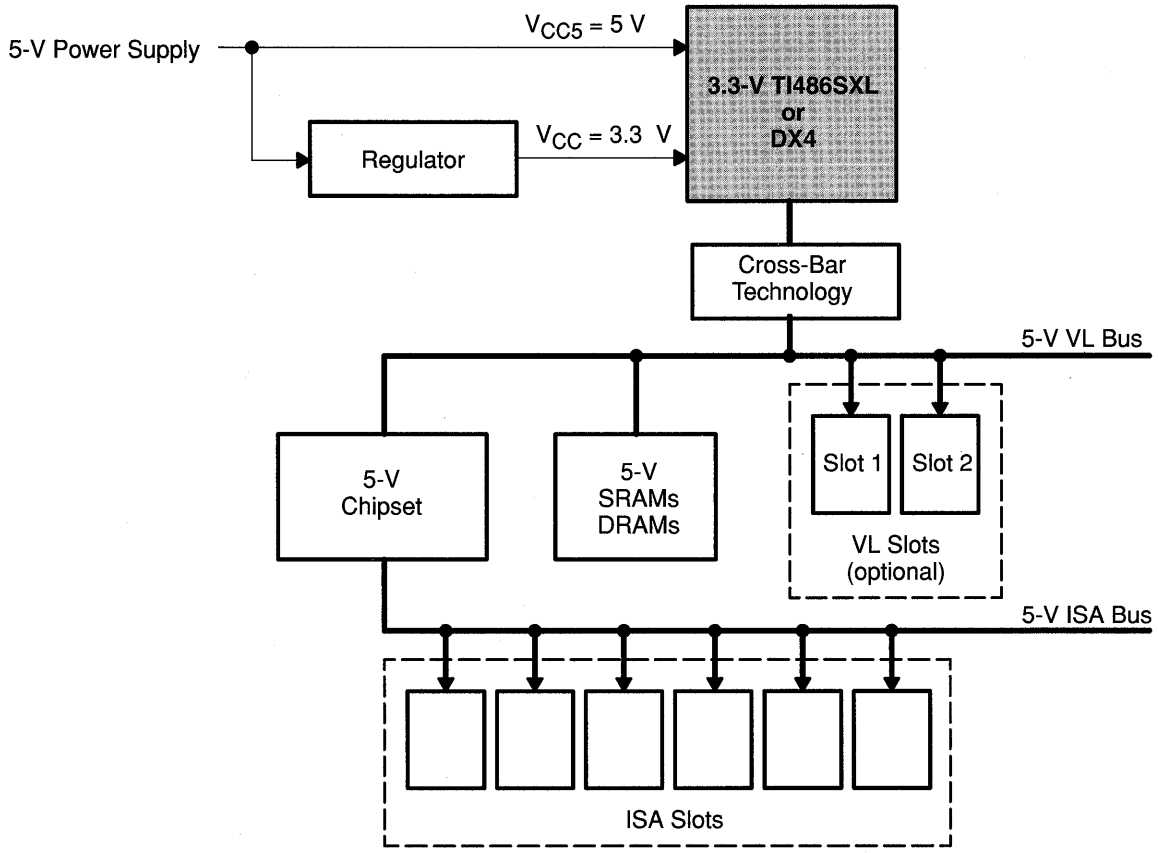
Figure D–4. 3.3-V VL-Bus Implementation



D.5.2 Power Planes for Mixed 3.3-V/5-V Systems

Figure D–5 shows the implementation of a 3.3-V/5-V system that supports use of either the TI486SXL or the 486DX4 microprocessor. This implementation yields a 5-V ISA and and a 5-V VL bus with the mocroprocessor running at 3.3 V.

Figure D–5. Mixed 3.3-V/5-V VL-Bus Implementation



D.6 Chipset Support

The following list of chipset vendors providing single-chipset solutions that support both the Intel/AMD and the TI486SXL interface was compiled from information received from the specified chipset vendors. This is a partial list and is not meant to be all inclusive.

- ACC Microelectronics
- Acer Laboratories
- EFAR
- ETEQ Microsystems
- Headland Technology
- OPTI
- PicoPower Technology
- SARC/PC Chip
- Silicon Integrated Systems (SIS)
- Symphony Laboratories
- Tidalwave
- UMC
- UniChip
- Western Digital