BUS1
BUSPC

GND
RESET
VCC
INQ2
-5V
DRQ2
-12V
UNUSED
+12V
GND
MEM
MEM
IOW
IOR
DACK3
DRQ3
DACK1
DRQ1
DACK0
CLK
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
TC
ALE
VCC
OSC
GND

IO
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
IO_READY
AEN
BA19
BA18
BA17
BA16
BA15
BA14
BA13
BA12
BA11
BA10
BA09
BA08
BA07
BA06
BA05
BA04
BA03
BA02
BA01
BA00

RESDRV
IRQ2
*CARDSEL
*MEMW
*MEMR
*IOW-ISA
*IOR-ISA
IRQ7
IRQ5
IRQ4
IRQ3

PC-DB7
PC-DB6
PC-DB5
PC-DB4
PC-DB3
PC-DB2
PC-DB1
PC-DB0
AEN
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2-ISA
A1-ISA
A0-ISA

U11
74LS245
A0 A1 A2 A3 A4 A5 A6 A7
A->B
CE
B0 B1 B2 B3 B4 B5 B6 B7
PC-DB0 PC-DB1 PC-DB2 PC-DB3 PC-DB4 PC-DB5 PC-DB6 PC-DB7
D0 D1 D2 D3 D4 D5 D6 D7
*IOR-ISA
*CS_IDE

U?
74LS245
PC-DB8 PC-DB9 PC-DB10 PC-DB11 PC-DB12 PC-DB13 PC-DB14 PC-DB15
D8 D9 D10 D11 D12 D13 D14 D15

IDE INTERRUPT SELECTION JUMPERS
J5
INTERRUPT
IRQ2 IRQ3 IRQ4 IRQ5 IRQ7
NOTE: Interrupts not used on current BIOSes

IDE1
CONN_20X2
*RESET D7 D6 D5 D4 D3 D2 D1 D0 GND DMARQ *IOW-IDE *IOR-IDE IORDY DMACK INTRQ A1-IDE A0-IDE *CS1FX *DASP
GND D8 D9 D10 D11 D12 D13 D14 D15 VCC_CF GND GND GND CSEL GND IOCS16 PDIAG A2-IDE *CS3FX GND

J4
CONN_2
VCC
IDE/CF POWER SUPPLY OPTION JUMPER

NOTE: FOR COMPATIBILITY MODE SET PINS 1-2 (DEFAULT) J2 AND J3
FOR HI-SPEED ("CHUCK MOD") MODE SET PINS 2-3 (OPTION) J2 AND J3

IDE IO PORT ADDRESS
RP1
10K
SW1
I/O ADDR
*CARDSEL
*CARDSEL_SWITCHED
Card Select (XT Slot 8 Support)
For use with Slot 8 Support mod

U8
74LS688
P=R
P0 P1 P2 P3 P4 P5 P6 P7
R0 R1 R2 R3 R4 R5 R6 R7
G
A9 A8 A7 A4 A5 A6
*CS_IDE
AEN

U6A U6B U6C U6D U6E
74LS04

U5A U5B U5C
74LS32

U7
74LS138
*IOW-ISA
*IOR-ISA
A2-ISA
A1-ISA
A0-ISA
A3
*HI_BYTE_OUTPUT
*IOR_DELAYED
RESDRV

U3
74LS245
A0 A1 A2 A3 A4 A5 A6 A7
A->B
CE
B0 B1 B2 B3 B4 B5 B6 B7
7 6 A2-ISA A1-ISA *IOR_DELAYED *IOW-ISA
*CS1FX *CS3FX A2-IDE A0-IDE A1-IDE *IOR-IDE *IOW-IDE *RESET

J1 J2
CONN_3

I/O Delay Chains
U4A U4B U4C U4D U4E U4F U5D
74LS04
*IOR-ISA
*IOR_DELAYED
*HI_BYTE_OUTPUT
*HI_OUT_DELAYED
*IOR_DELAYED causes IDE devices to output past the latch strobe time.
*HI_OUT_DELAYED causes the high data byte to be output past *IOR-ISA time.

Bypass and Decoupling Capacitors
C12 47uF
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11
ALL CAPS MARKED C ARE 0.01 - 0.1 uF BYPASS

Slot 8 Suppor Test Points
*CARDSEL_SWITCHED TP1
*IOR-ISA TP2
*CS_IDE TP3

Mounting Holes
GND P6
GND P7

RP2
10K
SW2
ROM OPT
D7
R2 10K
R3 10K
Switch Settings
1-4 ROM Address (ON == 1)
5 A14 Enable (ON == enabled)
6 A13 (ON == enabled)
7 ROM Enable (ON == enabled)
8 Write Enable (ON == enabled)
A14 A13 AEN *MEMW
/ROM_WE
ROM Address Notes:
For full 32K device (28C256) set S1 3,4,5,6 OFF
For 8K device (28C64B) set S1 5,6 ON
S1 3,4 become address switches

U10
74LS688
P=R
P0 P1 P2 P3 P4 P5 P6 P7
R0 R1 R2 R3 R4 R5 R6 R7
G
A16 A15 A17 A18 A19
/CS_ROM

U9
28C256
A0-ISA A1-ISA A2-ISA A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
D0 D1 D2 D3 D4 D5 D6 D7
PC-DB0 PC-DB1 PC-DB2 PC-DB3 PC-DB4 PC-DB5 PC-DB6 PC-DB7
/ROM_WE
*MEMR
/CS_ROM
WE OE CS

Optional (but probably desired) Boot ROM
NOTE: ROM 0xC0000 - 0xDFFFF only
RP2 always required, or 10K resistor between pins 1-2

NOTE: Only compatible with Atmel 28C64B revision 8K EEPROMs

J. Chapman
The Glitch Works
Sheet: /
File: XT-IDE-16bits.sch

Title: XT-IDE 8-bit ISA IDE Controller

Size: USLedger | Date: 2016-05-14 | **Rev: 3B**
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