

HANDLING PRECAUTIONS

→ **NOTE :** Static electricity may cause damage to the integrated circuits on the mainboard. Before handling any mainboard outside of its protective packaging, ensure that there is no static electric charge in your body.

Observe any or all of these basic precautions when handling the mainboard or other computer components:

- Wear a static wrist strap which fits around your wrist and is connected to a natural earth ground.
- Touch a grounded or anti-static surface or a metal fixture such as a water pipe.
- Avoid contact with the components on add-on cards, boards and modules and with the "golden finger" connectors plugged into the expansion slot. It is best to handle system components by their mounting bracket.

Above methods either prevent static build-up or cause it to be discharged properly.

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Table of Contents

Chapter 1 Overview

| | |
|----------------------|-----|
| Specifications | 1-1 |
| Mainboard Layout | 1-3 |
| System Block Diagram | 1-4 |

Chapter 2 Mainboard Settings

| | |
|---------------------------------------|------|
| Jumpers | 2-1 |
| CPU Selector Jumpers | 2-1 |
| NS87311/312 Jumper Setting | 2-3 |
| NS87332 Jumper Setting | 2-4 |
| CPU Clock Jumper JK1-JK4 (VT8225N) | 2-4 |
| System Jumper Setting | 2-5 |
| Keyboard Controller Select | 2-5 |
| Connectors | 2-6 |
| IDE Controller Select | 2-9 |
| VESA Bus Connector | 2-11 |
| 3.3-Volt Regulator Board Installation | 2-14 |

Chapter 3 Memory Subsystem

| | |
|--|-----|
| Memory Locations | 3-1 |
| Installing DRAM | 3-2 |
| SIMM Banks | 3-2 |
| DRAM Configuration | 3-2 |
| Installation Instructions | 3-6 |
| Cache Memory | 3-6 |
| Installing Cache Memory | 3-7 |
| Cache SRAM Specifications and Settings | 3-8 |
| 128K Cache SRAM | 3-8 |

Overview

Based on the VIA GMC chipset, the 486-VIP-IO mainboard combines an ISA/VL-bus platform with the advanced PCI local bus. The VESA local bus which allows the system to run synchronously with the CPU and the PCI local bus which improves the performance of disk I/O dramatically speeds up graphics performance. This motherboard design delivers unsurpassed flexibility that supports SMM (System Management Mode) CPUs, multi-master operations and provides built-in power management features ideal for Green PCs. The optional enhanced IDE support allows the installation of four host interface devices including CD-ROM drives.

The board's specially equipped chipset, VIA VT82C505, is a bus bridge that extends the ISA/VL-bus to a complete PCI/ISA/VL system by fully integrating system management interface, power management unit, keyboard controller with PS/2 mouse interface, clock stop mechanism and write-back level-one cache support. In addition, it meets PCI2.0 specification for proper arbitration between PCI masters and transaction between PCI masters and slaves. This chapter gives you a brief overview of this mainboard, providing basic information on its major parts and components.

Specifications

The 486-VIP-IO mainboard comes with the following features:

- Supports Intel 80486SX/DX/IntelDX2™/IntelDX4™/486 SL-Enhanced/Cyrix Cx486S/DX™ microprocessor in a PGA package.
- VIA VT82C486A-F PC/AT chipset includes built-in 8042 keyboard controller.
- VIA VT82C505-D chipset for VESA to PCI bridge.

- Optional Flash ROM.
- Award BIOS.
- Supports 128K/256K/512K/1M direct-mapped write-back/write-through cache memory.
- 72-pin SIMM sockets supports up to 64MB DRAM, provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors.
- Optional Regulator Daughter Board provides 3.45V for IntelDX4™ CPU.
- Supports three 16-bit ISA expansion slots.
- Supports two VESA bus expansion slots.
- Supports four PCI bus expansion slots.
- DALLAS DS12885Q real time clock/calendar.
- Provides built-in power management features necessary for Green PCs.
- Cable for the PS/2 mouse interface (optional).
- Supports VIA 83C461/Promise PDC20230C (optional) Local IDE.
- Optional enhanced IDE support allows for up to four host interface devices.
- Built-in IDE HDD/FDD and Local Bus IDE interface.
- NS PC87311/312/332 chipset for two serial/one parallel port.
- Supports ECP/EPP Protocol (NS 332 only).

Mainboard Layout

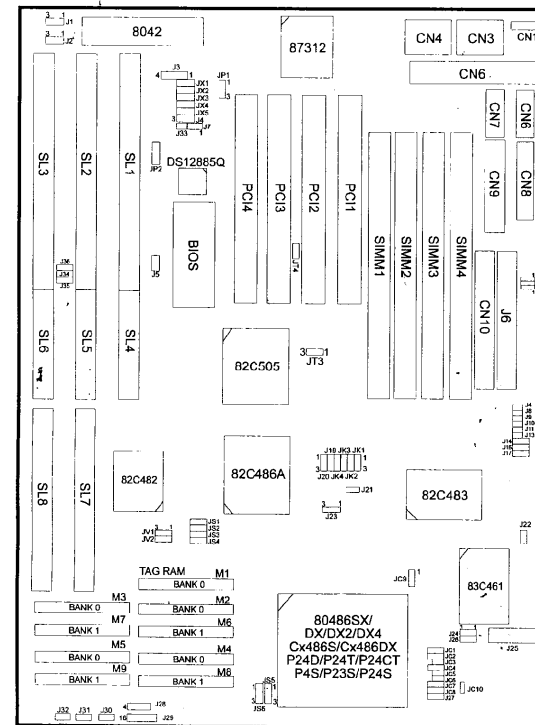


Figure 1-1. Mainboard Layout

| JUMPER (RP 00. 8P4R) | P23S/P4S/ P24S/P24T | 486SX/DX/ IntelDX2 | Cx486S/DX (M6, M7) | IntelDX4/ P24D/P24CT |
|-------------------------|------------------------|-----------------------|-----------------------|-------------------------|
| JC5 | short | open | open | short |
| RN18 | empty | empty | inserted | empty |
| RN19 | empty | empty | empty | inserted |
| RN20 | empty | empty | empty | empty |

| JUMPER | 486SX/ P23S | P24S*/P4S*/ 486DX/ Intel DX2/ Intel DX4 | P24CT/ P24T* | Cx486S (M6) | Cx486DX (M7) Cx486S+ Cx487S (M6 + C6) | P24D |
|----------|----------------|--|-----------------|----------------|--|-------|
| JC1, JC2 | 2-3 | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 |
| JC3 | open | open | short | open | open | open |
| JC4 | 1-2 | 1-2 | 2-3 | 1-2 | 1-2 | 2-3 |
| JC6 | short | short | short | open | open | short |

* P23S, P24S, P24D and P4S are the SL-enhanced CPUs while P24T is the Pentium OverDrive Processor.

→ **NOTE :** When the onboard 3.3-volt regulator is not present, the 3.3-volt daughter board should be inserted. If not, please read page 2-14.

| JUMPER | PIN DEFINITION |
|--------|---|
| JC7 | Write-back/write-through select for P24D/P24T 1-2 write-back 2-3 write-through |
| JC8 | For Intel's 3.3V CPU or Cyrix's 3.6V CPU 1-2 Intel DX4 2-3 Cyrix 486DX/DX2-V |
| JC9 | 1-2 Intel-S CPU 2-3 P24D/P24T/Cyrix 486DX |
| JC10 | If onboard regulator is present, selector for Intel's 3.3V CPU or Cyrix's 3.6V CPU open Intel DX4 short Cyrix 486DX/DX2-V |

Table 2-1. Jumper Setting for CPU Selector (Continued)

| JUMPER | PIN DEFINITION |
|---------------|--|
| J27 | DX4 clock mode select 1-2 2.5X mode 2-3 2X mode open 3X mode |
| JX1, J20, J23 | 1-2 (default) |
| JX2, JX5 | 2-3 (default) |
| JT3 | 1-2 IRQ14 2-3 IRQ10 (default) |
| JT4, J19 | 1-2 PCICLK=CPUCLK (default) 2-3 PCICLK=CPUCLK/2 (40MHz is recommended for better performance.) |

Table 2-1. Jumper Setting for CPU Selector

→ **NOTE :** Users are not encouraged to change the jumper settings not listed in this manual. Changing the jumper settings improperly may adversely affect system performance.

NS87311/312 Jumper Setting

| BASE I/O ADDRESS | | | |
|------------------|---------------|-------|--------------|
| JF | INDEX ADDRESS | | DATA ADDRESS |
| | 1-2 | 26EH* | 26FH* |
| | 2-3 | 398H | 399H |

| PRINTER PORT DIRECTION SELECT | | | |
|-------------------------------|--------|-------|-------------|
| JUMPER | OUTPUT | INPUT | BIDIRECTION |
| JG | 1-2* | 1-2 | 2-3 |
| JH | 2-3* | 1-2 | N/A |

* factory default

Table 2-2. NS87311/312 Jumper Setting

NS87332 Jumper Setting

| BASE I/O ADDRESS | | | | |
|------------------|-----|------|---------------|--------------|
| JF | JG | JH | INDEX ADDRESS | DATA ADDRESS |
| 1-2 | 1-2 | 2-3* | 2EH | 2FH |
| 1-2 | 2-3 | | 26EH* | 26FH* |
| 2-3 | 1-2 | | 15CH | 15DH |
| 2-3 | 2-3 | | 398H | 399H |

* factory default

Table 2-3. NS87332 Jumper Setting

CPU Clock Jumper JK1-JK4 (VT8225N)

| CLK 2 | 50 MHz | 40 MHz | 33.3 MHz | 25 MHz |
|-------|--------|--------|----------|--------|
| JK1 | 2-3 | 1-2 | 2-3* | 2-3 |
| JK2 | 1-2 | 1-2 | 2-3* | 1-2 |
| JK3 | 2-3 | 2-3 | 1-2* | 2-3 |
| JK4 | 2-3 | 1-2 | 1-2* | 1-2 |

* factory default

Table 2-4. CPU Clock Jumper Selection JK1-JK4 (VT8225N)

NS87332 ECP MODE DMA CHANNEL

| JP1, JP2 | DREQ1, DACK1 | DREQ3, DACK3 |
|----------|--------------|---------------|
| | 2-3 | 1-2 (default) |

Table 2-5. NS87332 ECP Mode DMA Channel Selection

System Jumper Setting

| JUMPER | PIN DEFINITION |
|--------|---|
| J7 | Password clear select open (default) short Clear password |
| J33 | Display type select open Mono/EGA/VGA (default) short Color |

Table 2-6. System Jumper Setting

| IRQ PULL UP/PULL DOWN | | |
|-----------------------|-------|---------------------------------------|
| J1 | IRQ14 | 1-2 Pull up (default) |
| J2 | IRQ11 | 2-3 Pull down if PCI card is inserted |
| J34 | IRQ5 | |
| J35 | IRQ9 | |
| J36 | IRQ10 | |

Table 2-7. IRQ Pull Up/Down Jumper Setting

Keyboard Controller Select

| JX3 JUMPER | JX4 JUMPER | FUNCTION |
|------------|------------|--------------------------------------|
| 2-3 | 2-3 | Internal keyboard with PS/2 mouse |
| 1-2 | 2-3 | Illegal |
| 2-3 | 1-2 | Internal keyboard without PS/2 mouse |
| 1-2* | 1-2* | External keyboard controller |

Table 2-8. Keyboard Jumper Setting

| JUMPER | INTERNAL KEYBOARD CONTROLLER WITH PS/2 MOUSE | INTERNAL KEYBOARD CONTROLLER WITHOUT PS/2 MOUSE | EXTERNAL KEYBOARD CONTROLLER |
|--------|--|---|------------------------------|
| J17 | 2-3 | 2-3 | 1-2* |
| RN1 | empty | empty | inserted* |
| RN2 | inserted | empty | empty |
| RN3 | empty | inserted | empty |

* factory default

Table 2-9. Internal/External Keyboard Selection

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

| CONNECTOR | PIN-OUTS | SIGNAL NAME |
|--|--------------------------|--|
| CN1 PS/2 Mouse Connector (Jumper Type) | 1 2 3 4 5 | Mouse data NC Ground + 5V Mouse clock |
| CN2 PS/2 Keyboard Connector | 1 2, 6 3 4 5 | Keyboard data NC Ground + 5V Keyboard clock |
| CN3 Keyboard Connector | 1 2 3 4 5 | Keyboard clock NC Ground + 5V Keyboard clock |
| CN4 PS/2 Mouse Connector (Mini-DIN Type) | 1 2, 6 3 4 5 | Mouse data NC Ground + 5V Mouse clock |

Table 2-10. Connector Pin Definitions (Continued)

| CONNECTOR | PIN-OUTS | SIGNAL NAME |
|-----------------------------------|---|---|
| CN5 Power Connector | 1 2, 10, 11, 12 3 4 5, 6, 7, 8 9 | Power good + 5V + 12V - 12V Ground - 5V |
| CN6 Serial Port 2 Connector | 1 2 3 4 5 | Data carrier detect Receive data Transmit data Data transmit ready Signal ground |
| CN7 Serial Port 1 Connector | 6 7 8 9 | Ready to receive data Request to send data Clear to send Ring indicator |
| CN8 Parallel Port Connector | 1 2-9 10 11 12 13 14 15 16 17 18-25 | LPT strobe Data bit 0 - Data bit 7 LPT acknowledge LPT busy Paper end Selected status Auto line feed LPT error Initiate printer Select printer Ground |
| CN9 FDD Connector | 2 4, 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 1, 3, 5, 7, 9, 11 13, 15, 17, 19 21, 23, 25, 27, 33 | Density select NC Index detection Select motor A Select drive A Select drive B Select motor B Direction control Step pulse Write Data Write enable Track 0 Write protect Read data Head select Disk change Ground |

Table 2-10. Connector Pin Definitions (Continued)

| CONNECTOR | PIN-OUTS | SIGNAL NAME |
|---|---|---|
| J3 External Battery Connector | 1 2, 3 4 | Anode + NC Cathode - |
| J5 Hardware Sleep Connector | 1 2 | Hardware sleep signal Ground |
| J21 Green Power Supply Connector | 1 2 | LED + LED - |
| J22* Green Power Supply Connector | 1 2 | Enable/disable power supply outlet Ground |
| J24 CPU Fan Connector | 1 2 3 | Ground + 12V Ground |
| J25** 3.3V Daughter Board Connector (For 3.3V/3.8V CPU Only) | 1, 3, 14, 16 2, 4, 15, 15 5, 12 6, 11 7, 8, 9, 10 | +3.3V + 5V Voltage switch signal + 12V Ground |
| J28 Speaker Connector | 1 2 3 4 | Speaker signal NC Ground + 5V |
| J29 Keyboard and Power LED Connector | 1, 2 3, 5 4 | Power LED Ground Keyboard lock |
| J30 Reset Switch Connector | 1 2 | Ground Reset signal |
| J31 Turbo Switch Connector | 1 2 | Turbo signal Ground |
| J32 Turbo LED Connector | 1 2 | LED + LED - |

* Insert two-pin connector wires from Green Power Supply into Connector J22.

** If you decide not to use the 3.3V daughter board, the caps on pin 1-2, pin 15-16 should be replaced.

Table 2-10. Connector Pin Definitions

IDE Controller Select

| JUMPER | SPEED 0 | SPEED 1 | SPEED2 |
|--------|---------|---------|--------|
| J14 | 2-3 | 2-3 | 1-2 |
| J16 | 1-2 | 1-2 | 1-2 |

Table 2-11. Local IDE Connector Jumper Setting
(Promise PDC 20230 Only)

| JUMPER | ENABLE LOCAL IDE | DISABLE LOCAL IDE |
|--------|------------------|-------------------|
| J26 | 1-2 | 2-3 |

Table 2-12. Local IDE Connector Jumper Setting

| JUMPER | PIN DEFINITION |
|--------|---|
| J9 | short IDE connector pin27 linked to IOCHRDY signal open IDE connector pin27 open (default) |
| J10 | short IDE connector pin28 linked to BALE signal open IDE connector pin28 open (default) |

Table 2-13. Local IDE Connector Jumper Definitions

| CONNECTOR | PIN-OUTS | SIGNAL NAME |
|-----------------------------------|------------|---------------------|
| J4, J13 HDD_LED Connector | 1 2 | LED + LED - |
| J6 Primary Local IDE Connector | 1 | Reset hard disk |
| | 2, 19, 22 | Ground |
| | 24, 26, 30 | |
| | 40 | HDD7 |
| | 3 | HDD8 |
| | 4 | HDD6 |
| | 5 | HDD9 |
| | 6 | HDD5 |
| | 7 | HDD10 |
| | 8 | HDD4 |
| | 9 | HDD11 |
| | 10 | HDD3 |
| | 11 | HDD12 |
| | 12 | HDD2 |
| | 13 | HDD13 |
| | 14 | HDD1 |
| | 15 | HDD14 |
| | 16 | HDD0 |
| | 17 | HDD15 |
| | 18 | NC |
| | 20, 21, 29 | |
| | 34 | HDD I/O write |
| | 23 | HDD I/O read |
| | 25 | IOCHRDY |
| | 27 | HDD address latched |
| | 31 | IRQ14 |
| | 32 | IOCS16 |
| | 33 | HDD A1 |
| | 35 | HDD A0 |
| | 36 | HDD A2 |
| | 37 | HDD chip select 0 |
| | 38 | HDD chip select 1 |
| | 39 | HDD active |

Table 2-14. Local IDE Connector Pin Definitions

| CONNECTOR | PIN-OUTS | SIGNAL NAME |
|---------------------------------|----------|--|
| CN10 Secondary IDE Connector | 31 | IRQ 15 (The rest are same as J6, page 2-10) |
| J13 HDD_LED Connector | 1 2 | LED + LED - |

Table 2-15. ISA IDE Connector Pin Definitions

| JUMPER | PIN DEFINITION |
|--------|---|
| J8 | short: IDE connector pin27 linked to IOCHRDY signal open: IDE connector pin27 open (default) |
| J11 | short: IDE connector pin28 linked to BALE signal open: IDE connector pin28 open (default) |

Table 2-16. ISA IDE Jumper Definitions

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL7 and SL8, for use with VESA peripherals. The VESA bus connector can be utilized for one Local Bus Master and one Local Bus Slave either (SL7) or (SL8). The following tables give the pin assignments for SL7 and SL8. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV1 and JV2 give more information on settings on the mainboard and the VL-bus controller.

| JUMPER | PIN DEFINITION |
|--------|---|
| JV1 | High speed write select 1-2 One wait write 2-3 Zero wait write (default) |
| JV2 | CPU speed select 1-2 Greater than 33MHz 2-3 Less than or equal to 33MHz (default) |

Table 2-17. VL-Bus Controller Jumper Setting

| SIDE A : PINS AND PIN-OUTS | | SIDE B : PINS AND PIN-OUTS | |
|----------------------------|-----------|----------------------------|-----------|
| 01 | DAT01 | 01 | DAT00 |
| 02 | DAT03 | 02 | DAT02 |
| 03, 10, 17, 24, 35, 43, 51 | Ground | 03 | DAT04 |
| 04 | DAT05 | 04 | DAT06 |
| 05 | DAT07 | 05 | DAT08 |
| 06 | DAT09 | 06, 14, 22, 29, 38, 49, 55 | Ground |
| 07 | DAT11 | 07 | DAT10 |
| 08 | DAT13 | 08 | DAT12 |
| 09 | DAT15 | 09, 20, 32, 57 | VCC |
| 11 | DAT17 | 10 | DAT14 |
| 12, 27, 40, 53 | VCC | 11 | DAT16 |
| 13 | DAT19 | 12 | DAT18 |
| 14 | DAT21 | 13 | DAT20 |
| 15 | DAT23 | 15 | DAT22 |
| 16 | DAT25 | 16 | DAT24 |
| 18 | DAT27 | 17 | DAT26 |
| 19 | DAT29 | 18 | DAT28 |
| 20 | DAT31 | 19 | DAT30 |
| 21 | ADR30 | 21 | ADR31 |
| 22 | ADR28 | 23 | ADR29 |
| 23 | ADR26 | 24 | ADR27 |
| 25 | ADR24 | 25 | ADR25 |
| 26 | ADR22 | 26 | ADR23 |
| 28 | ADR20 | 27 | ADR21 |
| 29 | ADR18 | 28 | ADR19 |
| 30 | ADR16 | 30 | ADR17 |
| 31 | ADR14 | 31 | ADR15 |
| 32 | ADR12 | 33 | ADR13 |
| 33 | ADR10 | 34 | ADR11 |
| 34 | ADR08 | 35 | ADR09 |
| 36 | ADR06 | 36 | ADR07 |
| 37 | ADR04 | 37 | ADR05 |
| 38 | WBACK2-3 | 39 | ADR03 |
| 39 | BE02-3 | 40 | ADR02 |
| 41 | BE12-3 | 41 | NC |
| 42 | BE22-3 | 42 | RESET2-3 |
| 44 | BE32-3 | 43 | DIC2-3 |
| 45 | ADS2-3 | 44 | MIO2-3 |
| 48 | LRDY2-3 | 45 | WIR2-3 |
| 49 | LDEV02-3 | 48 | RDYRTN2-3 |
| 50 | LREQ2-3 | 50 | IRQ9 |
| 52 | LGNT2-3 | 51 | BRDY2-3 |
| 54, 55, 56 | ID2, 3, 4 | 52 | BLAST2-3 |
| 57 | LKEN2-3 | 53, 54 | ID0, 1 |
| 58 | LEADS2-3 | 56 | LCLK0 |
| | | 58 | LBS162-3 |

Table 2-18. SL7 Local Bus Connector Pin Assignment

486-VIP-IO

| SIDE A : PINS AND PIN-OUTS | | SIDE B : PINS AND PIN-OUTS | |
|----------------------------|-----------|----------------------------|-----------|
| 01 | DAT01 | 01 | DAT00 |
| 02 | DAT03 | 02 | DAT02 |
| 03, 10, 17, 24, 35, 43, 51 | Ground | 03 | DAT04 |
| 04 | DAT05 | 04 | DAT06 |
| 05 | DAT07 | 05 | DAT08 |
| 06 | DAT09 | 06, 14, 22, 29, 38, 49, 55 | Ground |
| 07 | DAT11 | 07 | DAT10 |
| 08 | DAT13 | 08 | DAT12 |
| 09 | DAT15 | 09, 20, 32, 57 | VCC |
| 11 | DAT17 | 10 | DAT14 |
| 12, 27, 40, 53 | VCC | 11 | DAT16 |
| 13 | DAT19 | 12 | DAT18 |
| 14 | DAT21 | 13 | DAT20 |
| 15 | DAT23 | 15 | DAT22 |
| 16 | DAT25 | 16 | DAT24 |
| 18 | DAT27 | 17 | DAT26 |
| 19 | DAT29 | 18 | DAT28 |
| 20 | DAT31 | 19 | DAT30 |
| 21 | ADR30 | 21 | ADR31 |
| 22 | ADR28 | 23 | ADR29 |
| 23 | ADR26 | 24 | ADR27 |
| 25 | ADR24 | 25 | ADR25 |
| 26 | ADR22 | 26 | ADR23 |
| 28 | ADR20 | 27 | ADR21 |
| 29 | ADR18 | 28 | ADR19 |
| 30 | ADR16 | 30 | ADR17 |
| 31 | ADR14 | 31 | ADR15 |
| 32 | ADR12 | 33 | ADR13 |
| 33 | ADR10 | 34 | ADR11 |
| 34 | ADR08 | 35 | ADR09 |
| 36 | ADR06 | 36 | ADR07 |
| 37 | ADR04 | 37 | ADR05 |
| 38 | WBACK2-3 | 39 | ADR03 |
| 39 | BE02-3 | 40 | ADR02 |
| 41 | BE12-3 | 41 | NC |
| 42 | BE22-3 | 42 | RESET2-3 |
| 44 | BE32-3 | 43 | DIC2-3 |
| 45 | ADS2-3 | 44 | MIO2-3 |
| 48 | LRDY2-3 | 45 | WIR2-3 |
| 49 | LDEV12-3 | 48 | RDYRTN2-3 |
| 50 | LREQ2-3 | 50 | IRQ9 |
| 52 | LGNT2-3 | 51 | BRDY2-3 |
| 54, 55, 56 | ID2, 3, 4 | 52 | BLAST2-3 |
| 57 | LKEN2-3 | 53, 54 | ID0, 1 |
| 58 | LEADS2-3 | 56 | LCLK0 |
| | | 58 | LBS162-3 |

Table 2-19. SL8 Local Bus Connector Pin Assignment

486-VIP-IO

3.3-Volt Regulator Board Installation

This section describes the installation of the 3.3-volt regulator board used for the IntelDX4 processor. The IntelDX4 processor is a new member of the Intel 486 processor family based on the Intel 486DX2 processor core. It offers features such as System Management Mode (SMM) and Stop Clock Mode ideal for power management function. Its internal core frequency can operate up to maximum of 100MHz. It also operates with a 3.3-volt (Vcc) supply. If the onboard 3.3-volt regulator is not present, the 3.3-volt regulator must be installed before using the IntelDX4 processor. Please refer to the steps below on how to install the 3.3-volt regulator. Please also refer to page 2-2 for the correct CPU jumper selection.

→ **NOTE :** If you do not install the daughter board, you must set connector J25's pin 1-2 and pin 15-16 to be shorted for booting up.

1. Remove jumpers from connector J25.
2. Place the 3.3-volt regulator board as shown on the figure below with the correct pin orientation.

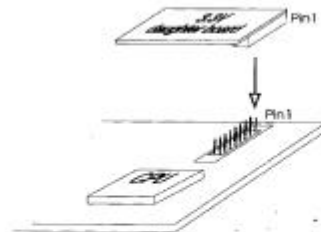


Figure 2-2. 3.3-Volt Regulator Board Installation

Memory Subsystem

The 486-VIP-IO is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

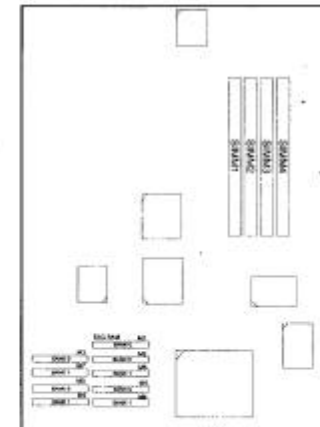


Figure 3-1. Cache and Memory Locations

Installing DRAM

SIMM Banks

The 486-VIP-IO can accommodate onboard memory from 1 to 64MB using SIMMs (Single-In-Line Memory Modules). The mainboard has four memory banks — Bank 0, 1, 2, 3. Each bank can accept either a 1MB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

| TOTAL MEMORY | BANK 0 (72-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) | BANK 3 (72-PIN) |
|--------------|-----------------|-----------------|-----------------|-----------------|
| 1MB | 1MB | | | |
| | | 1MB | | |
| | | | 1MB | |
| 2MB | 1MB | 1MB | | |
| | 1MB | | 1MB | |
| | | | 1MB | 1MB |
| 3MB | 1MB | 1MB | 1MB | |
| | | 1MB | 1MB | 1MB |
| | 1MB | | 1MB | 1MB |
| 4MB | 1MB | 1MB | 1MB | 1MB |
| | 4MB | | | |
| | | 4MB | | |
| 5MB | | | 4MB | |
| | 4MB | 1MB | | |
| | 1MB | 4MB | | |
| | 1MB | | 4MB | |
| | 4MB | | 1MB | |
| | | 1MB | 4MB | |

Table 3-1. DRAM Configurations (Continued)

486-VIP-IO

| TOTAL MEMORY | BANK 0 (72-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) | BANK 3 (72-PIN) |
|--------------|-----------------|-----------------|-----------------|-----------------|
| 6MB | 4MB | 1MB | 1MB | |
| | 1MB | 1MB | 4MB | |
| | 1MB | 4MB | 1MB | |
| | | 4MB | 1MB | 1MB |
| 7MB | 4MB | | 1MB | 1MB |
| | 4MB | 1MB | 1MB | 1MB |
| | 1MB | 4MB | 1MB | 1MB |
| 8MB | 4MB | 4MB | | |
| | 4MB | | 4MB | |
| | | | 4MB | 4MB |
| | | 4MB | 4MB | |
| 9MB | 1MB | 4MB | 4MB | |
| | 4MB | 1MB | 4MB | |
| | 4MB | 4MB | 1MB | |
| | | 1MB | 4MB | 4MB |
| 10MB | 1MB | | 4MB | 4MB |
| | 4MB | 4MB | 1MB | 1MB |
| | 4MB | 4MB | 4MB | |
| 12MB | | 4MB | 4MB | 4MB |
| | 4MB | | 4MB | 4MB |
| 13MB | 1MB | 4MB | 4MB | 4MB |
| | 4MB | 1MB | 4MB | 4MB |
| | 4MB | 4MB | 4MB | 4MB |
| 16MB | 16MB | | | |
| | | 16MB | | |
| | | | 16MB | |
| 17MB | 16MB | 1MB | | |
| | 1MB | 16MB | | |
| | 1MB | | 16MB | |
| | | 16MB | 1MB | |
| | | 1MB | 16MB | |

Table 3-1. DRAM Configurations (Continued)

486-VIP-IO

| TOTAL MEMORY | BANK 0 (72-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) | BANK 3 (72-PIN) |
|--------------|-----------------|-----------------|-----------------|-----------------|
| 18MB | 16MB | 1MB | 1MB | |
| | 1MB | 1MB | 16MB | |
| | 1MB | 16MB | 1MB | |
| | | 16MB | 1MB | 1MB |
| 19MB | 16MB | 1MB | 1MB | 1MB |
| | 1MB | 16MB | 1MB | 1MB |
| 20MB | 16MB | 4MB | | |
| | 4MB | 16MB | | |
| | 4MB | | 16MB | |
| | | 4MB | 16MB | |
| 21MB | 16MB | 4MB | 1MB | |
| | 1MB | 4MB | 16MB | |
| | 1MB | 16MB | 4MB | |
| | 4MB | 1MB | 16MB | |
| 22MB | 16MB | 4MB | 1MB | 1MB |
| | 4MB | 16MB | 1MB | 1MB |
| 24MB | 16MB | 4MB | 4MB | |
| | 4MB | 4MB | 16MB | |
| | 4MB | 16MB | 4MB | |
| 25MB | | 16MB | 4MB | 4MB |
| 28MB | 16MB | 4MB | 4MB | 4MB |
| | 4MB | 16MB | 4MB | 4MB |
| 32MB | 16MB | 16MB | | |
| | | | 16MB | |
| | | | 16MB | 16MB |
| | 32MB* | | | |
| | | | 32MB* | |

Table 3-1. DRAM Configurations (Continued)

| TOTAL MEMORY | BANK 0 (72-PIN) | BANK 1 (72-PIN) | BANK 2 (72-PIN) | BANK 3 (72-PIN) |
|--------------|-----------------|-----------------|-----------------|-----------------|
| 33MB | 16MB | 16MB | 1MB | |
| | 1MB | 16MB | 16MB | |
| | | 1MB | 16MB | 16MB |
| | | | 16MB | 16MB |
| 34MB | 16MB | 16MB | 1MB | 1MB |
| | 1MB | 1MB | 16MB | 16MB |
| 36MB | 16MB | 16MB | 4MB | |
| | 4MB | 16MB | 16MB | |
| | | 4MB | 16MB | 16MB |
| | 4MB | | 16MB | 16MB |
| 37MB | 1MB | 4MB | 16MB | 16MB |
| | 4MB | 1MB | 16MB | 16MB |
| 40MB | 16MB | 16MB | 4MB | 4MB |
| | 4MB | 4MB | 16MB | 16MB |
| 48MB | 16MB | 16MB | 16MB | |
| | | 16MB | 16MB | 16MB |
| 49MB | 1MB | 16MB | 16MB | 16MB |
| 52MB | 4MB | 16MB | 16MB | 16MB |
| 64MB | 16MB | 16MB | 16MB | 16MB |
| | 32MB * | | 32MB * | |

* Double-RAS SIMM

Table 3-1. DRAM Configurations

→ NOTE : Only Banks 0 and 2 can accept double-RAS SIMM. If Bank 0 has a double-RAS SIMM inserted, then Bank 1 should be free of SIMM. Likewise, if Bank 2 has a double-RAS SIMM inserted, then Bank 3 should be free of SIMM.

Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

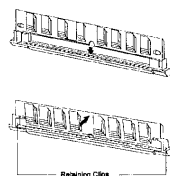


Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMMs, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-VIP-IO can accept cache memory of 128KB, 256KB, 512KB, or 1MB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

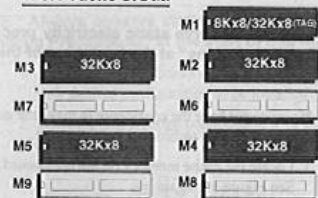
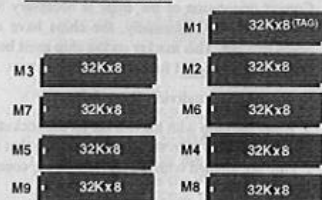
If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard.
See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

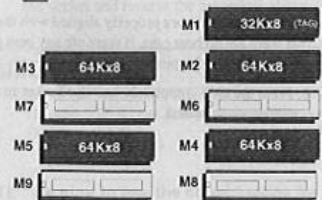
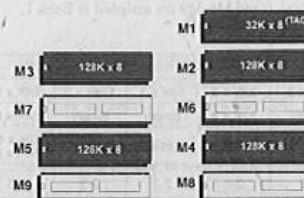
Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

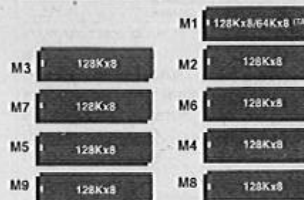
3. Align the chip with the marker on the socket.
Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
 4. Carefully apply enough pressure to partially seat the chip into the socket.
- Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.
5. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings**128K Cache SRAM****256K Cache SRAM**

OR

**512K Cache SRAM**

OR

**1MB Cache SRAM**

The cache size is jumper selectable. M2-M5 are assigned as Bank 0 and M6-M9 are assigned as Bank 1.

| | 128K | | 256K | | 512K | | 1M |
|--------------|--------------------|---------|---------|----------|---------------------|----------------------|----|
| Bank 0 | 32K x 8 | 32K x 8 | 64K x 8 | 128K x 8 | 64K x 8 | 128K x 8 | |
| Bank 1 | Empty | 32K x 8 | Empty | Empty | 64K x 8 | 128K x 8 | |
| Tag RAM (M1) | 8K x 8/ 32K x 8 | 32K x 8 | 32K x 8 | 32K x 8 | 32K x 8/ 64K x 8 | 64K x 8/ 128K x 8 | |
| JS1 (Jumper) | 1-2 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | |
| JS2 (Jumper) | 1-2 | 2-3 | 2-3 | 2-3 | 2-3 | 2-3 | |
| JS3 (Jumper) | 1-2 | 1-2 | 1-2 | 2-3 | 2-3 | 2-3 | |
| JS4 (Jumper) | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 2-3 | |
| JS5 (Jumper) | 1-2 | 1-2 | 1-2 | 2-3 | 2-3 | 2-3 | |
| JS6 (Jumper) | 1-2 | 1-2 | 1-2 | 1-2 | 1-2 | 2-3 | |

Table 3-2. Cache Configuration Size

Award BIOS Setup

The 486-VIP-IO comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

System Setup

A Setup program, built into the system BIOS, is stored in the CMOS RAM that allows the configuration settings to be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

After power-on RAM testing, the message "TO ENTER SETUP BEFORE BOOT, PRESS CTRL-ALT-ESC or " appears. After pressing the above mentioned keys, the following screen appears:

| ROM PCI/ISA BIOS (2A4L4000) STANDARD CMOS SETUP AWARD SOFTWARE, INC. | |
|---|------------------------|
| STANDARD CMOS SETUP | SUPERVISOR PASSWORD |
| BIOS FEATURES SETUP | USER PASSWORD |
| CHIPSET FEATURES SETUP | IDE HDD AUTO DETECTION |
| POWER MANAGEMENT SETUP | SAVE & EXIT SETUP |
| PCI CONFIGURATION SETUP | EXIT WITHOUT SAVING |
| LOAD BIOS DEFAULTS | |
| LOAD SETUP DEFAULTS | |
| Esc : Quit ↑ ↓ → ← : Select Item F10 : Save and Exit Setup (Shift) F2 : Change Color | |
| Time, Date, Hard Disk Type ... | |