

MB838000-20

CMOS 8M-BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The Fujitsu MB838000 is a CMOS Si-gate mask-programmable static read only memory organized as 1,048,576 words by 8bits.

The MB838000 has TTL-compatible I/O 3-state output level with fully-static operation (i.e. no need of clock signal) and single +5v power supply.

Also, the MB838000 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

- Organization: 1,048,576 words x 8bits
- Access time: 200ns max.
- Completely static operation: No clock required
- TTL compatible Input/Output
- Three state output
- Single +5V power supply
- Power dissipation: 257mW max. (Active)
5.5mW max. (Standby, TTL input level)
275μW max. (Standby, CMOS input level)
- 32-pin Plastic DIP: Suffix-p

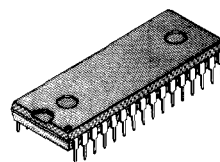
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0 *	V
Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5 *	V
Output Voltage	V_{OUT}	-0.5 to V_{CC} +0.5 *	V
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-45 to +125	°C

* Referenced to GND

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY



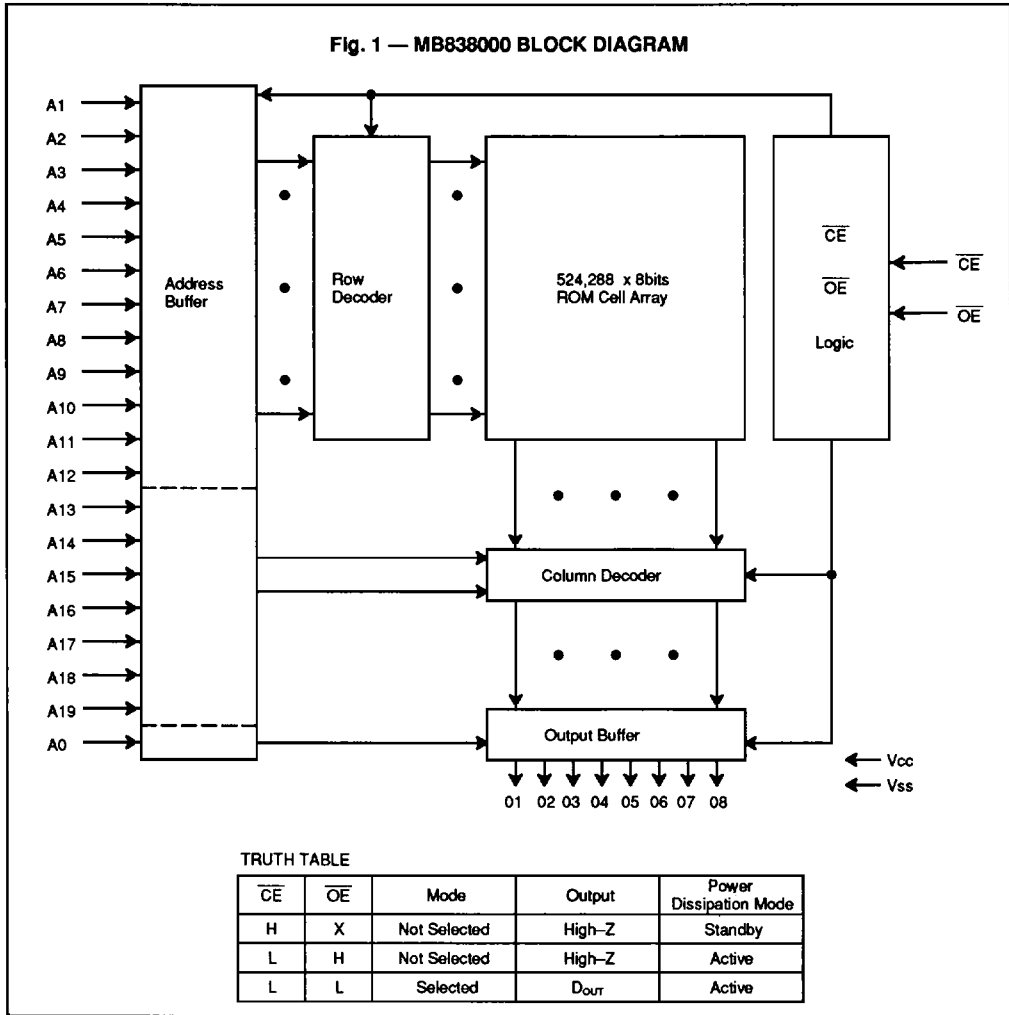
PLASTIC PACKAGE
DIP-32P-M01

PIN ASSIGNMENT

(TOP VIEW)

A19	1	32	V_{CC}
A16	2	31	A18
A15	3	30	A17
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	\overline{OE}
A2	10	23	A10
A1	11	22	\overline{CE}
A0	12	21	O8
O1	13	20	O7
O2	14	19	O6
O3	15	18	O5
V_{SS}	16	17	O4

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.



CAPACITANCE (TA = 25° C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V _{OUT} =0V)	C _{OUT}			15	pF
Input Capacitance (V _{IN} =0V)	C _{IN}			10	pF

RECOMMENDED OPERATING CONDITIONS
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.2		$V_{CC}+0.3$	V
Ambient Temperature	T_A	0		70	°C

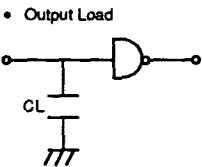
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DC CHARACTERISTICS
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Active Supply Current	$\overline{CE}=V_{IL}$, Minimum Cycle	I_{CC}			50	mA
Standby Supply Current	$\overline{CE}=V_{IH}$	I_{SB1}			1	mA
	$\overline{CE}=V_{CC}=V_{IH1}$, $V_{IN}=V_{SB}$ or V_{CC}	I_{SB2}			50	μA
Input Leakage Current	$V_{IN}=0$ to V_{CC}	I_U	-10		10	μA
Output Leakage Current	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IH}$	I_{LLO}	-10		10	μA
Output High Voltage	$I_{OH}=-400\mu A$	V_{OH}	2.4			V
Output Low Voltage	$I_{OL}=2.1mA$	V_{OL}			0.4	V

Fig. 2 — AC TEST CONDITIONS

- Input Pulse Level : 0.6 to 2.4V
- Input Pulse Rise and Fall Time : $t_r=5ns$
- Timing Reference Levels : Input: $V_{IL}=0.8V$, $V_{IH}=2.2V$
Output: $V_{OL}=0.8V$, $V_{OH}=2.2V$
: 1 TTL Gate and 100pF



AC CHARACTERISTICS

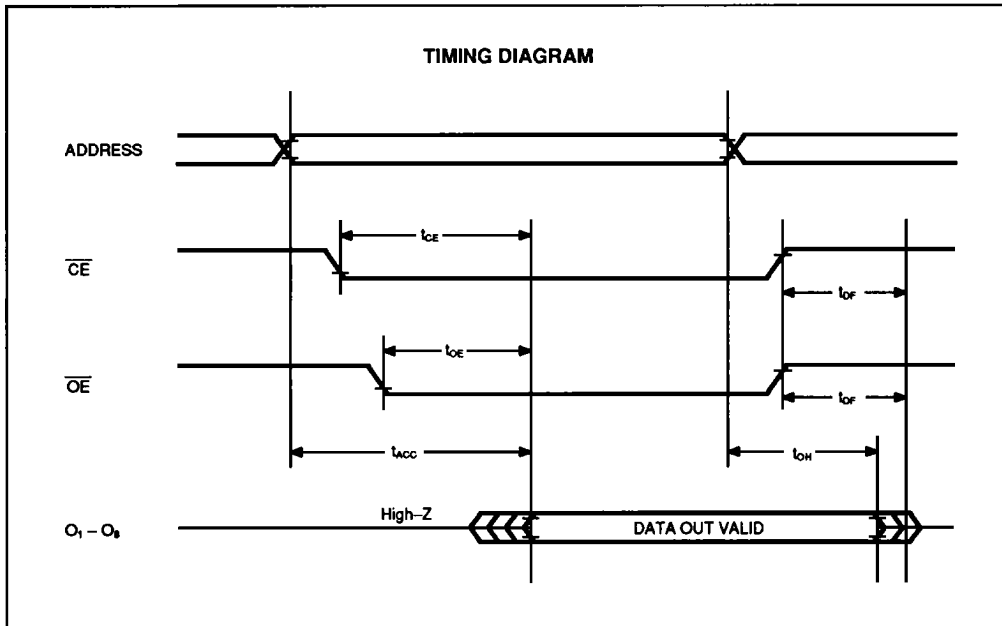
(Recommended operating conditions unless otherwise noted.)

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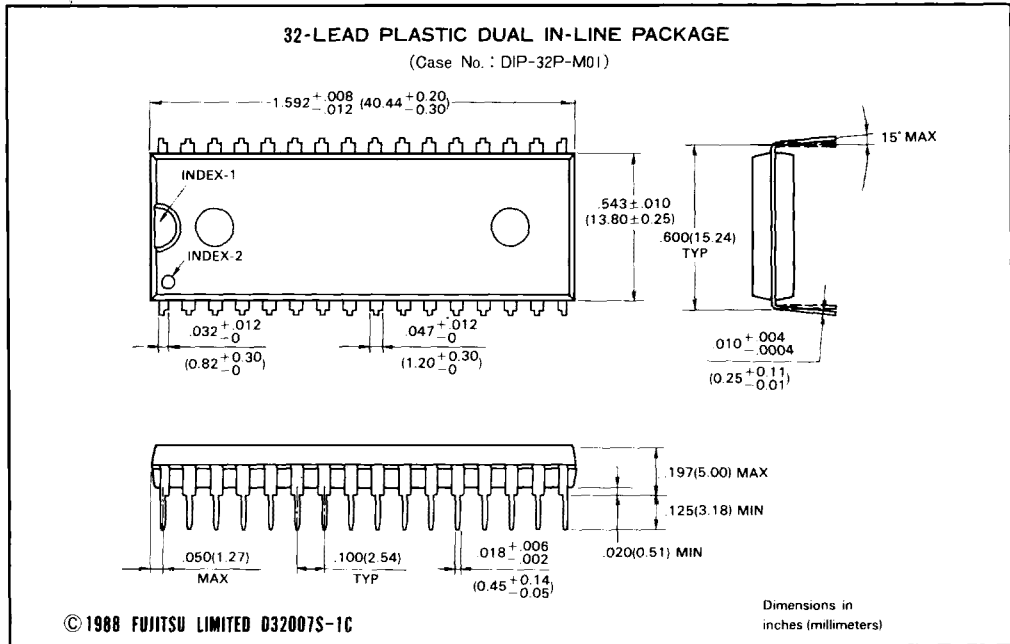
Parameter	Test Condition	Symbol	Min	Max	Unit
Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{acc}		200	ns
Chip Enable Access Time	$\overline{OE}=V_{IL}$	t_{cE}		200	ns
Output Enable Access Time	Note 1	t_{oE}		80	ns
Output Disable Time	Note 2	t_{oF}		60	ns
Output Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	t_{oH}	0		ns

Note 1: Maximum \overline{OE} delay which does not affect t_{acc} is $t_{acc} - t_{oE}$.

Note 2: t_{oF} is specified by either of \overline{CE} or \overline{OE} changing to High earlier.



PACKAGE DIMENSIONS



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