5. PIN DESCRIPTIONS OF MAJOR COMPONENTS

5.4 UMC UM8886-N PCI TO ISA BRIDGE

SYMBOL	TYPE	DESCRPTION
AD{31:0}	I/O	32 BIT PCI ADDRESS AND DATA BUS
C/BE{3:0}	I/O	PCI BUS COMMAND AND BYTE ENABLE SIGNALS
DEVSEL#	I/O	PCI BUS DEVESEL SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
TRDY#	I/O	PCI BUS TRDY SIGNAL. THIS ACTS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
IRDY#	I/O	PCI BUS IRDY SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC ISSUES A CYCLE TO PCI BUS OTHERWISE. IT IS AN INPUT PIN.
FRAME#	I/O	PCI BUS FRAME SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC ISSUES A CYCLE TO PCI BUS OTHERWISE. IT IS AN INPUT PIN.
IDSEL	I	PCI BUS IDSEL INPUT SIGNAL. IDSEL IS USED AS CHIP SELECT DURING CONFIGURATION READ AND WRITE TRANSACTION.
PAR	O	PCI BUS PARITY BIT.
SERR#	I	SYSTEM ERROR. UPON SAMPLING THIS PIN ACTIVE. THE IBC GENERATES AN NMI TO THE CPU.
LOCK#	I	PCI BUS LOCK SIGNAL TO INDICATE LOCK CYCLE.
STOP#	I/O	PCI BUS STOP SIGNAL. THIS ACTS AS AN OUTPUT PIN WHEN THE IBC IS THE SLAVE OF PCI BUS CYCLE TRANSACTION: OTHERWISE. IT IS AN INPUT PIN.
INT{D:A}	I	PCI BUS INTERRUPT REQUEST A. B. C. D.
BCLK	O	ISA BUS CLOCK OUTPUT.
BALE	O	BUS ADDRESS LATCH ENABLE.
SA{19:0}	O	SYSTEM ADDRESS BUS SA{19:0}. SA{19:0} ARE OUTPUT. EXCEPT DURING ISA MASTER CYCLES.
LA{18:17}/ MIRQ{0:1}	I/O	LATCH-ABLE ADDRESS BUS LA{23:17} OR MOTHERBOARD STEERABLE IRQ REQUESTS. IN NORMAL/PNP MODE, LA{23:17} ARE OUTPUT, EXCEPT DURING ISA MASTER CYCLES; IN DOCK/EXPAND MODE, THEY BECOME THE ADDITIONAL IRQ ROUTE WHICH WILL BE STEERED TO INTERNAL 8259S.
LA19/ UNDOCKSMI	I/O	LATCH-ABLE ADDRESS BUS LA19 OR UN-DOCKING REQUEST BY ASSERT SMI#. IN NORMAL/PNP MODE, IT IS LA19; IN DOCK/EXPAND MODE, IT IS ONE OF THE SMI# SOURCE FROM DOCKING STATION FOR USER WANT UN-DOCKING.
LA{23:20}	I/O	LATCH-ABLE ADDRESS BUS LA{23:20}. LA{23:20} ARE OUTPUT/EXCEPT DURING ISA MASTER CYCLES.
SBHE#	O	SYSTEM BUS HIGH ENABLE INDICATES THE HIGH BYTE ON THE ISA DATA BUS SD{15:8} IS VALID.
SD{15:0}	I/O	16 BIT ISA SYSTEM DATA BUS.
IOR#	O	ISA I/O READ COMMAND.
IOW#	O	ISA I/O WRITE COMMAND.
MEMR#	O	ISA MEMORY READ COMMAND.
MEMW#	O	ISA MEMORY WRITE COMMAND.

SYMBOL	TYPE	DESCRPTION
SMEMR#	O	ISA SYSTEM MEMORY READ COMMAND.
SMEMW#	O	ISA SYSTEM MEMORY WRITE COMMAND.
IOCS16#	I	16-BIT I/O. THIS SIGNAL INDICATES THAT BUS SIZE OF CURRENT ISA I/O SLAVE IS 16 BITS.
MEMCS16#	I/O	16-BIT MEMORY. THIS PIN INDICATES THAT THE BUS SIZE OF CURRENT ISA MEMORY SLAVE IS 16 BIT.
0WS#/ACIN	I	NO WAIT STATES. THIS SIGNAL IS ASSERTED BY ISA SLAVE IN ORDER TO SHORTEN THE CYCLE.
IOCHRDY	I/O	CHANNEL READY. IOCHRDY IS USED BY ISA SLAVES TO INSERT WAIT STATES.
MASTER#	I	16-BIT MASTER. INDICATES THAT A 16-BIT ISA MASTER HAS CONTROL OF THE ISA BUS.
AEN	O	ISA BUS AEN SIGNAL. WHEN HIGH. INDICATES THAT DMA OR REFRESH CONTROLS THE ISA BUS.
IOCHCK#/ CLKRUN#	I	I/O CHANNEL CHECK. IBC WILL GENERATE NMI TO CPU UPON SAMPLING THIS PIN ACTIVE; CLKRUN IS RESERVED FOR FUTURE USE.
REFRESH#	I/O	I/O SYSTEM REFRESH CONTROL. OUTPUT TO ISA BUS WHEN CONVERTING SYSTEM TIMER TICKS INTO REFRESH CYCLE.
CPUREQ	I	CPU REQUEST. CPU INITIATOR REQUESTS THE PCI BUS.
CPUGNT	O	CPU GRANT ARBITER HAS GRANTED PCI BUS TO CPU INITIATOR.
REQ0#/ COVERSW#	I	PCI MASTER REQUEST 0. FOR REEQUESTS INITIATED FROM PCI BUS MASTER. COVERSW FROM EXTERNAL LCD COVER SWITCH TO INFORM THE PMU THAT THE LCD COVER HAD BEEN CLOSED SO THAT PMU CAN FORCE SYSTEM TO ENTER SUSPEND MODE.
REQ1#	I	PCI MASTER REQUEST 1.
REQ2#/ 891BUSY#/ DK_REQB# /SDATA2	I	PCI MASTER REQUEST 2 OR DOCKING REQUEST A.. IN NORMAL/PNP MODE, IT IS THE REQUEST INITIATED FROM PCI BUS MASTER OR 891 BUSY IS RESERVED FOR FUTURE USE; IN DOCK/EXPAND MODE, IT IS THE PCI BUS REQUEST FROM DOCKING STATION.
REQ3#/ COVERSW#	I	PCI MASTER REQUEST 3. THIS PIN ALSO ACTS AS "COVERSW" FROM EXTERNAL LCD COVER SWITCH TO INFORM THE PMU THAT LCD COVER HAD BEEN CLOSED SO THAT PMU CAN FORCE SYSTEM ENTER SUSPEND MODE.
GNT0#/ NCLKDC#	O	PCI MASTER GRANT 0. ARBITER HAS GRANTED PCI BUS MASTER OR AS NCLKDC# UM8886N WILL FORCE NCLKDC# LOW TO INFORM UM8891 THAT CPU CLOCK WILL BE DC.
GNT1#	O	PCI MASTER GRANT 0.
GNT2#/ SUSP#/ DK_DACKB #/SDATA3	O	PCI MASTER GRANT 2 OR SUSPEND REQUEST TO CPU FOR STOPPING CPU CLOCK OR DOCK DMA ACKNOWLEDGE B /SERIAL DATA 3. IN NORMAL/PNP MODE, THE ARBITER HAS GRANTED PCI BUS TO PCI BUS MASTER; IN DOCK/EXPAND MODE, IT IS THE ACKNOWLEDGE TO PCI DMA REQUEST FROM DK_DREQB# OR SERIAL DATA OUTPUT TO DOCKING STATION.

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SYMBOL	TYPE	DESCRPTION
GNT3#/ NCLKDC#	O	PCI MASTER GRANT 3. OR NCLKDC# UM 8886N WILL FORCE NCLKDC# TO LOW TO INFORM UM 8891 THAT CPU CLOCK WILL BE D£.
X32K	I	32K CLOCK INPUT.
DREQ{0,1,3}/ MDRQ{2:0}/ MUXSEL{2:0}	I	DMA REQUEST. THESE SIGNALS ARE USED TO REQUEST DMA SERVICE OR TO GRANT CONTROL OF THE EXPANSION BUS TO ISA MASTER. IN NORMAL MODE, THE DREQn ARE NOT STEERABLE; IN PNP/DOCK MODE, THEY ARE STEERABLE TO OTHER DMA CHANNEL REQUEST; IN EXPAND MODE, THEY BECOME THE SELECT SIGNAL OF EXTERNAL DMA REQUEST MULTIPLEXER
DREQ2/ MUXIN	I	DMA REQUEST CHANNEL_2 OR MULTIPLEX INPUT. IN NORMAL/PNP/DOCK MODE, IT IS DMA CHANNEL_2 REQUEST FOR FLOPPY; IN EXPAND MODE, IT IS INPUT FROM THE MULTIPLEXER OUTPUT OF ALL EXTERNAL DMA REQUEST.
DREQ5/ DSPWROK	I	DMA REQUEST CHANNEL_5 OR DOCK STATION POWER OKAY.
DREQ6/ CD#	I	DMA REQUEST CHANNEL_6 OR CARD DETECTED. IN NORMAL/PNP MODE, IT IS DEDICATED AS DMA CHANNEL_6 REQUEST; IN DOCK/EXPAND MODE, IT IS INDICATOR OF THE DOCK-ON.
DREQ7/ DK_REQA#/ SDATA1	I	DMA REQUEST CHANNEL_7 OR DOCKING REQUEST A. IN NORMAL/PNP MODE, IT IS DEDICATED AS DMA CHANNEL_7 REQUEST; IN DOCK/EXPAND MODE, IT IS THE PCI BUS REQUEST FROM DOCKING STATION.
DACK{0,1,3}#/ MDACK{2:0}# /DAC{2:0}	B	DMA ACKNOWLEDGE. THE IBC ASSERTED THESE OUTPUT LINES TO INDICATE THAT THE DMA DEVICE HAS BEEN GRANTED SERVICE. IN NORMAL MODE, THE DACK{0,1,3}# ARE NOT STEERABLE; IN PNP/DOCK MODE, THEY ARE STEERABLE; IN EXPAND MODE, THEY ARE THE ENCODED FROM DACK{3:0,7:5}# DACK3 WILL BE INPUT WHEN RESET FOR SELECTING THE NORMAL/PNP/DOCK/EXPAND MODE
DACK2#/ CD1#	B	DMA ACKNOWLEDGE CHANNEL 2 /CARD DETECT PIN 1.
DACK5#/ ENBUF#	B	DMA ACKNOWLEDGE 5 OE ENABLE THE DOCKING CONNECTOR SIGNAL BUFFERS.
DACK6#/ UNDOCKGNT	B	DMA ACKNOWLEDGE 6 /NOTEBOOK PC UN-DOCKING GRANTED.
DACK7#/ DK DACKA#/ SCLK	O	DMA ACKNOWLEDGE 7 /DOCK DMA ACKNOWLEDGE A /SERIAL CLOCK. IN NORMAL/PNP MODE IT IS DACK7# FUNCTION; IN DOCK/EXPAND MODE IT IS THE ACKNOWLEDGE TO PCI DMA REQUEST FROM DK_DREQA#.
EOP	I/O	END OF PROCESS. IN INPUT MODE. THIS PIN IS USED BY THE DMA DEVICE TO STOP CURRENT DMA TRANSFER. IN OUTPUT MODE. DMA CONTROLLER ASSERTS EOP TO INDICATE TO THE ACTIVE DMA DEVICE THAT THE TRANSFER HAS REACHED THE TERMINAL COUNT.
IRQ1	I	ISA BUS INTERRUPT REQUEST 1.
IRQ{7:3}	I	ISA BUS INTERRUPT REQUEST {7:3}
IRQ8	I	RTC INTERRUPT REQUEST.
IRQ{12:9}	I	ISA BUS INTERRUPT REQUEST {12:9}
IRQ{15:14}	I	ISA BUS INTERRUPT REQUEST {15:14}
INTR	O	MASKABLE INTERRUPT TO CPU.
NMI	O	NONMASKABLE INTERRUPT TO CPU.
SMI#	I/O	SYSTEM MANAGEMENT INTERRUPT. OUTPUT TO CPU TO REQUEST SMM SERVICE. INPUT FROM CPU INDICATES THAT CPU HAS ENTERED SMM MODE.
STPCLK#	O	CPU SLOW DOWN /STOP CLOCK CONTROL.

SYMBOL	TYPE	DESCRPTION
PWRLCH2	O	LATCH SIGNAL TO LATCH PMC OUTPUT PINS FROM SD{7:0} TO GENERATE PMC0-5, PMC8 AND CKGENPD.
PWRLCH1	O	LATCH SIGNAL TO LATCH PMC OUTPUT PINS FROM SD{7:0} TO GENERATE PMC6, PMC7/SUSP, PMC8, PMC9 AND CLKSEL{2:0}.
EXTSMI#	I	EXTERNAL SMI1.
SMIACT#	I	SYSTEM MANAGEMENT INTERRUPT ACKNOWLEDGE FROM INTEL SL ENHANCED CPU.
PCICLKI	I	PCI BUS CLOCK INPUT TO THE IBC.
CLKIN	I	OSCILLATOR CLOCK INPUT TO GENERATE CPU AND PCICLOCKS.
OSC	I	TIME BASE 14.318 MHZ CLOCK INPUT.
HCLK	O	CLOCK OUTPUT TO CPU HOST.
PCICLK0	O	CLOCK OUTPUT TO PCI BUS.
CPURST	O	CPU RESET. THIS PIN IS USED TO INITIALIZE CPU.
RSTDRV	O	RSTDRV. THIS PIN IS USED TO RESET ENTIRE SYSTEM, EXCEPT THE CPU.
KBCLK	I/O	KEYBOARD CONTROLLER CLOCK. CLOCK OUTPUT TO THE 8742.
RC/PGP0	I/O	RESETS INPUT FROM 8042, OR ACTS AS PROGRAMMABLE INPUT, OR OUTPUT PIN 0.
GA20/PGP1/ LDEV#	I/O	ADDRESS A20 GATE FROM 8042. OR ACTS AS PROGRAMMABLE INPUT/OUTPUT PIN 1. OR ACTS AS LOCAL DEVICE INPUT FROM VL BUS.
ROMCS#/ KBCS#	O	ROMCS AND KBCS. DUAL FUNCTION PIN. FOR I/O CYCLES, THIS PIN IS KBCS: FOR MEMORY CYCLES, IT IS ROMCS.
SPKR	O	SPEAKER DRIVE OUTPUT.
XDEN/PGP3/ TCRAMWR	O	XD BUS DIRECTION CONTROL. OR ACTS AS PROGRAMMABLE OUTPUT PIN 3. OR AS TCRAMWR TO READ/WRITE EXTERNAL 4KB RTC.
RTCAS	O	RTC ADDRESS LATCH.
RTCWR	O	RTC WRITE COMMAND.
RTCRD	O	RTC READ COMMAND.
IDE1FX	O	IDE 1FX CHIP SELECT.
IDE3FX	O	IDE 3FX CHIP SELECT.
ONOFF#/ ACIN	I	"ON/OFF" SWITCH INPUT TO PMU. SWITCHES BETWEEN FULL-ON MODE AND SUSPEND MODE OR ACTS AS ACIN.
LB1/LB2	I	LOW BATTERY 1 OR LOW BATTERY 2 INPUT.
IDE17X/ PGP3	O	IDE 17X CHIP SELECT. OR ACTS AS PROGRAMMABLE OUTPUT PIN 3.
IDE37X/ PGP2	O	IDE 37X CHIP SELECT. OR ACTS AS PROGRAMMABLE OUTPUT PIN 2.
IDEHDEN	O	ENABLE IDE CYCLE.
A20M	O	MASK PROCESSOR ADDRESS 20: ACTIVE WHEN GA20 IS LOW OR I/O PORT 92H BIT 1 IS HIGH.
EXSMI2/LB2 /KBCLKI	I	EXTERNAL SMI INPUT 2 OR ACTS AS LOW BATTERY 2 INPUT OR KEYBOARD CLOCK INPUT.
FERR#	I	WHEN LOW INDICATES THAT A FLOATING POINT ERROR HAS OCCURRED.
IGNNE#	O	IGNNE IS ASSERTED LOW TO INSTRUCT THE CPU TO IGNORE A NUMERIC ERROR AND CONTINUE EXECUTING NON-CONTROL FLOATING POINT INSTRUCTIONS.
TEST	I	THIS PIN USED FOR TESTING ONLY FOR NORMAL OPERATION IT SHOULD BE PULLED HIGH.
VCC5		+5V VOLT POWER SUPPLY.
VCC3		3.3-VOLT POWER SUPPLY.