KDA0471/0476/0478

CMOS RAMDACs™
Preliminary

FEATURES

- Triple 6 or 8-bit High Performance D-to-A Converters
- 50, 66, 80, 100 and 120 MHz Operation
- Personal System/2® Compatible
- "Snow-Free" Operation
- 256 Word Color Palette SRAM
- 15 x 18 Overlay Palette SRAM (KDA0471)
- 15 x 24 Overlay Palette SRAM (KDA0478)
- RS343A/RS170 Compatible Outputs
- Sync on All Three Channels (KDA0471/0478)
- Standard MPU Interface
- External Voltage or Current Reference
- Programmable Pedestal (KDA0471/0478)
- Single +5 Volt Power Supply
- 44-Pin PLCC, 32-Pin PLCC, 28-Pin (600 mil) DIP Package

DESCRIPTION

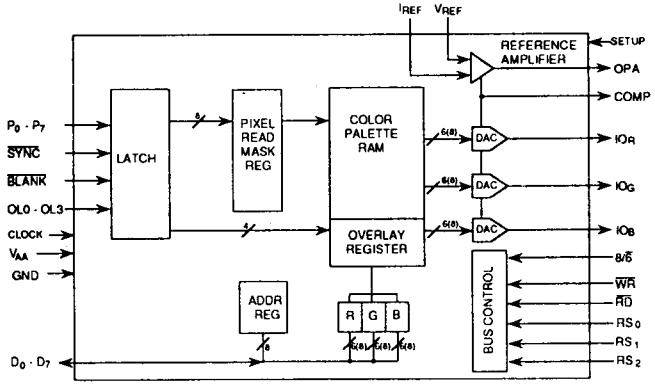
The KDA0471, KDA0476 and KDA0478 RAM DACs are designed using Samsung's single poly double metal, 1 micron CMOS technology for high resolution color graphics. These RAM DACs support Personal System/2 compatible color graphic applications. The KDA0471 and KDA0478 come in a 44-pin PLCC package. The KDA0476 comes in 32, 44-pin PLCC and 28-pin 600 mil DIP

The KDA0471 contains a 256 x 18 look up table and three 6-bit video D-to-A converters. The KDA0476 is similar to the KDA0471 except that it does not contain overlays or sync information on the analog outputs. The KDA0478 contains a 256 x 24 bit color palette and three 8-bit video D-to-A converters, which may be configured for either 6-bit or 8-bit D-to-A converter operation.

The KDA0471 and KDA0478 contain 15 overlay registers which support overlaying of cursors, grids, menus, and EGA emulation. These two devices also support generation of sync signal on all three channels, and programmable pedestal (0 or 7.5 IRE). In addition, they allow use of an external voltage reference or an external current reference.

The KDA0471/0476/0478 generate RS-343A compatible red, green and blue video outputs capable of directly driving a doubly-terminated 75Ω coax cable, and RS-170 compatible video outputs capable of driving singly-terminated 75Ω cable without the need for external buffers.

FUNCTIONAL BLOCK DIAGRAM



APPLICATION

- High Resolution Color Graphics
- CAD/CAM/CAE Applications
- Image Processing
- Desktop Publishing

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PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
RS0, RS1, RS2	I	**Register Select Inputs.** These inputs specify the type of read or write operation being performed as shown in Tables 2 and 3. (TTL compatible)
D0–D7	I/O	**Data Bus.** MPU data is transferred over this bus in both directions. (TTL compatible)
$\overline{WR}$	I	**Write Control Inputs.** Data (D0–D7) is latched on the rising edge of $\overline{WR}$ signal. RS0–RS2 are latched on the falling edge of $\overline{WR}$ during MPU write operations. (TTL compatible)
$\overline{RD}$	I	**Read Control Inputs.** $\overline{RD}$ must be at logic zero level for reading data from the device. RS0-RS2 are latched on the falling edge of the $\overline{RD}$ during MPU read operations. (TTL compatible)
*8/$\overline{6}$	I	**6-bit or 8-bit DAC Select Input.** With logic one on this signal, the MPU performs 8-bit operations and D7 is the MSB. With logic zero on this input, the MPU performs 6-bit operations and D5 is the MSB. (TTL compatible)
$\overline{BLANK}$	I	**Composite Blank Control Input.** A logic zero on this input will drive analog outputs to the blanking level (see Tables 5 and 6). This is latched on the rising edge of CLOCK. When the $\overline{BLANK}$ is at logic zero, the pixel and overlay inputs are ignored. (TTL compatible)
SETUP	I	**SETUP Control Input.** SETUP is used to specify either a 0 IRE or 7.5 IRE blanking pedestal operation mode.
**$\overline{SYNC}$	I	**Composite Sync Control Input.** A logic zero on this input will switch off a 40 IRE current source on the analog outputs (shown in Figures 1 and 2). As stated before, the $\overline{SYNC}$ does not override any other control or data input, so it must be activated only during the blanking interval. $\overline{SYNC}$ is latched on the rising edge of the CLOCK. When $\overline{SYNC}$ is not required on the analog output, it should be connected to ground. (TTL compatible)
P0 – P7	I	**Pixel Select Inputs.** These inputs specify one of the 256 color data entries in the color palette RAM to be used for color information. (TTL compatible)
**OL0 – OL3	I	**Overlay Select Inputs.** These inputs specify the palette to be used for color information. When accessing the overlay palette, the pixel inputs P0-P7 are ignored. OL0 is the LSB. See Table 4. (TTL compatible)
CLOCK	I	**CLOCK Input.** The data P0-P7, OL0-OL3, $\overline{SYNC}$ and $\overline{BLANK}$ inputs are latched on the rising edge of the clock. The input should be driven by a TTL buffer. (TTL compatible)
COMP	I	**Compensation Pin.** When using an external voltage reference, this pin should be connected to OPA. When using an external current reference, this pin should be connected to I_{REF}. A bypass capacitor of 0.1μF with shortest possible lead lengths should be connected between this pin and V_{AA}. (See figures 3 and 4)
IOR, IOG, IOB	O	**Red, Green and Blue Current Outputs.** These high impedance current sources are capable of directly driving a doubly-terminated 75Ω coaxial cable. (See figures 3 and 4)
V_{REF}	I	**Voltage Reference Input.** The external reference voltage, if used, must be applied to this input (Reference voltage is 1.2V). When external current reference is used, this input must be left open except for the bypass capacitor. A bypass capacitor of 0.1μF with shortest possible lead lengths should be connected between this pin and the V_{AA}. (See figures 3 and 4)

PIN DESCRIPTIONS (Continued)

SYMBOL	TYPE	DESCRIPTION
I_{REF}	I	**Full Scale Adjust Control.** This setting will not change the I_{REF} relationship shown in Figures 1 and 2. When external voltage reference is used, the magnitude of the full scale video output is controlled by the resistor R_{SET} which is connected between the I_{REF} and GND pins. The relationship between the R_{SET} and full scale output current on each output is given by: $R_{SET} = K * 1000 * V_{REF}/I_{OUT}$ (R_{SET} in Ohms, recommended 147Ω. V_{REF} in Volts, and I_{OUT} in mA). When external current reference is used, the relation between I_{REF} and the full scale output current on each output is: $I_{REF} = I_{OUT}/K$ I_{OUT} in mA. Constant K is listed on Table 1 for 37.5 ohms loads
OPA	I	**Reference Amplifier Output.** Connected to COMP when an external voltage reference is used, and left open when external current reference is used.
V_{AA}		**Analog Power.** All V_{AA} pins must be connected together.
GND		**Analog Ground.** All GND pins must be connected together.

* This pin is not available on the KDA0471/0476
* These pins are not available on the KDA0476

Table 1. Constant K for 37.5Ω Loads

Part	Mode	Pedestal	K
KDA0478	6-bit	7.5 IRE	3.170
	8-bit	7.5 IRE	3.195
	6-bit	0 IRE	3.000
	8-bit	0 IRE	3.025
KDA0471	(6-bit)	7.5 IRE	3.170
		0 IRE	3.000
KDA0476	(6-bit)	0 IRE	2.100

FUNCTIONAL DESCRIPTION

RAM DAC Data Bus

KDA0471, KDA0476

The internal data bus is only 6 bits wide and the lower 6 bits of the 8 bit input bus contain the color data. In this case, D0 is the LSB and D5 is the MSB of the color data. Data bits D6 and D7 are ignored during write cycle and they are logical zero during read cycle.

KDA0478

The function of the control input "8/$\overline{6}$" on this device is to specify whether the MPU reads and writes 8 bits of data or 6 bits of data in each cycle. With logical one on this signal, the data bus is 8 bits wide and with logical zero on this signal, the data bus is 6 bits wide. For 8-bit operation, the data bit D0 is the LSB and the data bit D7 is the MSB of the color data.

Microprocessor Interface

The KDA0471/0476/0478 devices support standard microprocessor interfaces which allows a microprocessor to access the color palette RAM and overlay registers. Microprocessor can access the address register, color palette RAM, overlay registers or read mask register and the selection is done by the RS0 to RS2 selection inputs shown in Table 2. The 8-bit address register is used to address the color palette RAM and overlay reigsters, without requiring any external address multiplexers. The data bit D0 is the LSB and it corresponds to the address bit ADDR0.

Table 2. Control Input Truth Table

RS2	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Reserved

Writing Data into the Color Palette RAM

For writing data into the color palette, the MPU must first write the address of the color palette location to be modified into the address register during the RAM Write Mode. The MPU will have to perform three successive write cycles each, one for red, green and blue color, using RS0 to RS2 to select the color palette RAM. The cycles may be 6-bit or 8-bit wide. After the last (blue) write cycle, all three bytes of color information are combined internally to make a 24-bit word (18-bit word in case of KDA0471/0476) and written to the RAM location given by the address register. The address register is auto-incremented to the next location. This allows consecutive update of the color palette locations, for which the MPU can continue supplying sequences of red, green and blue data until the entire block has been written.

Reading Data from the Color Palette RAM

For reading data from the color palette, the MPU must first load the address register with the address of the color palette RAM location to be read, during the RAM Read Mode. The color contents from this location are copied into the RGB registers and the address register is incremented to the next location. The MPU will have to perform three successive read cycles (6 or 8 bit) each for red, green and blue color selecting RS0 to RS2 bits for color palette RAM. After the last (blue) read cycle, the contents of the specified color palette RAM location are copied into the RGB registers and the address register is once more auto- incremented. This allows reading consecutive locations of the color palette. In this way, the MPU continues to perform red, green, and blue read cycles until a block has been read.

Writing Color Data into the Overlay Registers

For writing data into overlay registers, the MPU must first write the address of the overlay register location to be modified into the address register, during the Overlay Write Mode. The MPU will have to perform three successive write cycles each one for red, one for green and one for blue color using RS0 to RS2 to select overlay registers. The cycles may be 6-bit or 8-bit wide. After the last (blue) write cycle, all three bytes of color information are combined internally to make a 24-bit word (18-bit word in case of KDA0471/0476) and written to the overlay register location given by the address register. The address register is auto-incremented to the next location. As stated before, it is possible to update consecutive locations of the overlay register. For this, the MPU can continue supplying sequence of red, green and blue data until the entire block has been written.

Reading Data from the Overlay Registers

For reading data from the overlay registers, the MPU must first load the address register with the address of the overlay register location to be read, during the Overlay Register Read Mode. The color contents from this location are copied into the RGB registers and the address register is auto-incremented to the next location. The MPU will have to perform three successive read cycles (6 or 8 bit) each for red, green and blue color using RS0 to RS2 bits to select overlay registers. After the last (blue) read cycle, the contents of the specified overlay register location are copied into the RGB registers and the address register is once more incremented. As stated before, the MPU can perform continuous block read simply by specifying the block start address and then continuously reading red, green, blue cycles until the entire block has been read.

When accessing the color palette RAM, the address register will reset to $00 following a blue read or write cycle to RAM location $FF. When accessing the overlay registers, the address bits ADDR4 to ADDR7 (four MSBs) are ignored.

The operation of the MPU interface is asynchronous with respect to the pixel clock. The internal logic will synchronize data transfers between the color palette RAM, overlay registers and the R,G,B color registers. These data transfers occur in between accesses by the MPU.

"Snow-Free" Operation

In most equivalent RAM DACs, frequent accesses (Reads or Writes) to the look-up table RAM or overlay registers (e.g. Block writes) during display refresh result in noticeable disturbances on the screen. This is referred to as "Snow". To avoid this, programmers resorted to polling for the blanking interval to make such accesses. This results in less than optimum system performance.

Samsung's unique design of the KDA0471/0476/0478 RAM DACs frees the programmer from this restriction. Any number of continuous accesses to the look-up table RAM and overlay registers can be made during screen refresh, without snow disturbances.

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Table 3. Address Register Operation

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa,b	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00-$FF XXXX0000 XXXX0001 : : : : XXXX1111	0 1 1 1	0 0 0 0	1 1 1 1	color palette RAM reserved overlay color 1 : : : : overlay color 15

Table 4. Pixel and Overlay Control Truth Table

OL0-OL3	P0-P7	Addressed by Frame Buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Address Register Operation

There are two bits ADDRa and ADDRb in the address register whose function is to keep track of the red, green and blue read and write cycles. These two bits are only reset to zero when the MPU writes to the address register and the MPU does not have access to them. The MPU can access the eight bits ADDR0 to ADDR7 which are used to address the color palette RAM and overlay registers as shown in Table 3. The MPU can read the address register at any time without modifying its contents or modifying the read/write mode.

Graphics Controller Interface

On this interface, the pixel inputs P0 to P7, and overlay bits OL0 to OL3 are used to address the color palette RAM and overlay registers as shown in Table 4. These inputs are updated from the graphics controller as shown in the application example. Also, $\overline{BLANK}$ and $\overline{SYNC}$ signals are provided by the VGA controller. The data bit D0 of the pixel read mask register corresponds to pixel input P0. The color palette location addressed by the pixel/overlay inputs, provides 24 bits of color information to three DACs. In the case of the KDA0471/0476, these are 18 bits.

As illustrated in figures 1 and 2, the $\overline{SYNC}$ and $\overline{BLANK}$ inputs are latched on the leading edge of the clock to;

1. keep synchronization with the color data
2. add weighted currents to the analog outputs and
3. generate specific output level for video applications.

Modifications of the output levels by these signals are shown in Tables 5 and 6.

The SETUP input specifies whether 0 IRE or 7.5 IRE blanking pedestal is used.

SETUP = GND for 0 IRE
SETUP = V_{AA} for 7.5 IRE

The analog outputs of all three devices are capable of directly driving a 37.5Ω load without any buffering.

Table 5. Video Output Truth Table (SETUP = V_{AA})

Item	KDA0471/0478 I_{OUT} (mA)	SYNC	BLANK	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA-SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK-SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$XX
SYNC	0	0	0	$XX

Doubly-terminated load of 75Ω, SETUP = V_{AA}, V_{REF} = 1.235V, R_{SET} = 147 Ω

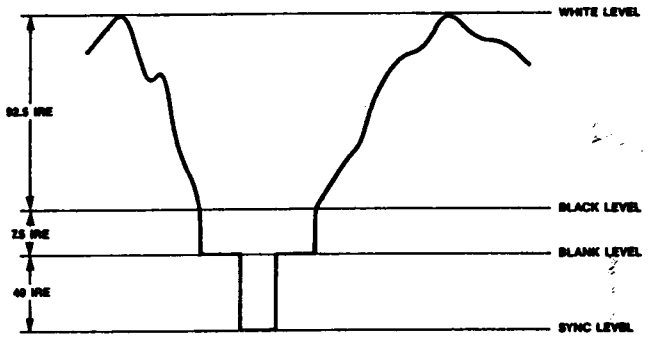
Table 6. Video Output Truth Table (SETUP = GND)

Item	KDA0476 I_{OUT} (mA)	KDA0471/0478 I_{OUT} (mA)	SYNC	BLANK	DAC Input Data
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA-SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK-SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$XX
SYNC	0	0	0	0	$XX

Doubly-terminated load of 75Ω, SETUP = GND, V_{REF} = 1.235V, R_{SET} = 147 Ω

Figure 1. Composite Video Output Waveforms (SETUP = V_{AA})

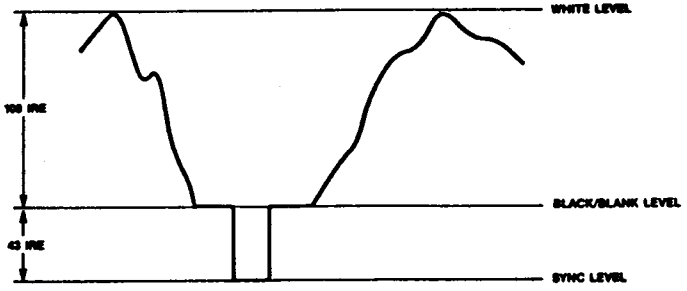
KDA0471/0478 W/O SYNC		KDA0471/0478 W/ SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75Ω doubly-terminated load, SETUP = V_{AA}. V_{REF} = 1.235V, R_{SET} = 147Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms (SETUP = GND)

KDA0476 OR KDA0471/0478 W/O SYNC		KDA0471/0478 W/ SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75Ω doubly-terminated load, SETUP = GND. V_{REF} = 1.235V, R_{SET} = 147Ω. RS-343A levels and tolerances assumed on all levels.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply 80, 66 MHz Parts 50, 35 MHz Parts	V_{AA}	 4.75 4.50	 5.00 5.00	 5.25 5.50	 V V
Ambient Operating Temperature	T_A	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration Reference Voltage	V_{REF}	1.14	1.235	1.26	V
Current Reference Configuration I_{REF} Current Standard RS-343A PS/2 Compatible	REF	 –3 –3	 –8.39 –8.88	 –10 –10	 mA mA

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Typ	Max	Units
V_{AA} (measured to GND)				7.0	V
Voltage on Any Digital Pin		GND – 0.5		V_{AA} + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	I_{SC}		indefinite		
Ambient Operating Temperature	T_A	–55		+125	°C
Storage Temperature	T_S	–65		+150	°C
Junction Temperature	T_J			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	T_{SOL}			260	°C
Vapor Phase Soldering (1 minute)	T_{VSOL}			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
KDA0478		8	8	8	Bits
KDA0471/0476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	I_L				
KDA0478				±1	LSB
KDA0476				±1/2	LSB
KDA0471				±1/4	LSB
Differential Linearity Error	D_L				
KDA0478				±1	LSB
KDA0476				±1/2	LSB
KDA0471				±1/4	LSB
Gray Scale Error				±5	%Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{AA} + 0.5	V
Input Low Voltage	V_{IL}	GND – 0.5		0.8	V
Input High Current (V_{IN} = 2.4V)	I_{IH}			1	µA
Input Low Current (V_{IN} = 0.4V)	I_{IL}			–1	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4V)	C_{IN}			7	pF
Digital Outputs					
Output High Voltage (I_{OH} = –400µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}			0.4	V
Three-State Current	I_{OZ}			50	µA
Output Capacitance	CD_{OUT}			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
KDA0471/0478					
SETUP = V_{AA}		0.95	1.44	1.90	mA
SETUP = GND		0	5	50	µA
KDA0476		0	0	0	µA
Blank Level					
KDA0471/0478		6.29	7.62	8.96	mA
KDA0476		0	5	50	µA
Sync Level (KDA0471/0478 only)		0	5	50	µA
LSB Size					
KDA0478 (8/$\overline{6}$ = logical one)			69.1		µA
KDA0471/0476			279.68		µA
DAC to DAC Matching			2	5	%
Output Compliance	V_{OC}	–1.0		+1.5	V
Output Impedance	RA_{OUT}		10		KΩ
Output Capacitance	CA_{OUT}			30	pF
(f = 1MHz, I_{OUT} = 0mA)					
Voltage Reference Input Current	I_{VREF}		10		µA
Power Supply Rejection Ratio (COMP = 0.1µF, f = 1KHz)	PSRR			0.5	%/%ΔV_{AA}

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V, SETUP = V_{AA}, 8/$\overline{6}$ = logical one. For 28-pin DIP version of the KDA0476, I_{REF} = –8.39mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

* Since the KDA0471 and KDA0476 have 6-bit DACs (and the KDA0478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

Analog Output Levels — PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
KDA0471/0478					
SETUP = V_{AA}		1.01	1.51	2.00	mA
SETUP = GND		0	5	50	µA
KDA0476		0	5	50	µA
Blank Level					
KDA0471/0478		6.6	8	9.4	mA
KDA0476		0	5	50	µA
Sync Level (KDA0471/0478 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with R_{SET} = 140Ω, V_{REF} = 1.235V, SETUP = V_{AA}, 8/$\overline{6}$ = logical one. For 28-pin DIP version of the KDA0476, I_{REF} = –8.88mA.

AC CHARACTERISTICS

Parameter	Symbol	80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	f_{MAX}			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus Three-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	$4*t_{CLK}$			$4*t_{CLK}$			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (t_{CLK})	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV-sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
V_{AA} Supply Current **	I_{AA}		180	200		180	200	mA

Note:

* "Recommended Operating Conditions" using external voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V, SETUP = V_{AA}, 8/$\overline{6}$ = loigcal one For 28-pin DIP (KDA0478), I_{REF} = –8.39mA and TTL input values are 0 to 3 volts with input rise/fall times ≤ 3ns (measured between 10% and 90% points). The timing reference points at 50% for inputs and outputs. Analog output load ≤ 10pF, D0–D7 output load ≤ 50pF. (Refer to timingchart — figure 7)

** At f_{MAX} · I_{AA} (typ) at V_{AA} = 5.0V. I_{AA} (max) at V_{AA} (max).

AC CHARACTERISTICS

Parameter	Symbol	50 MHz Devices			35 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	f_{MAX}			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus Three-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	$4*t_{CLK}$			$4*t_{CLK}$			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (t_{CLK})	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV-sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
V_{AA} Supply Current **	I_{AA}		170	200		170	200	mA

Note:

* "Recommended Operating Conditions" using external voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V, SETUP = V_{AA}, 8/$\overline{6}$ = loigcal one. For 28-pin DIP (KDA0478), I_{REF} = –8.39mA and TTL input values are 0 to 3 volts with input rise/fall times ≤ 3ns (measured between 10% and 90% points). The timing reference points at 50% for inputs and outputs. Analog output load ≤ 10pF, D0–D7 output load ≤ 50pF. (Refer to timing chart — figure 7).

** At f_{MAX} · I_{AA} (typ) at V_{AA} = 5.0V. I_{AA} (max) at V_{AA} (max).

AC CHARACTERISTICS

Parameter	Symbol	120 MHz Devices			100 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	f_{MAX}			120			100	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
$\overline{RD}$ Asserted to Data Bus Driven	3	5			5			ns
$\overline{RD}$ Asserted to Data Valid	4			40			40	ns
$\overline{RD}$ Negated to Data Bus Three-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	9	50			50			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	10	$4*t_{CLK}$			$4*t_{CLK}$			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (t_{CLK})	13	8.33			10			ns
Clock Pulse Width High Time	14	4			4			ns
Clock Pulse Width Low Time	15	4			4			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV-sec
DAC to DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
V_{AA} Supply Current **	I_{AA}		180	200		180	200	mA

Note:

* "Recommended Operating Conditions" using external voltage reference with R_{SET} = 147Ω, V_{REF} = 1.235V, SETUP = V_{AA}, $8/\overline{6}$ = logical one. For 28-pin DIP (KDA0478), I_{REF} = –8.39mA and TTL input values are 0 to 3 volts with input rise/fall times ≤ 3ns (measured between 10% and 90% points). The timing reference points at 50% for inputs and outputs. Analog output load ≤ 10pF, D0–D7 output load ≤ 50pF. (Refer to timing chart — figure 7).

** At f_{MAX} · I_{AA} (typ) at V_{AA} = 5.0V. I_{AA} (max) at V_{AA} (max).

PC BOARD LAYOUT CONSIDERATIONS

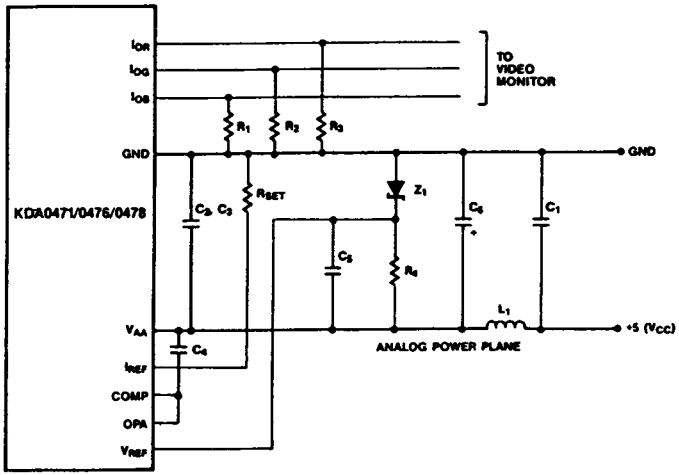
The digital inputs have to be shielded and decoupled so that noise is excluded from the power and ground lines (KDA0471/0476/0478). In addition, the lead length between the power and ground pins should be minimized to eliminate inductive ringing. The analog power should be connected to the PCB power plane (V_{CC}) through a single ferrite bead (refer to Figures 3, 4 and 5). This ferrite bead should be located within 3 inches of the KDA0471/0476/0478.

Note that the PCB power plane should provide the digital logic, and the analog power to all KDA0471/0476/0478 power pins and V_{REF} and I_{REF} circuitry. For better performance, bypass capacitors with the shortest leads, should be used to decouple the two groups of V_{AA} pins to ground (0.1μF ceramic capacitor). Refer to figures 3, 4 and 5 for noise free connection and external voltage and external current reference connections.

Finally, the video DACs output signals should also be terminated properly with the video monitor. The DAC being a current source should be doubly terminated with a 75 ohms resistor, one at each output of the DAC pin, and another at the input of the video monitor. This DAC termination method will avoid ringing and reflections in the cable as the speed increases (refer to figure 3).

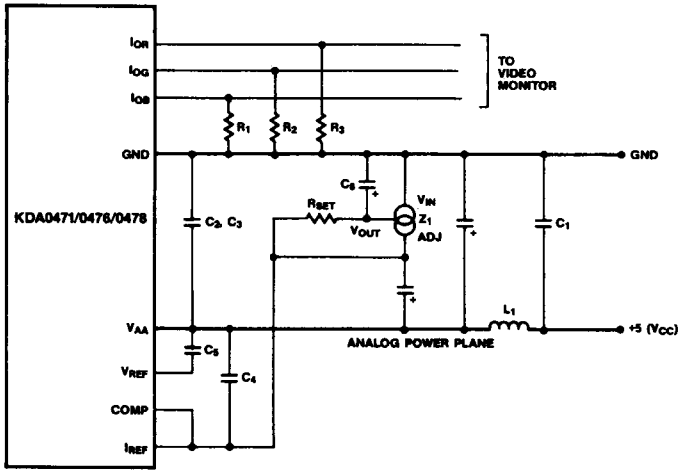
2

Figure 3. Connection Diagram (External Voltage Reference)



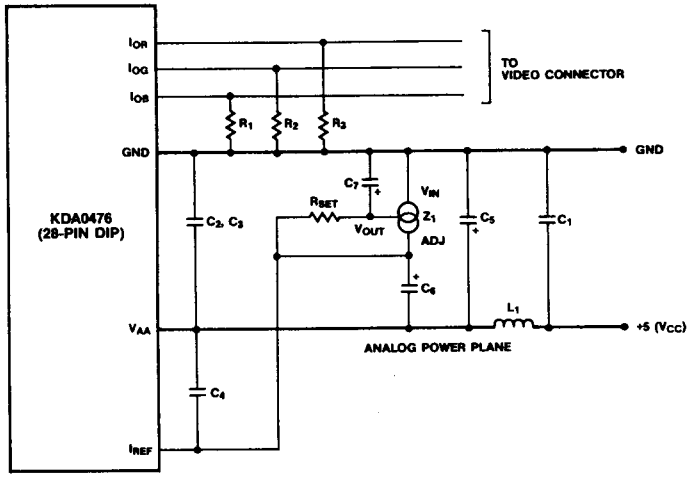
Location	Description
C1–C5	0.1μF ceramic capacitor
C6	10μF tantalum capacitor
L1	ferrite bead
R1, R2, R3	75Ω 1% metal film resistor
R4	1KΩ 5% resistor
R_{SET}	147Ω 1% metal film resistor
Z1	1.2V voltage reference

Figure 4. Connection Diagram (External Current Reference)



Location	Description
C1–C5	0.1μF ceramic capacitor
C6	10μF tantalum capacitor
C7	47μF capacitor
C8	1μF capacitor
L1	ferrite bead
R1, R2, R3	75Ω 1% metal film resistor
Z1	adjustable regulator
R_{SET}	1% metal film resistor

Figure 5. Connection Diagram (External Current Reference)



Location	Description
C1–C4	0.1μF ceramic capacitor
C5	10μF capacitor
C6	47μF capacitor
C7	1μF capacitor
L1	ferrite bead
R1, R2, R3	75Ω 1% metal film resistor
Z1	adjustable regulator
R_{SET}	1% metal film resistor

TIMING WAVEFORMS

Figure 6. MPU Read/Write Timing

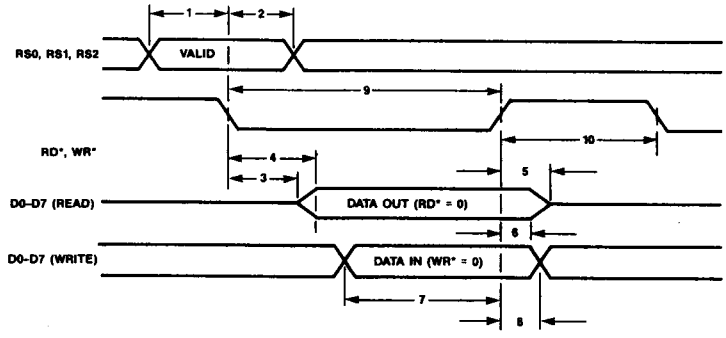
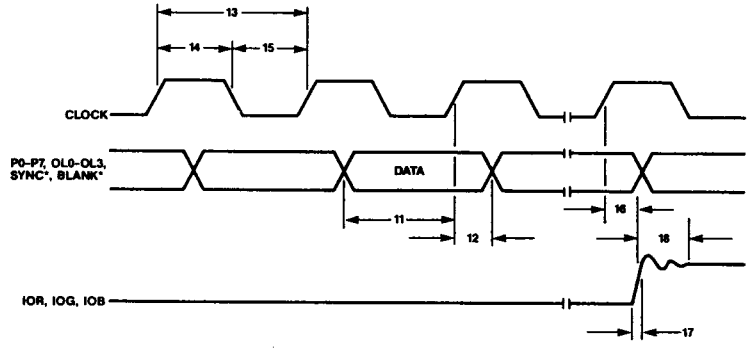


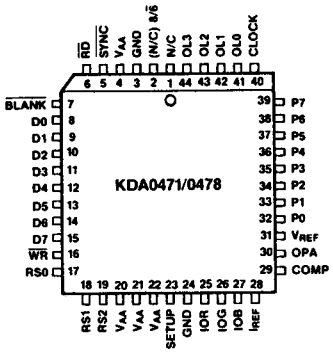
Figure 7. Video Input/Output Timing

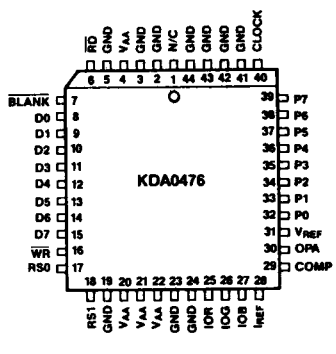


Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ±1 LSB (KDA0478), ±1/4 LSB (KDA0471), or ±1/2 LSB (KDA0476).
Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transiition.

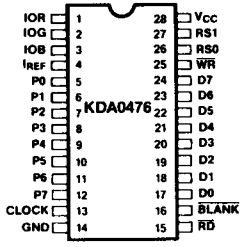
PIN CONFIGURATIONS

44-Pin Plastic J-Lead (PLCC)

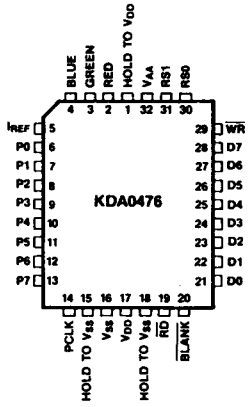




28-Pin DIP (600 mil)



32-Pin Plastic J-Lead (PLCC)



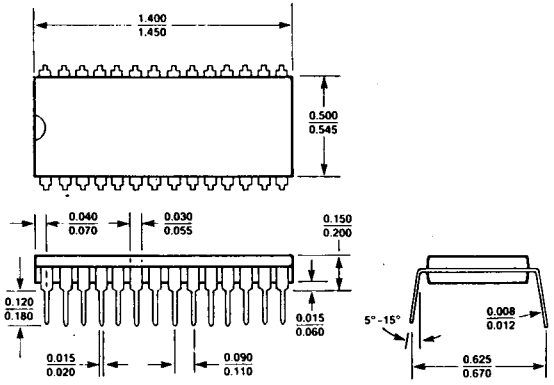
Notes:
1. N/C pins may be left unconnected without affecting the performance of the KDA0471/0476/0478.
2. ( ) for the KDA0471.

PACKAGE INFORMATION

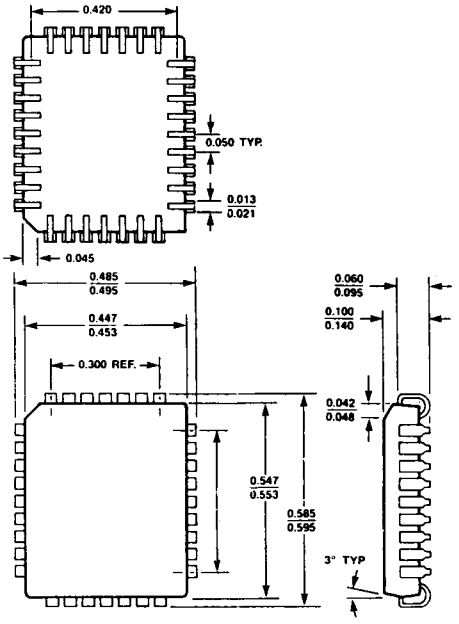
Samsung Part No.	Color Palette RAM	Overlay Palette	Speed (MHz)	Package
KDA0471PL-80	256 x 18	15 x 18	80	44-Pin PLCC
KDA0471PL-66	256 x 18	15 x 18	66	44-Pin PLCC
KDA0471PL-50	256 x 18	15 x 18	50	44-Pin PLCC
KDA0476CN-80	256 x 18	—	80	28-Pin DIP (600 mil)
KDA0476CN-66	256 x 18	—	66	28-Pin DIP (600 mil)
KDA0476CN-50	256 x 18	—	50	28-Pin DIP (600 mil)
KDA0476PL-80	256 x 18	—	80	44-Pin PLCC
KDA0476PL-66	256 x 18	—	66	44-Pin PLCC
KDA0476PL-50	256 x 18	—	50	44-Pin PLCC
KDA0476PJ-80	256 x 18	—	80	32-Pin PLCC
KDA0476PJ-66	256 x 18	—	66	32-Pin PLCC
KDA0476PJ-50	256 x 18	—	50	32-Pin PLCC
KDA0478PL-120	256 x 24	15 x 24	120	44-Pin PLCC
KDA0478PL-100	256 x 24	15 x 24	100	44-Pin PLCC
KDA0478PL-80	256 x 24	15 x 24	80	44-Pin PLCC
KDA0478PL-66	256 x 24	15 x 24	66	44-Pin PLCC
KDA0478PL-50	256 x 24	15 x 24	50	44-Pin PLCC

PACKAGE DIMENSIONS

28-Pin Plastic DIP (600 mil)



32-Pin Plastic Leaded Chip Carrier (PLCC)



44-Pin Plastic Leaded Chip (PLCC)