

Cover Sheet	1
Block Diagram	2
GPIO Spec.	3
Clock Generation	4
mPGA478-B INTEL CPU Sockets	5 - 6
INTEL Brookdale MCH -- North Bridge	7 - 8
INTEL ICH2 -- South Bridge	9 - 10
LPC I/O W83627HF	11
AC'97 Codec	12
Audio Amp TL072	13
FWH -- BIOS	14
SDR DIMM-168	15
AGP 4X SLOT (1.5V)	16
PCI SLOT 1 & 2 & 3	17
IDE CONNECTORS	18
Front Panel & Connectors	19
USB & FAN Connectors	20
Game Port and CPU Thermal-strip	21
Voltage Regulator	22
Intersil HIP6301 PWM	23
IO Connectors	24
LAN INTEL 82562EM/ET	25
PCI TO ISA BRIDGE AND ISA SLOT	26,27
JUMPER SETTING	28
MANUAL	29
Design Guide	30,31,32
HISTORY 1	33

MS-6530

Version 1.0
06/27/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

**INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)**

On Board Chipset:

**BIOS -- FWH
AC'97 Codec -- AD1881/1885
LPC Super I/O -- W83627HF
Clock Generation -- CY28324
/ICS950208
LAN -- INTEL 82562ET/EM**

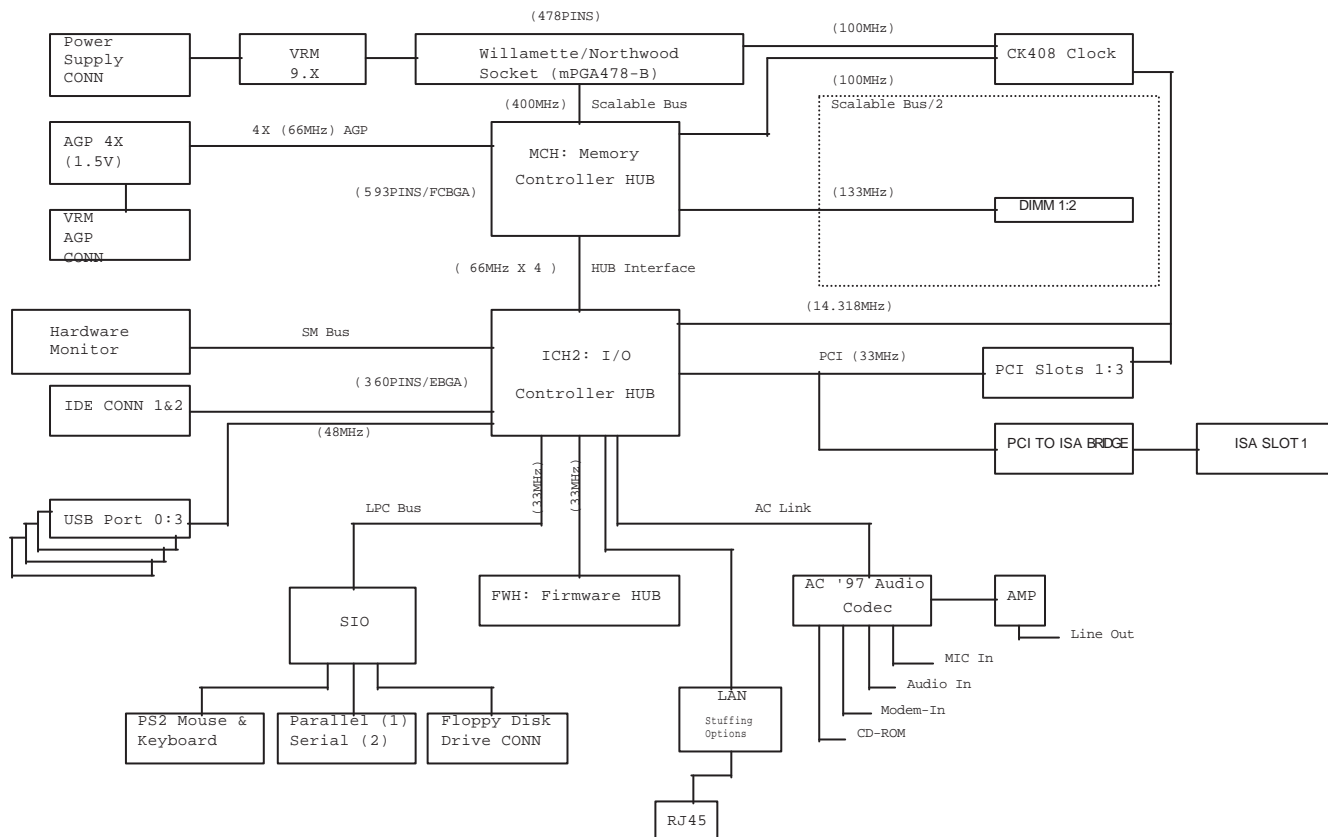
Expansion Slots:

**AGP2.0 SLOT * 1
PCI2.2 SLOT *3
CNR SLOT *0
ISA SLOT * 1 (Share PCI3)**

Option :

**A -> Without LAN
T -> Support CPU Thermstrip Function**

Micro-Star	Title MS-6530	Rev 100
Document Number Cover Sheet		
Last Revision Date: Wednesday, July 04, 2001		Sheet 1 of 33



Micro-Star	Title MS-6530	Rev 100
Document Number Block Diagram		
Last Revision Date: Wednesday, July 04, 2001		Sheet 2 of 33

General Purpose I/O Spec.

ICH2

GPIO Pin	PIN #	Type	Function
GPIO 0	M3	I	PCI TO ISA REQA#
GPIO 1	L3	I	Not Using (PREQ#5)
GPIO 2	N3	I	Not Using (INTE#)
GPIO 3	N2	I	Not Using (INTF#)
GPIO 4	N1	I	Not Using (INTG#)
GPIO 5	M4	I	Not Using (INTH#)
GPIO 6	Y11	I	Reserved for futuer
GPIO 7	AA11	I	Non Connect
GPIO 8	Y14	I	LAN Wake Up
GPIO 9	Y22	I	AC'97 Serial Data In 0
GPIO 10		I	Non Connect
GPIO 11	AB17	I	Not Using (SMB_ALERT)
GPIO 12	W14	I	External SMI
GPIO 13	AB15	I	LPC PME
GPIO 14~15		I	Not Implemented
GPIO 16	L2	O	PCI TO ISA GNTA#
GPIO 17	L4	O	Non Connect
GPIO 18	A15	O	Non Connect
GPIO 19	D14	O	Non Connect
GPIO 20	C14	O	Non Connect
GPIO 21	L1	O	PCI TO ISA NOGO
GPIO 22	B14	OD	Non Connect
GPIO 23	A14	O	BIOS Locked/Unlocked
GPIO 24	V21	O	Reserved for futuer
GPIO 25	W15	O	LAN Enable/Disable Detected
GPIO 26		O	Non Connect
GPIO 27	AB14	I/O	Non Connect
GPIO 28	AA14	I/O	LAN ENABLE/DISABLE
GPIO 29~31		I/O	Not Implemented

FWH

GPIO Pin	PIN #	Type	Function
GPI 0	6	I	ATA IDE 1 Detect
GPI 1	5	I	ATA IDE 2 Detect
GPI 2	4	I	Not Using
GPI 3	3	I	Not Using

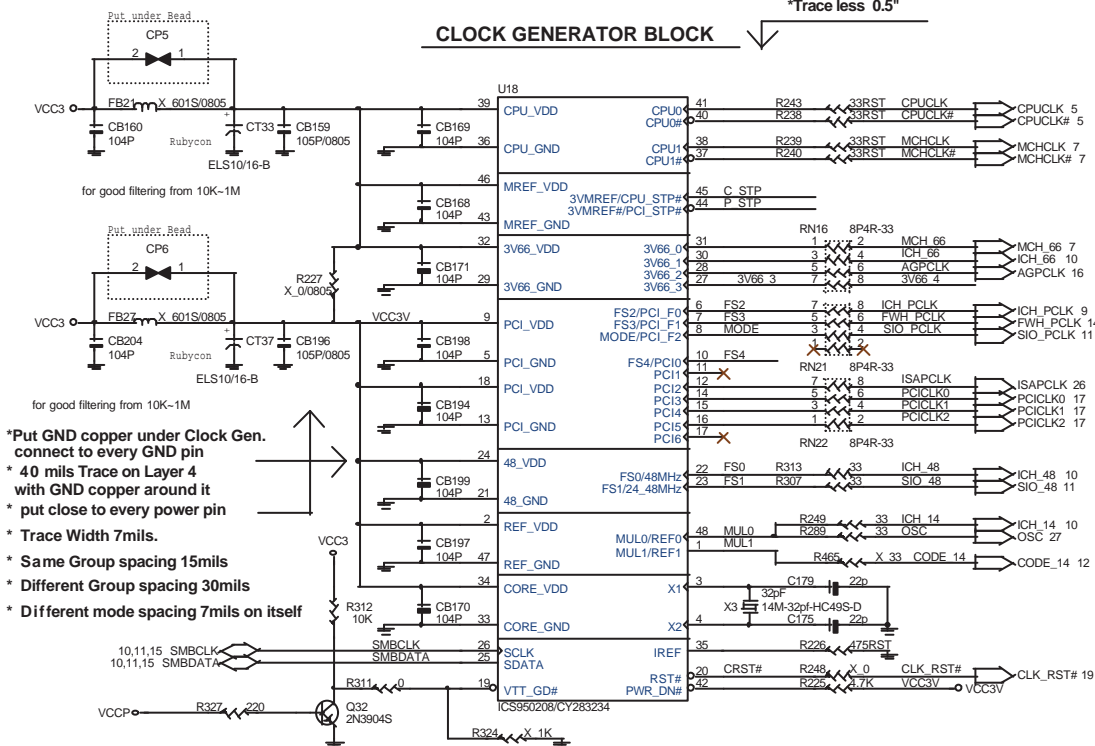
SIO

GPIO Pin	PIN #	Type	Function
GP32	71	I/OD	Non Connect
GP24	89	I/OD	Non Connect
GP34	69	I/OD	Non Connect
GP33	70	I/OD	Non Connect

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
ISA SLOT		AD22

CLOCK GENERATOR BLOCK

*Trace less 0.5"

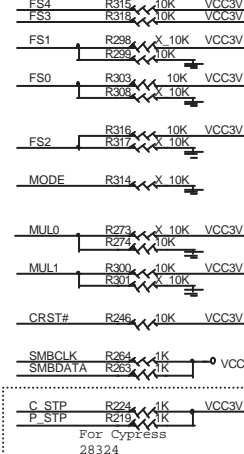


Shut Source Termination Resistors

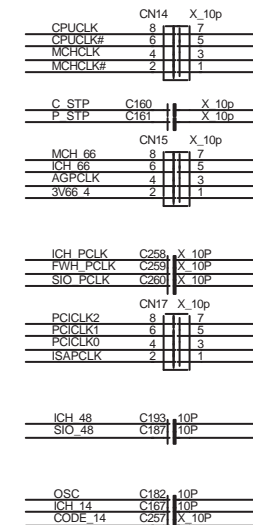


Trace less 0.2"
49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



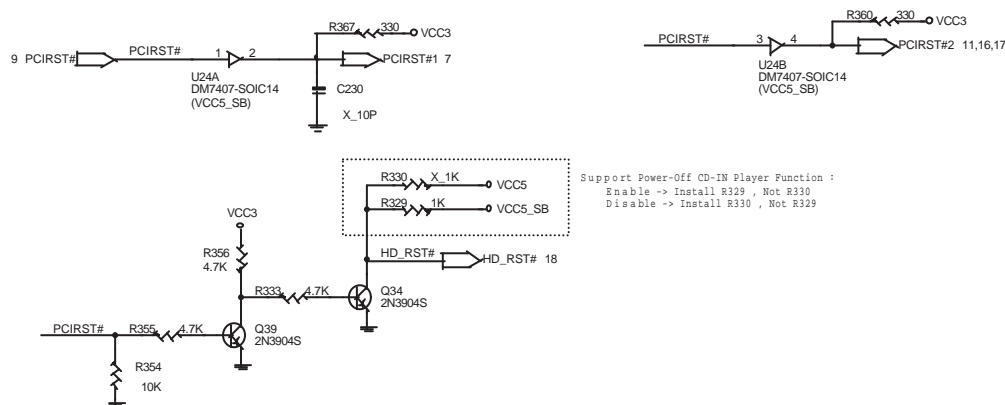
Pull-Down Capacitors



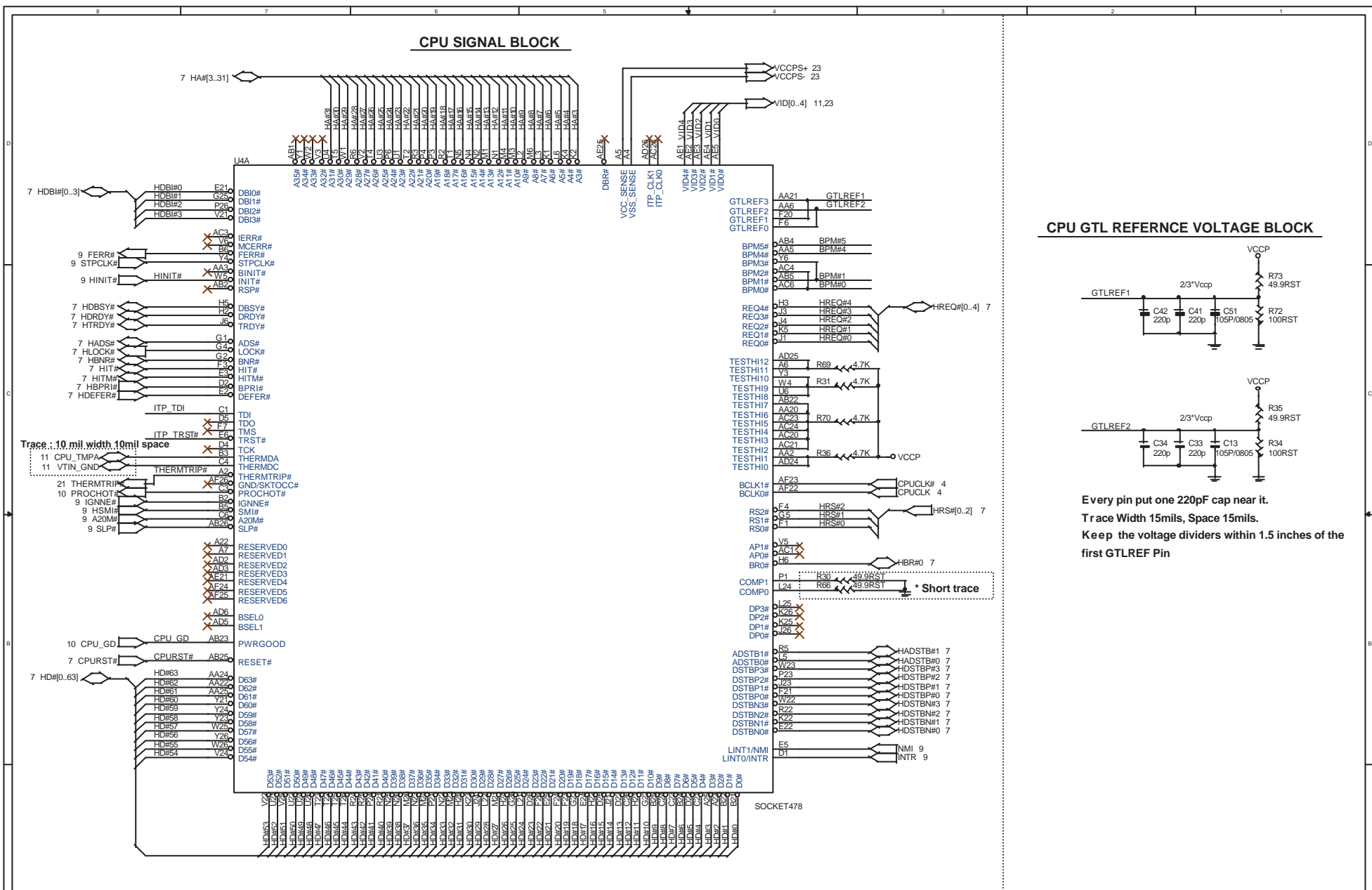
used only for EMI issue

Trace less 0.2"

RESET BLOCK



Micro-Star	Title MS-6530	Rev 100
Document Number	Clock CY28323/4	
Last Revision Date: Wednesday, July 04, 2001	Sheet	4 of 33



CPU STRAPPING RESISTORS

Signal	Resistor	Value	Connection
BPM#0	R12	49.9RST	VCCP
BPM#1	R15	49.9RST	VCCP
BPM#4	R17	49.9RST	VCCP
BPM#5	R18	49.9RST	VCCP

ALL COMPONENTS CLOSE TO CPU

Signal	Resistor	Value	Connection
PROCHOT#	R32	62	VCCP
CPU_GD	R67	300	VCCP
HBR#	R50	49.9RST	VCCP
CPURST#	R71	49.9RST	VCCP
THERMTRIP#	R62	K 62	VCCP
HINIT#	R466	300	VCCP

Horizontal scale bar: 8, 7, 6, 5, 4, 3

CPU STRAPPING RESISTORS

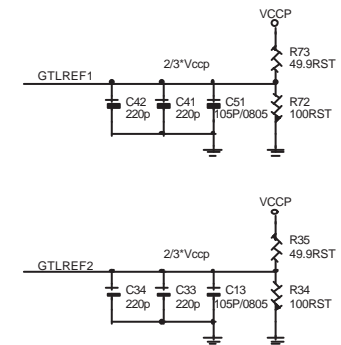
Component	Resistor	Value	Connection
BPM#0	R12	49.9RST	VCCP
BPM#1	R15	49.9RST	VCCP
BPM#4	R17	49.9RST	VCCP
BPM#5	R18	49.9RST	VCCP

ITP_TDI → R51 (150) → VCCP

ITP_TRST# → R33 (680) → VCCP

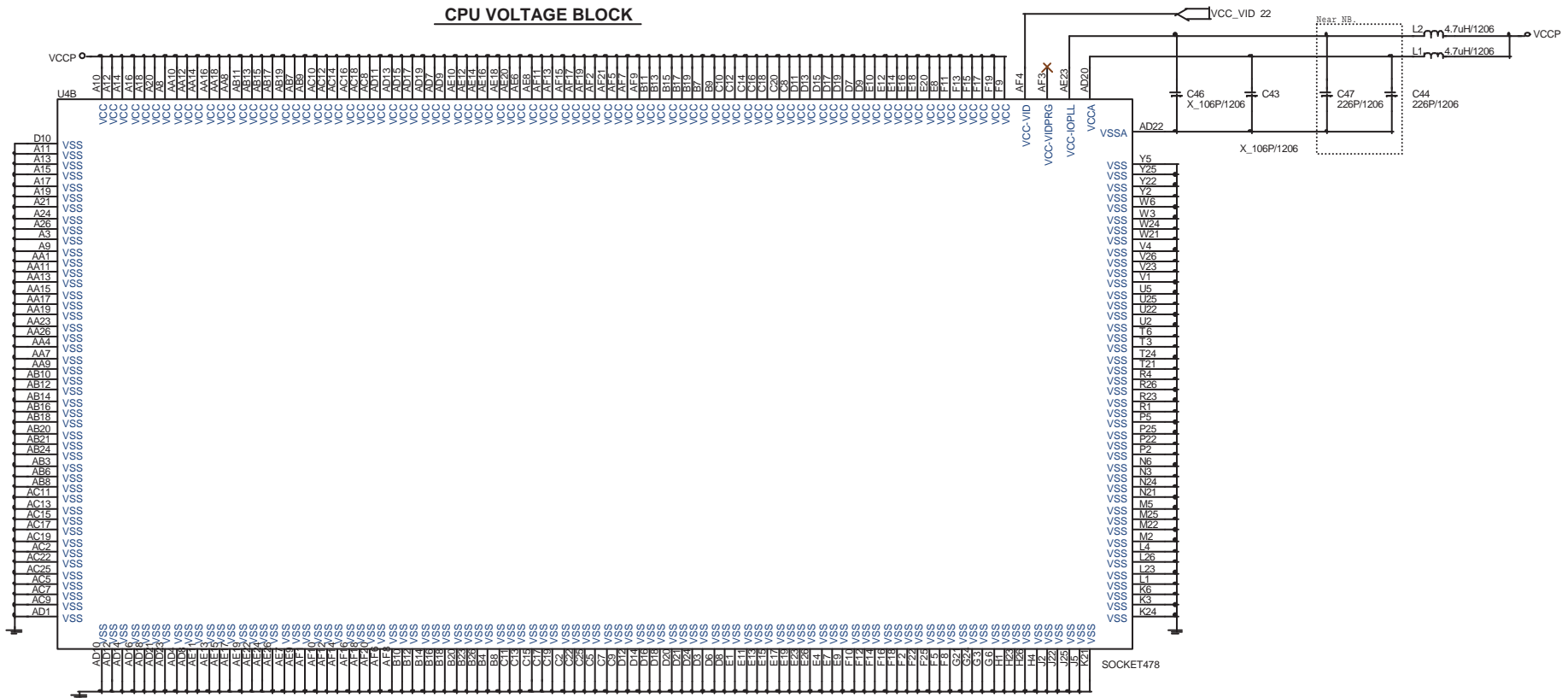
ALL COMPONENTS CLOSE TO CPU

Component	Resistor	Value	Connection
PROCHOT#	R32	52	VCCP
CPU_GD	R67	300	VCCP
HBR#	R50	49.9RST	VCCP
CPURST#	R71	49.9RST	VCCP
THERMTRIP#	R62	~ 62	VCCP
HINIT#	R46	300	VCCP



Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

<i>Micro-Star</i>	Title	<i>MS-6530</i>	Rev	<i>100</i>
Document Number				
INTEL mPGA478-B CPU1				
Last Revision Date: Wednesday, July 04, 2001		Sheet	5	of 33



VCCP

CT47
150UF/2.5V
CT9
150UF/2.5V
CT11
150UF/2.5V

<i>Mic ro-Star</i>	Title	<i>MS-6530</i>	Rev	<i>100</i>
Document Number				
INTEL mPGA478-B CPU2				
Last Revision Date: Wednesday, July 04, 2001		Sheet 6 of 33		

* Length must be matched within +/-0.1" of the Strobe Signals

HOST

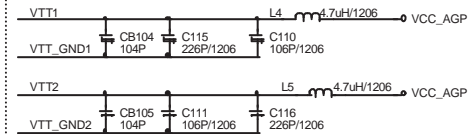
POWER

HUB LINK

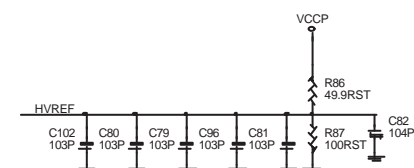
POWER

POWER

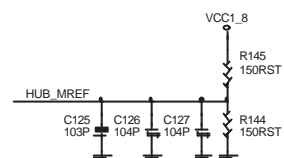
MCH REFERENCE BLOCK



Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

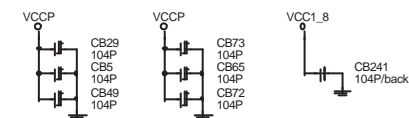


Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

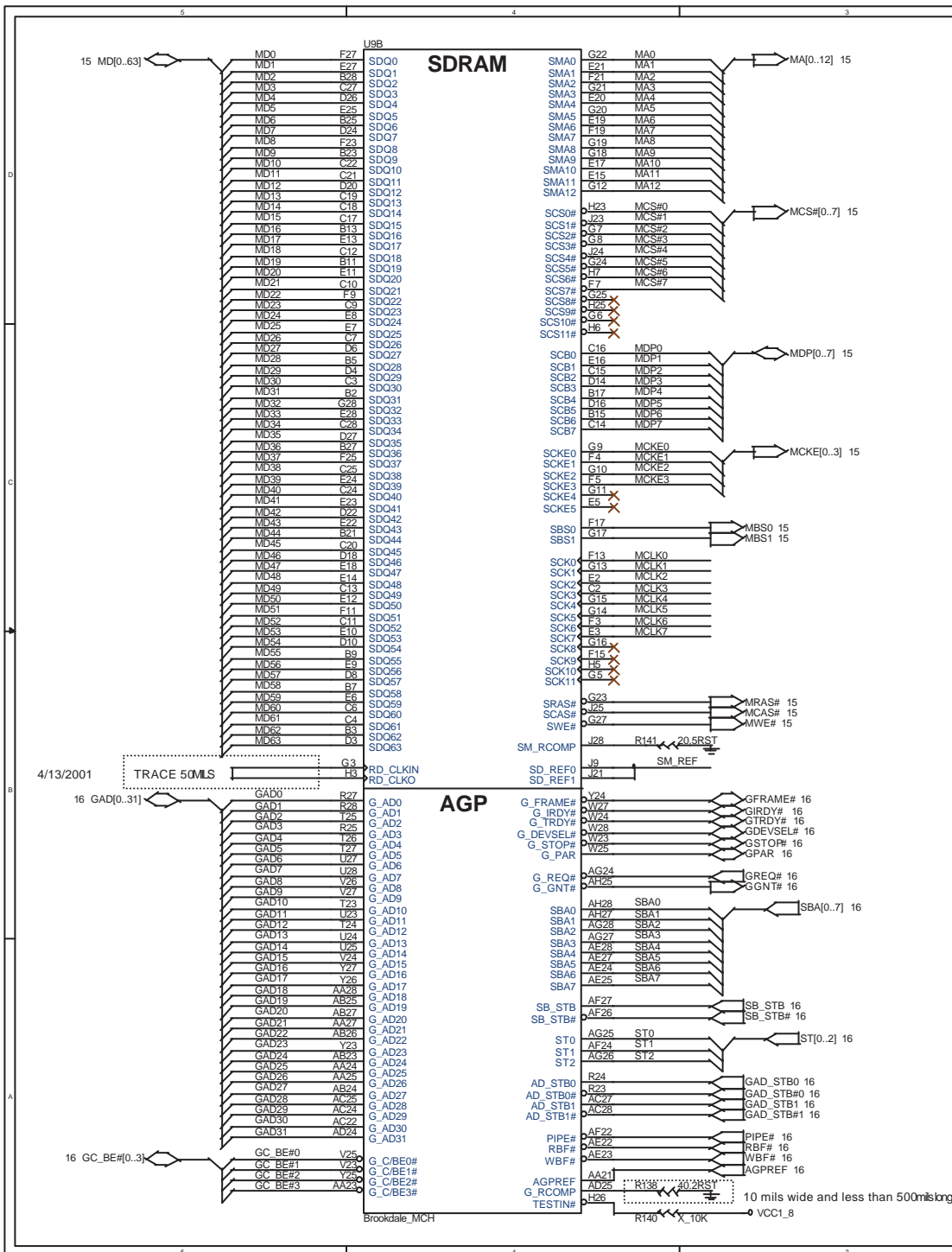


Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space

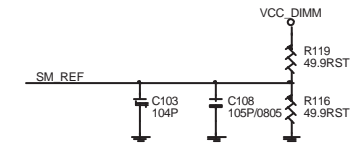
MCH Trace Decoupling Capacitors



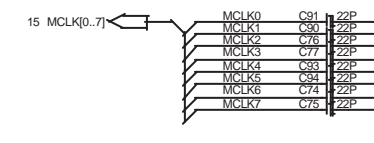
Document Number	Title	Rev
Micro-Star	MS-6530	100
Brookdale MCH1		
Last Revision Date: Wednesday, July 04, 2001	Sheet 7 of 33	



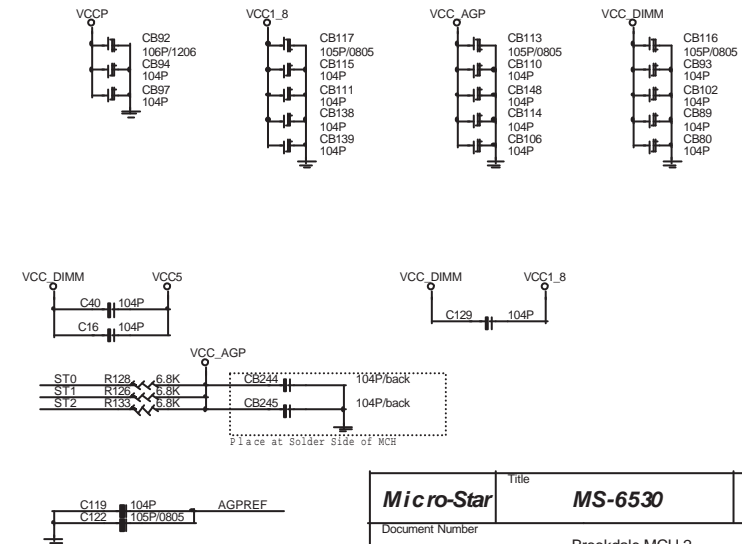
MCH REFERENCE VOLTAGE



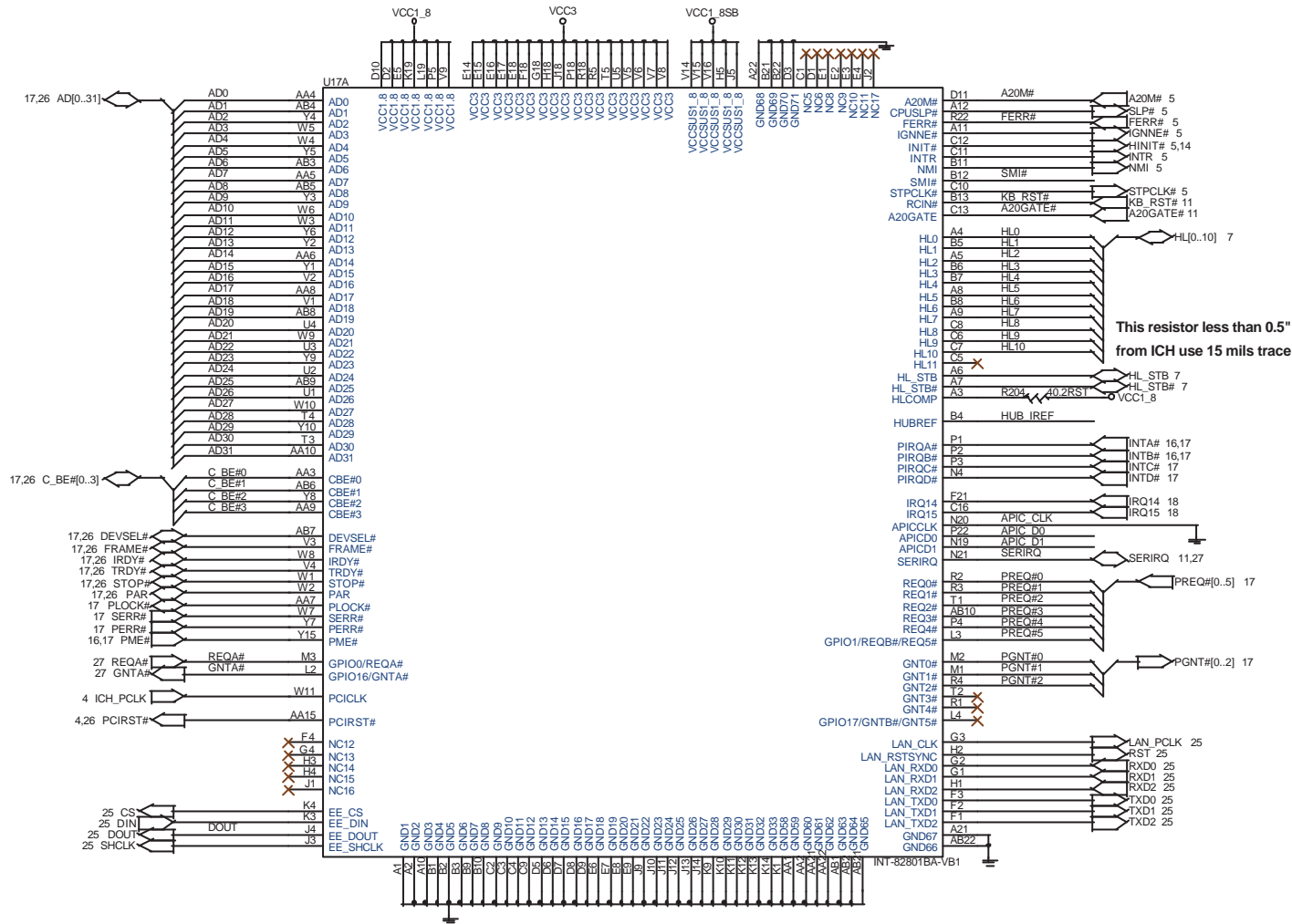
MCH MEMORY CLOCK RC CIRCUITS



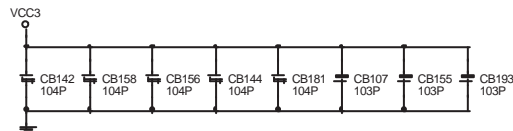
MCH DECOUPLING CAPACITOR



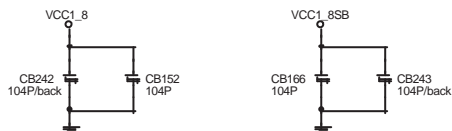
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



ICH2 DECOUPLING CAPACITORS



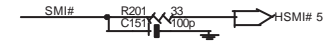
Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



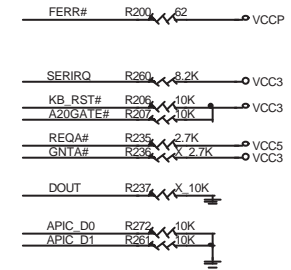
Distribute near the 1.8V power pin of the ICH2

Distribute near the VCC1_8SB Power pin of the ICH2

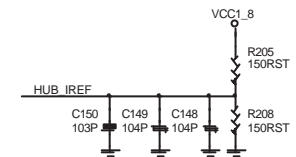
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS



ICH2 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

Micro-Star	Title MS-6530	Rev 100
Document Number	Brookdale ICH2 PCI	
Last Revision Date: Wednesday, July 04, 2001	Sheet 9	of 33

[illegible]

PROCHOT BLOCK

THRM#

Q33
2N3904S

VCCP R321 4.7K

5 PROCHOT#

ICH2 STRAPPING RESISTORS

PD_IORDY R223 4.7K VCC3

SD_IORDY R211 4.7K

PD_DREQ R234 5.6K

SD_DREQ R212 5.6K

INTRUDER# R296 10K RTC_VCC

RSMRST# R319 10K

SPKR R293 X 10K

PWR_GD R341 8.2K

GP6 R451 X 4.7K VCC3

R453 X 4.7K

GP24 R452 X 4.7K VCC3_SB

R454 X 4.7K

SM_LNK0 1 X 2

SM_LNK1 1 X 2

BATLOW# 5 X 2

SIO_PME# R477 4.7K

SMB_ALERT 1 X 2

RING# 1 X 2

GP28 5 X 2

GPIO22 R449 4.7K VCC3

THRM# R450 4.7K

VCC3_SB

VCC3

VCC3_SB

VCC3

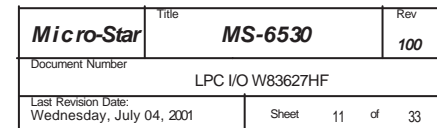
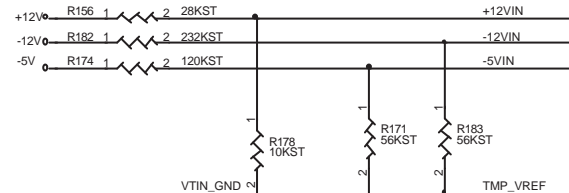
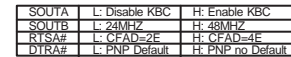
VCC3_SB

P. RESERVED FOR FUTURE

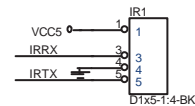
<i>Micro-Star</i>	Title	<i>MS-6530</i>	Rev	<i>100</i>
Document Number		Brookdale ICH2 Other		
Last Revision Date: Wednesday, July 04, 2001		Sheet 10 of 33		



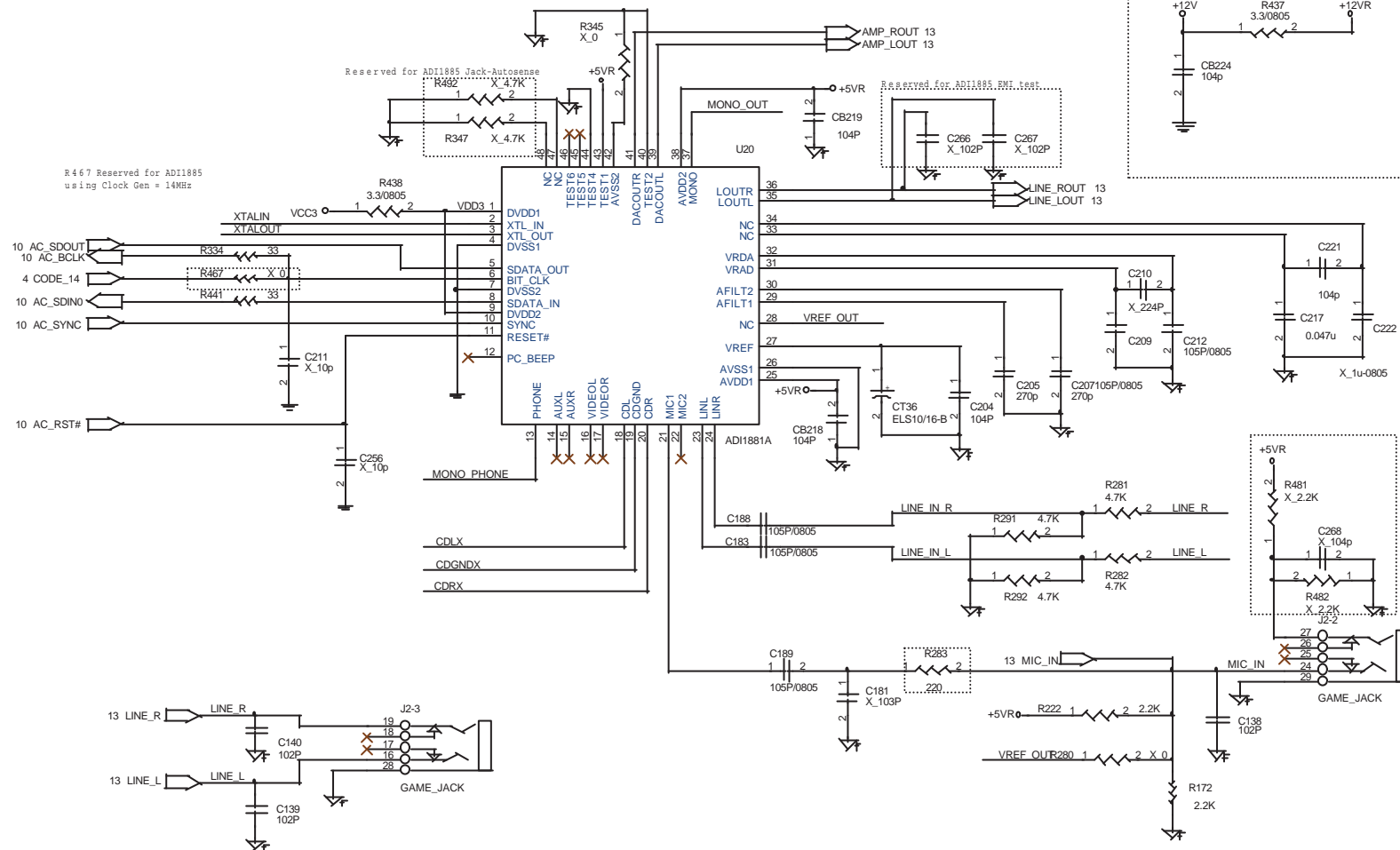
**NOTE: LOCATE CLOSE
STATUS PANEL**



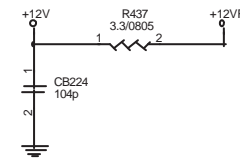
Stuff all for D version bug



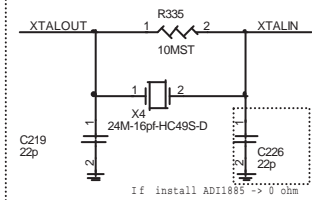
AD1885 AC97 CODEC



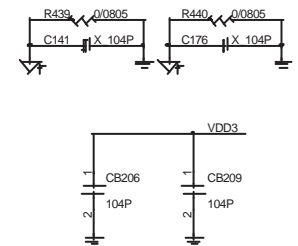
AUDIO CODE REGULATORS



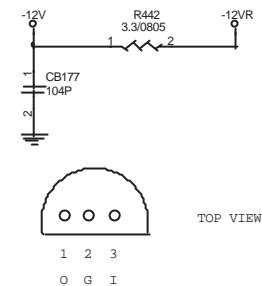
AUDIO CODE CRYSTAL CIRCUIT



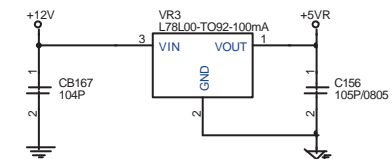
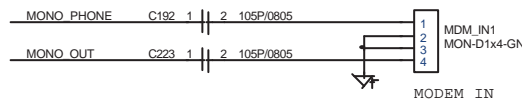
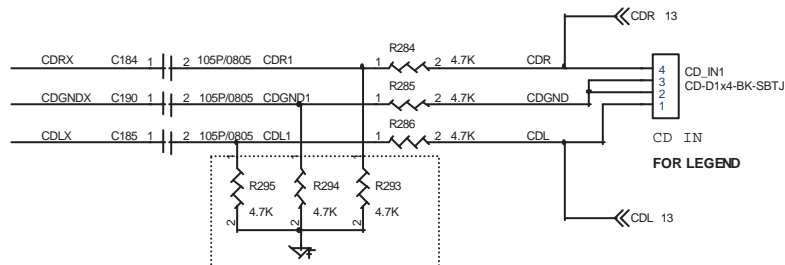
DECOUPLING CAPACITOR



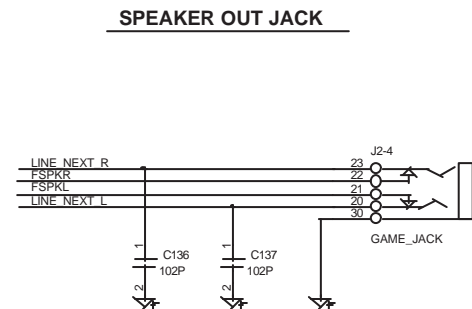
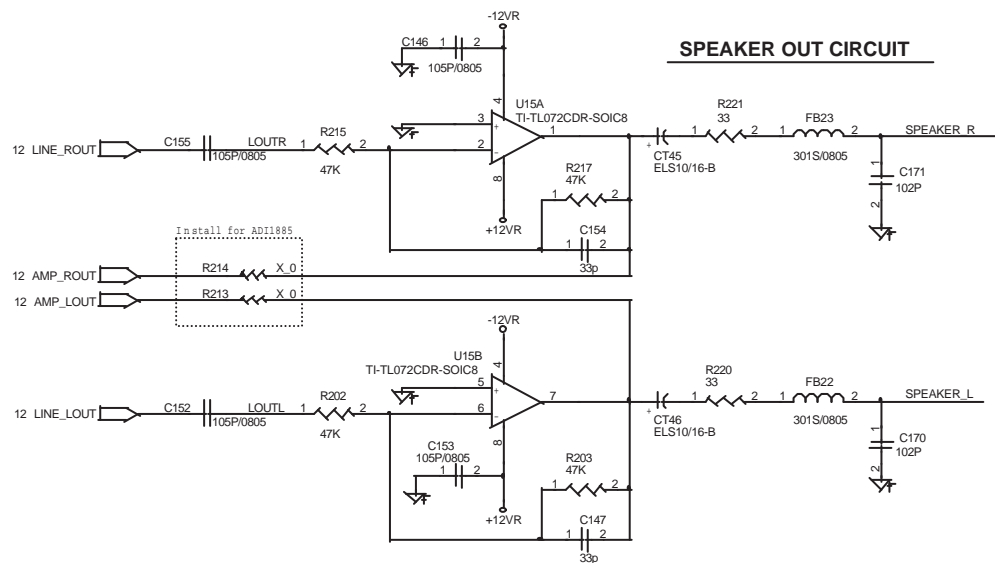
AUDIO CODE REGULATORS



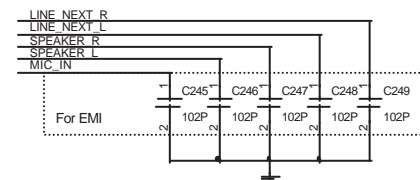
AUDIO CODE CD / AUX / MODEM IN HEADERS



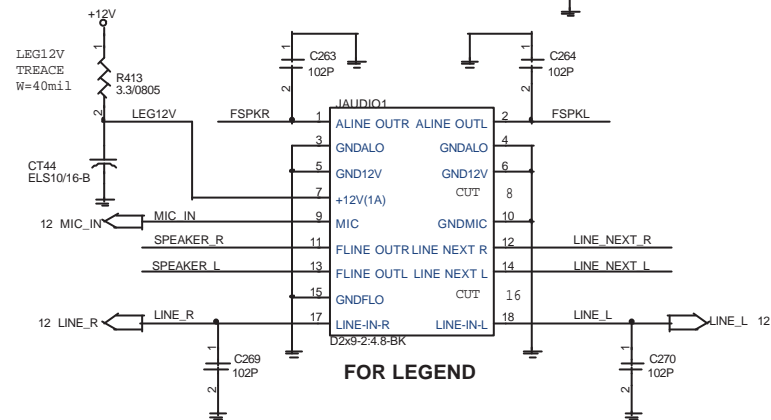
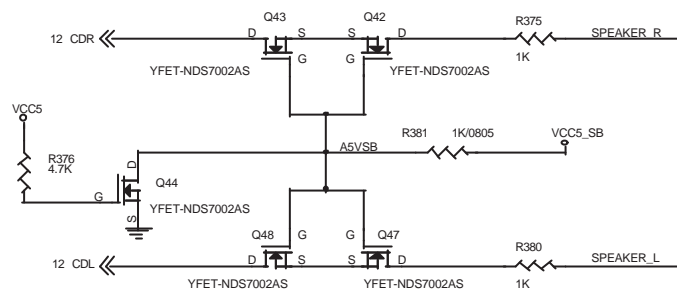
Micro-Star	Title MS-6530	Rev 100
Document Number	AC97 CODEC	
Last Revision Date: Wednesday, July 04, 2001	Sheet	12 of 33



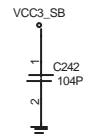
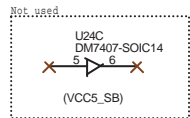
FOR MSI INTERNAL HEADER



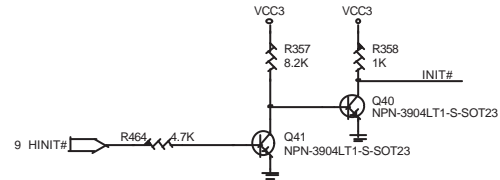
CD PANEL PLAY WITHOUT PC POWER_ON



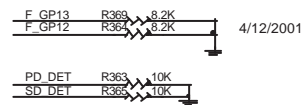
Micro-Star	Title	MS-6530	Rev	100
	Document Number	Audio Amp TL072		
	Last Revision Date:	Wednesday, July 04, 2001	Sheet	13 of 33



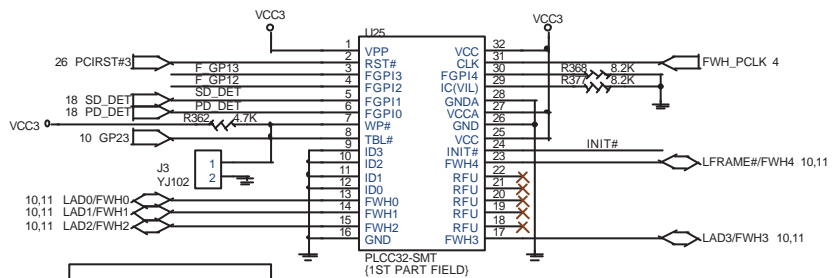
FWH INIT Signal Voltage Translation Block



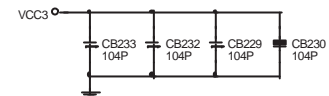
FWH RESISTORS



Firware Hub (FWH)



FWH DECOUPLING CAPACITORS



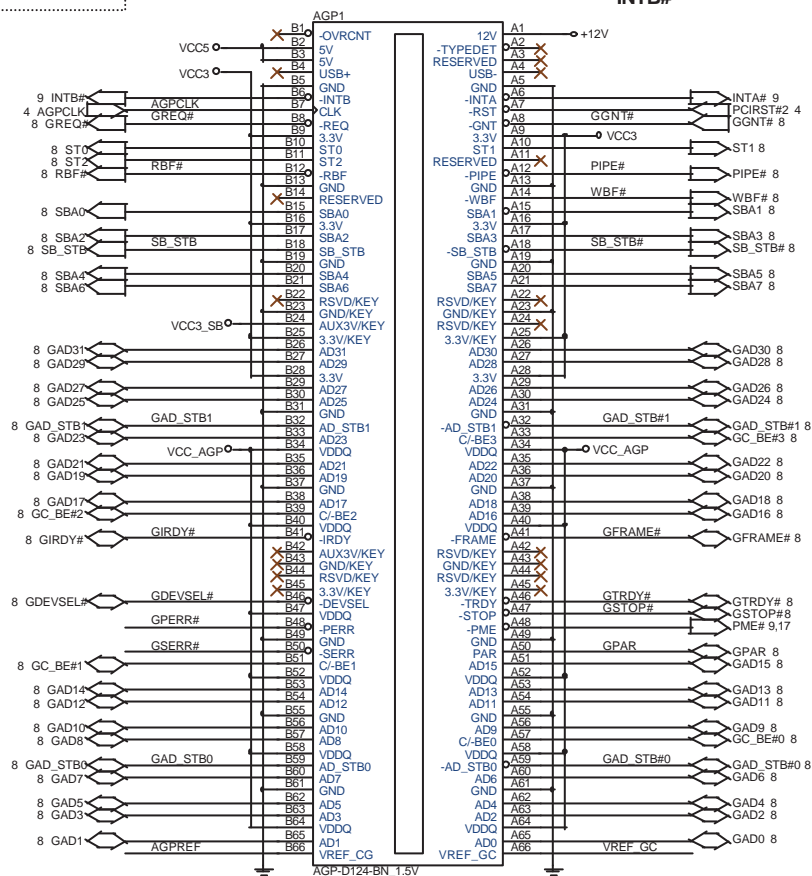
J3 BIOS Update	
SHORT	Locked
* OPEN	Unlocked

Micro-Star	Title MS-6530	Rev 100
Document Number FWH		
Last Revision Date: Wednesday, July 04, 2001		Sheet 14 of 33

VCC5 = 60mils trace / 15 mils space

VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#



VCC_AGP

R154
1KST

AGPREF: 10uA

AGPREF

AGPREF 8

R149
1KST

C128
105P/0805

C126
105P/0805

CB122
104P

NEAR AGP SLOT

C133 X 104P

VREF_GC

Trace width : 25 mils
C157 should be placed near MCH within 150 mils

GFRAME#	R196	X 6.8K		PIPE#	R163	X 6.8K	
GIRDY#	R197	X 6.8K		RBF#	R160	X 6.8K	
GTRDY#	R198	X 6.8K		WBF#	R164	X 6.8K	
GDRVSTLW	R199	X 6.8K					
GSTOP#	R193	X 6.8K					
GPAP	R195	X 6.8K		GAD_STB0	R187	X 6.8K	
GPERR#	R194	X 6.8K		GAD_STB1	R188	X 6.8K	
GSERR#	R192	X 6.8K		S5_STB1	R189	X 6.8K	
				GAD_STB#1	R159	X 6.8K	
GREQ#	R162	X 6.8K		GAD_STB#0	R158	X 6.8K	
GGNT#	R161	X 6.8K		SB_STB#	R154	X 6.8K	

LESS 100MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

The schematic diagram illustrates the power supply network for the system. It features six distinct power supply rails, each with its own decoupling network:

- VCC_AGP:** Decoupled by CT30 (1000uF) and a series of capacitors: CB137 (104P), CB145 (104P), CB134 (104P), CB132 (104P), and CB150 (104P).
- VCC3_SB:** Decoupled by CB126 (104P), CB124 (104P), and CB123 (104P).
- VCC5:** Decoupled by CB180 (104P) and a variable capacitor CB175 (X 100pF).
- VCC3:** Decoupled by a series of capacitors: CB133 (100p), CB135 (104P), CB136 (104P), CB127 (104P), CB149 (103P/10805), and CB121 (100p).

1X Timing group	2X/4X Timing group
AGPCLK	SET#1
PIPE#	GAD[15..0]
RFB#	GC_BE#1..0
WBF#	GAD_STB0
GTZ[2..0]	GAD_STB#
FRAME#	SET#2
GIRDY#	GAD[31..16]
GTRDY#	GC_BE#3..2
GSTOP#	GAD_STB1
GDEVSEL#	GAD_STB1#
GREQ#	SET#3
GNT#	SBA[7..0]
GPAR	SB_STB
	SB_STB#

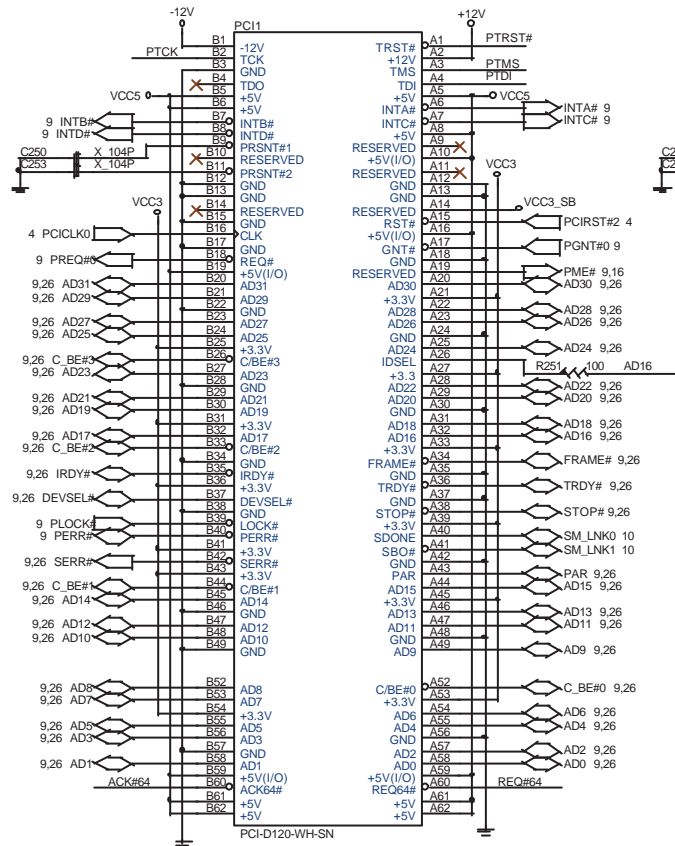
SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

Figure 1 consists of two horizontal bar charts comparing the signal-to-noise ratio (SNR) for different signal processing techniques. The top chart, labeled "Trace 5mils", compares "2x / 4x Signals" (black bar) and "2x / 4x Signals" (gray bar) for "15 / 20 mils" and "30 mils" conditions. The bottom chart compares "AGP STB" (black bar) and "AGP STB#" (gray bar) for the same conditions. The x-axis represents SNR in dB, ranging from 0 to 100. The y-axis lists the conditions and signal processing techniques.

Condition	Signal Processing Technique	SNR (dB)
Trace 5mils	2x / 4x Signals (Black)	~85
	2x / 4x Signals (Gray)	~85
	2x / 4x Signals (Black)	~85
	2x / 4x Signals (Gray)	~85
AGP STB	AGP STB (Black)	~85
	AGP STB# (Gray)	~85
	AGP STB (Black)	~85
	AGP STB# (Gray)	~85

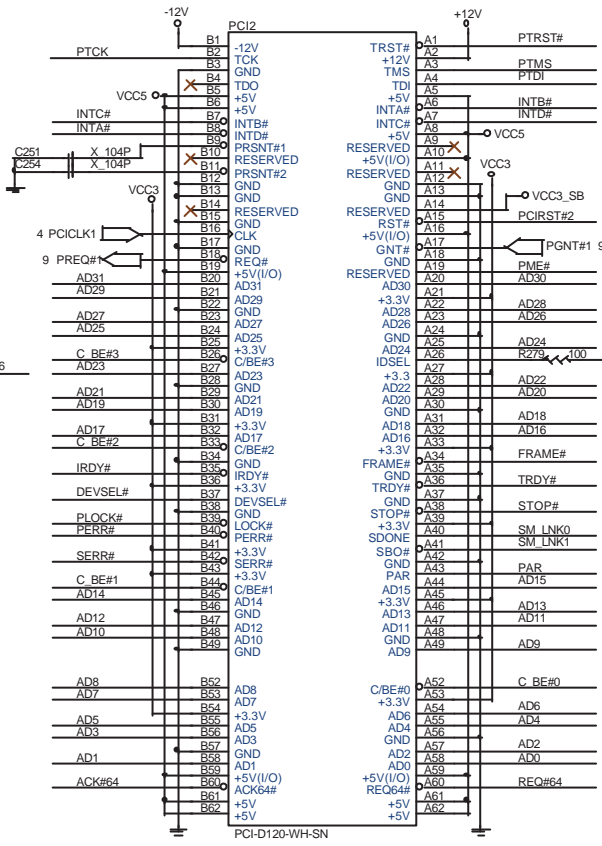
Micro-Star	Title MS-6530	Rev 100
Document Number		AGP Slot
Last Revision Date: Wednesday, July 04, 2001		Sheet 16 of 33

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



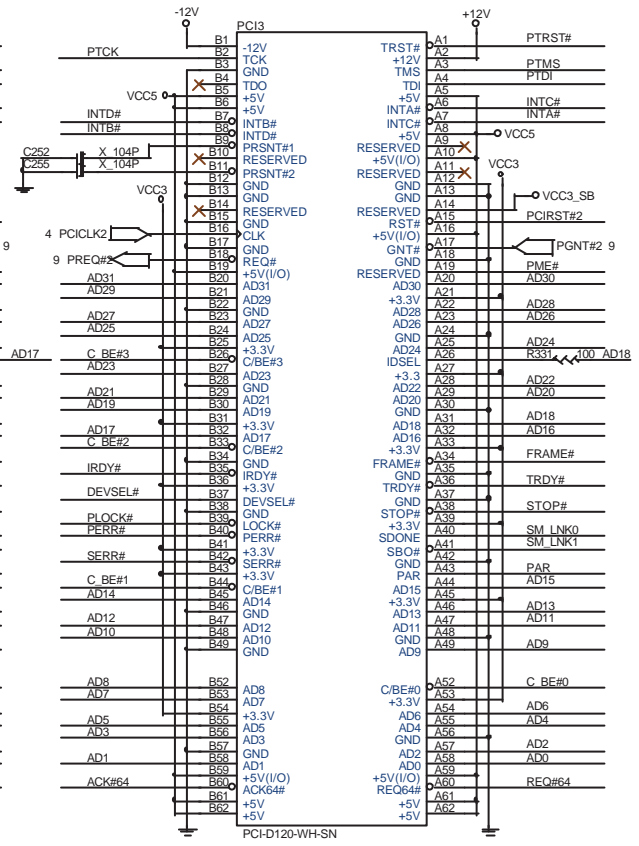
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



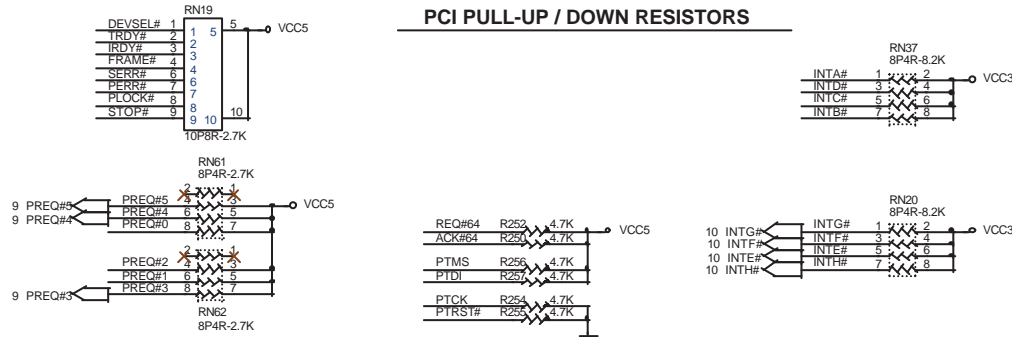
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

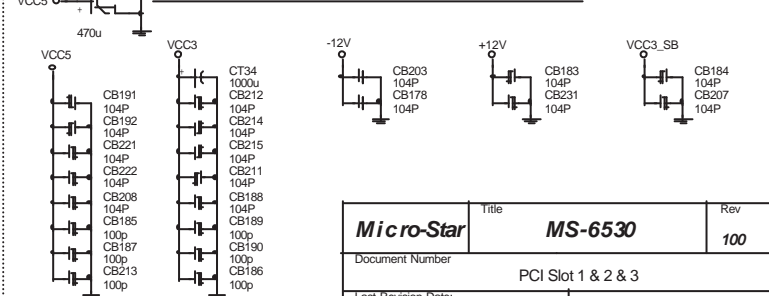


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



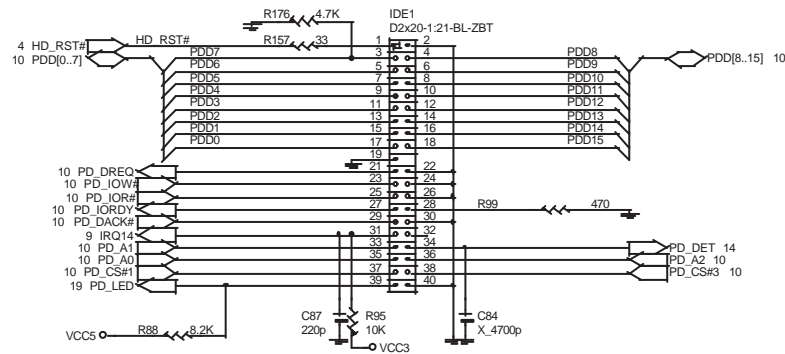
PCI SLOT DECOUPLING CAPACITORS



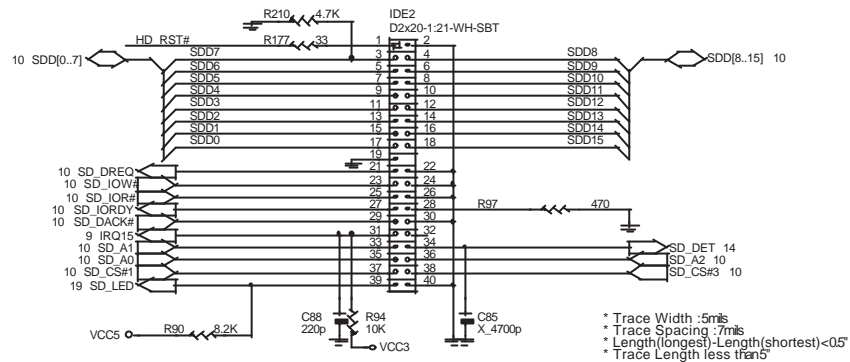
Document Number	MS-6530	Rev	100
PCI Slot 1 & 2 & 3			
Last Revision Date: Wednesday, July 04, 2001			
Sheet 17 of 33			

ATA100 IDE CONNECTORS

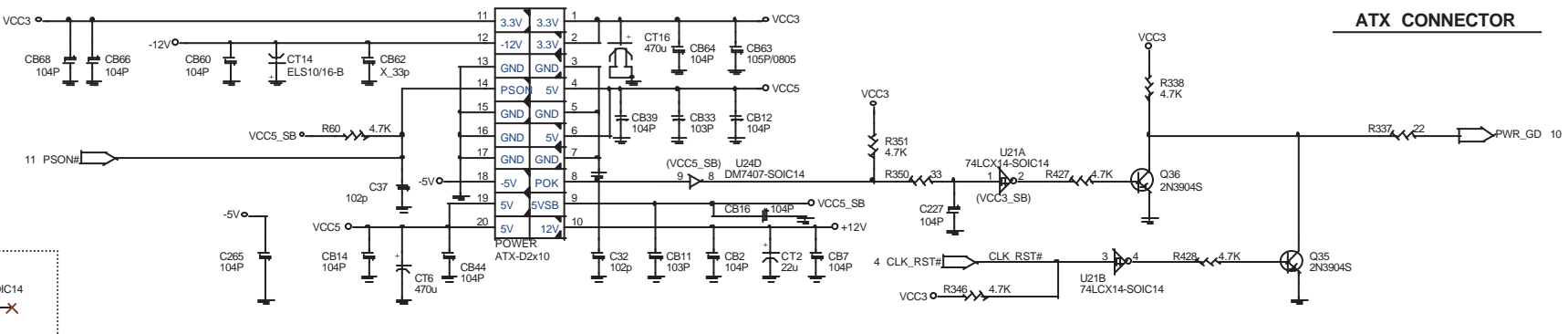
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



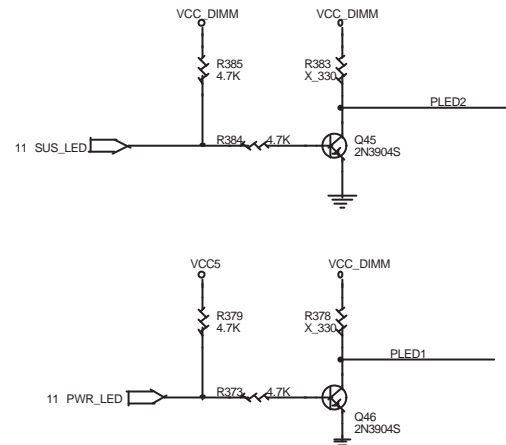
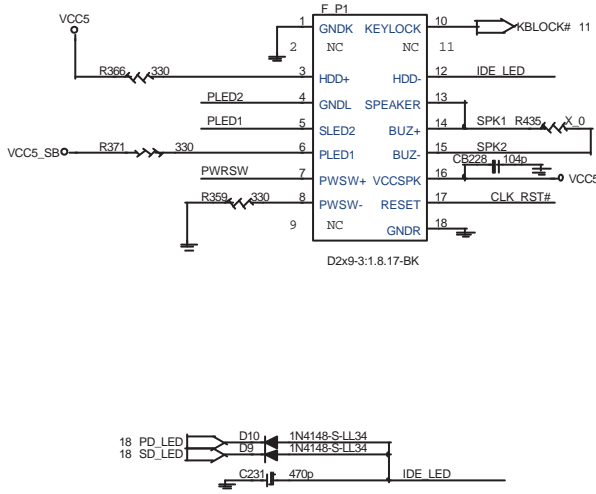
Micro-Star	Title	MS-6530	Rev	100
	Document Number	ATA100 IDE CONNECTORS		
	Last Revision Date:	Wednesday, July 04, 2001	Sheet	18 of 33



Not used

U24E
DM7407-SOIC14
11 10
(VCC5_SB)

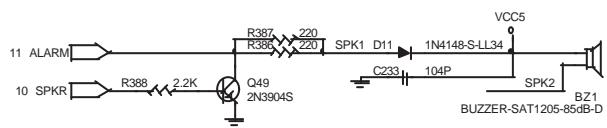
Brookdale FRONT PANEL-M



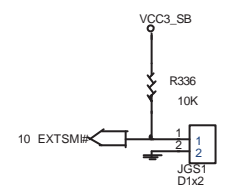
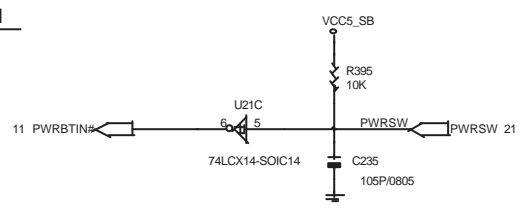
Front Panel LED Circuit component selection

	LEGEND	MSI
R371	ON	OFF
R373	ON	OFF
R378	OFF	OFF
R379	ON	OFF
R382	ON	OFF
R383	OFF	ON
R384	ON	ON
R385	4.7K	330
RN33	ON	OFF
RN35	OFF	ON
Q45	ON	ON
Q46	ON	OFF
JGL1	OFF	ON
JGLED1	ON	OFF

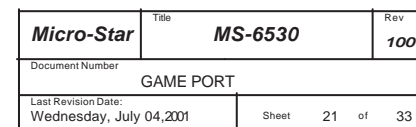
SPEAKER



POWER BUTTON



Micro-Star	Title MS-6530	Rev 100
Document Number Front Panel & Connector		
Last Revision Date: Wednesday, July 04, 2001		Sheet 19 of 33



[illegible][illegible]

Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN		28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

1.8V/3.3V SEQUENCE CIRCUIT

VCC3

R170
200RST

R167
470

R168
200RST

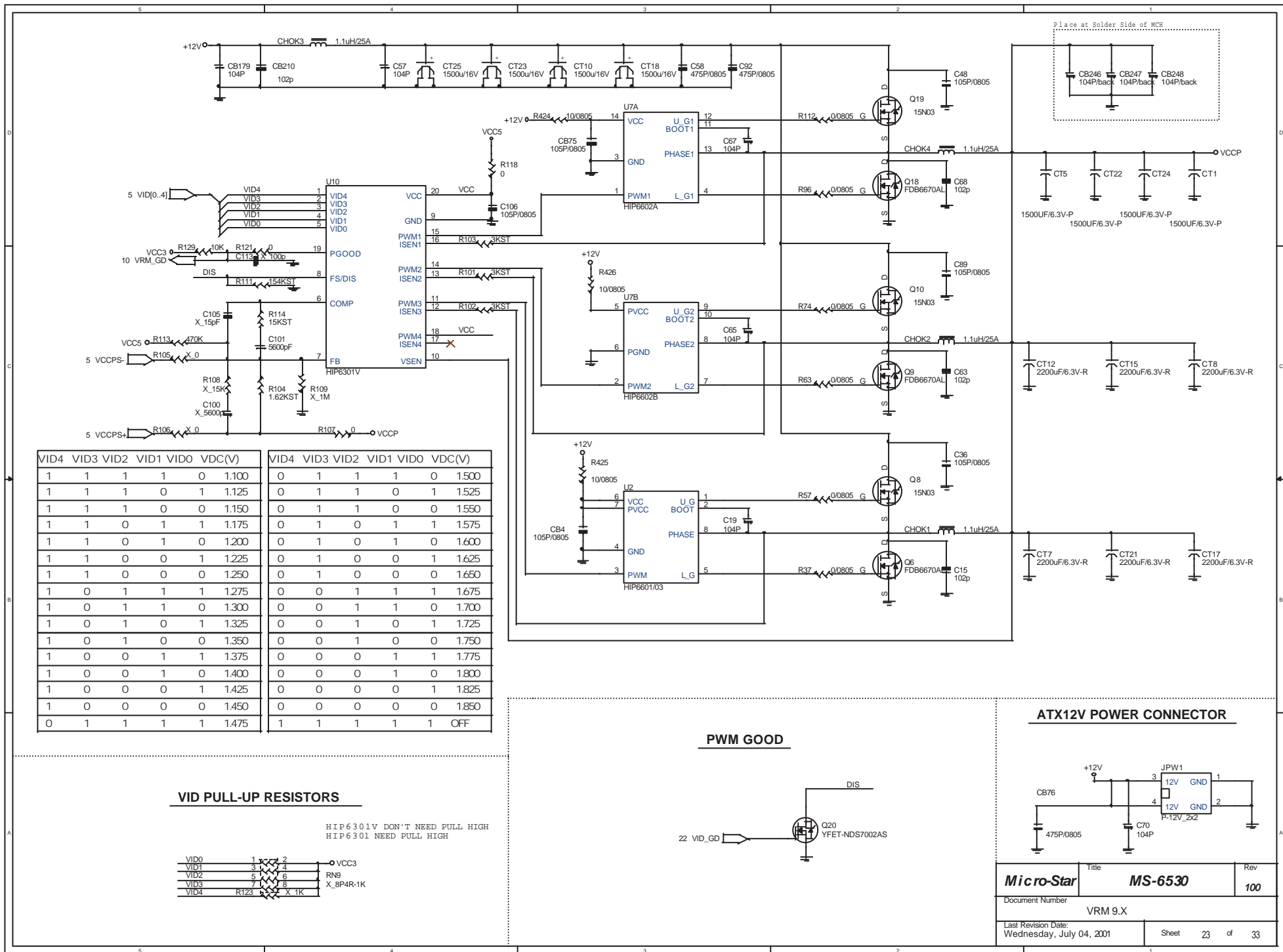
Q24
2N3906S
Ic=200mA
Vzbo=5V
Vceo=40V

Q23
2N3904S

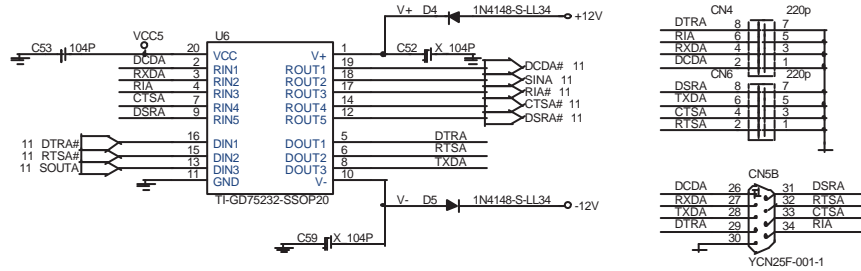
VCC1_8

The schematic diagram illustrates the internal circuitry of the MS-6530 Voltage Regulator. It shows a complex network of capacitors (CT29, CT28, CT19, CT43, CT41, CT27, CT26, CT32, CT31, CT30) and resistors (CB240, CB153, CB205, CB69, CB165, CB164, CB163) connected to various power supply pins (VCC1_8, VCC5_SB, VCC_DIMM, VCC5_STR, VCC3_SB, VCC3, VCC5) and an output pin (VCC5_STRO). The circuit is designed to regulate the output voltage from the input supply.

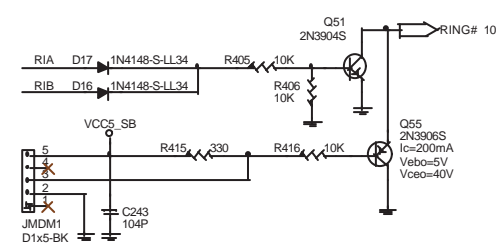
Title	Rev
Micro-Star MS-6530	100
Document Number	
Voltage Regulator	
Last Revision Date: Wednesday, July 04, 2001	Sheet 22 of 33



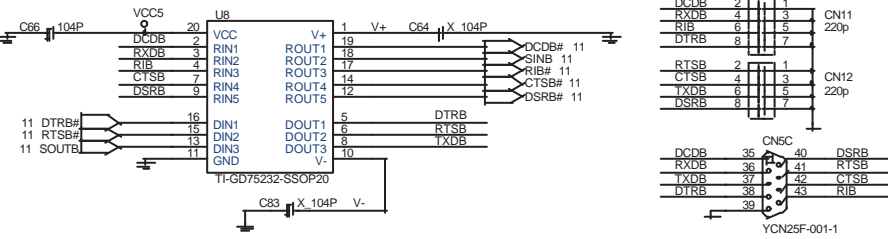
SERIAL PORT 1



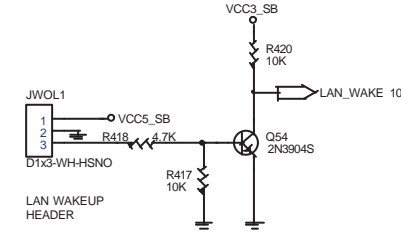
MODEM RING BLOCK



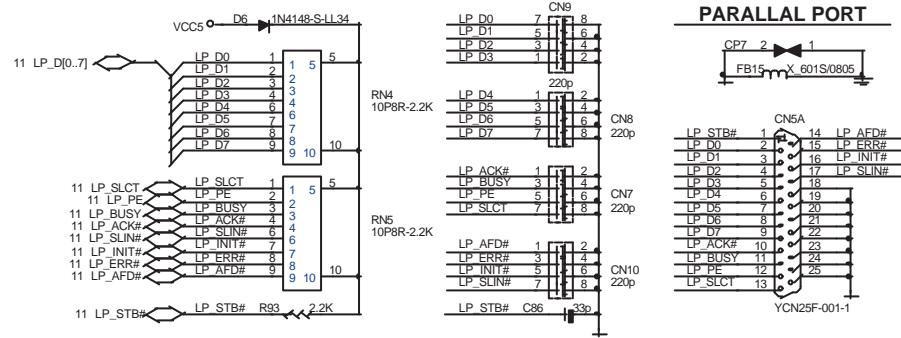
SERIAL PORT 2



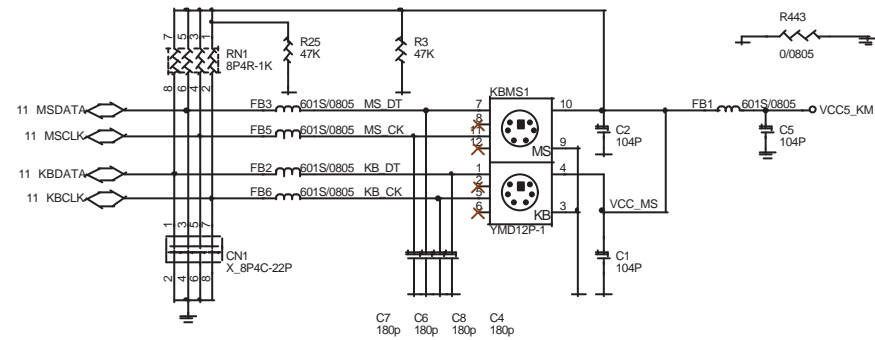
LAN WAKEUP BLOCK



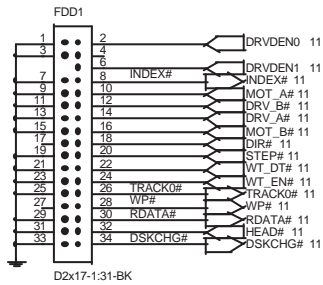
PARALLAL PORT



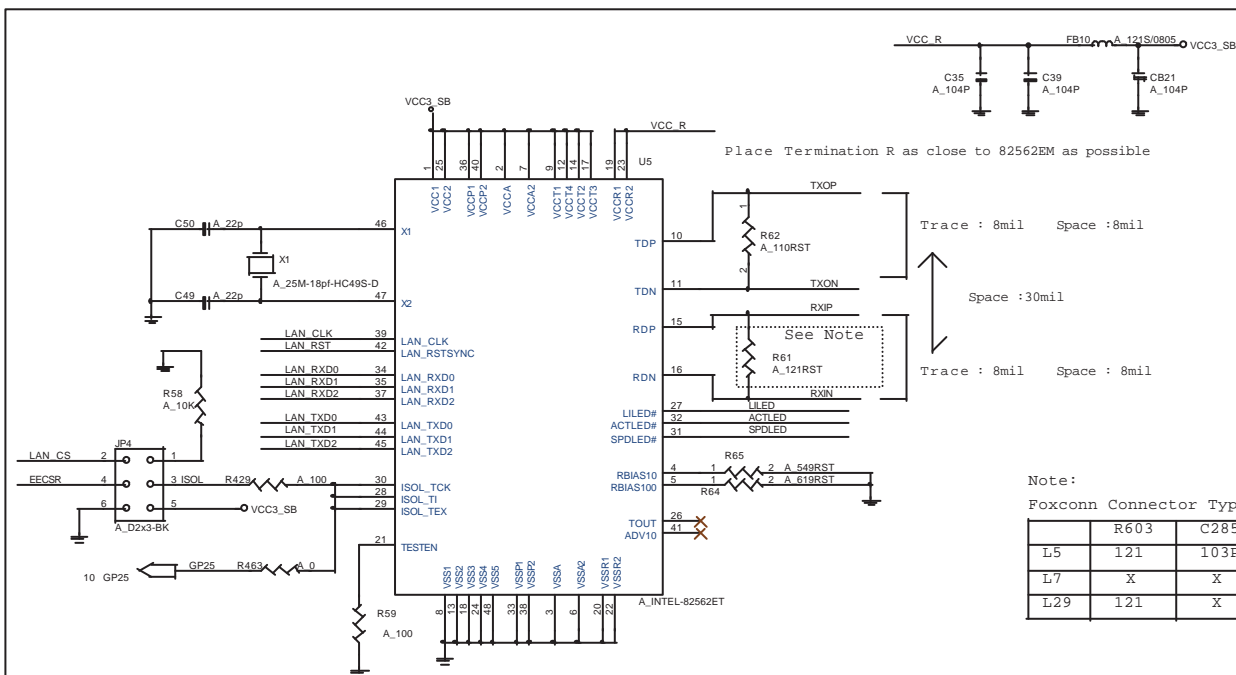
PS2 KEYBOARD & MOUSE CONNECTOR



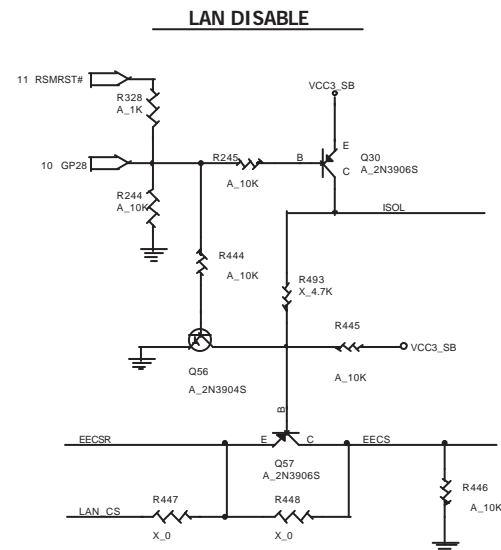
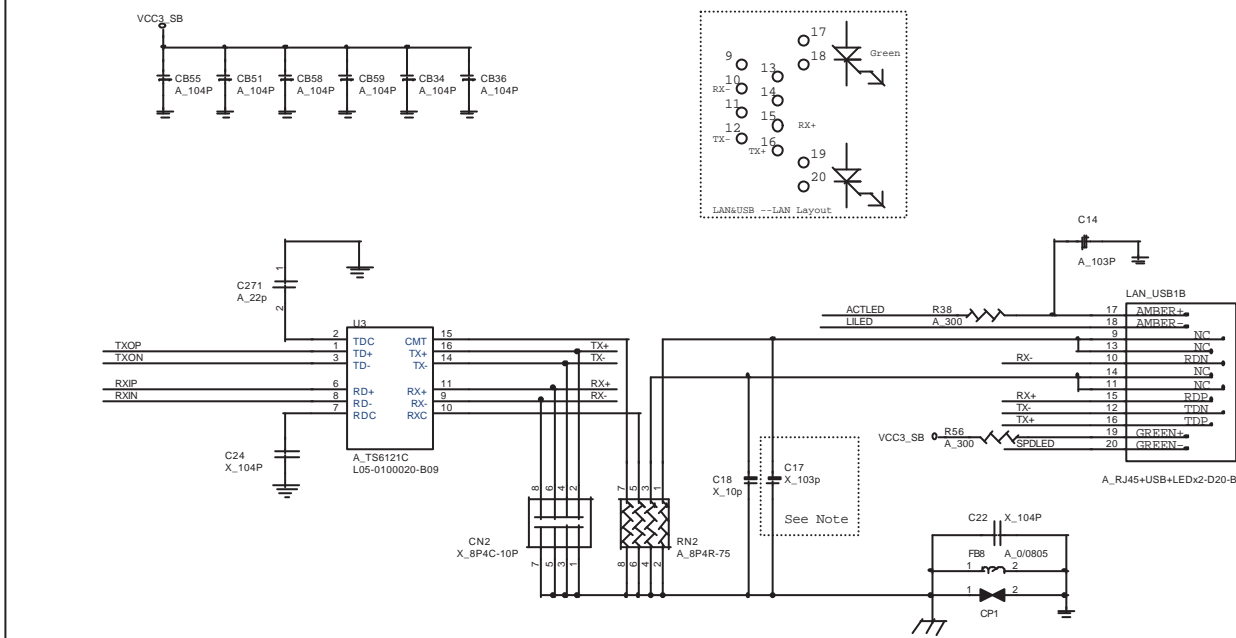
FLOPPY CONNECTOR



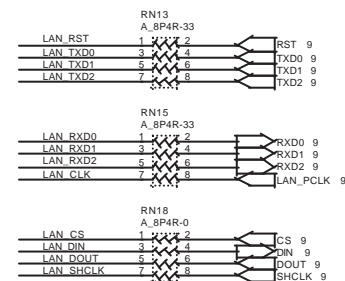
Micro-Star	Title	MS-6530	Rev
Document Number	IO Connector		
Last Revision Date:	Wednesday, July 04, 2001		
Sheet	24	of	33



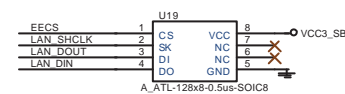
JP	ON BOARD LAN
1-3 / 2-4	ENABLE
3-5 / 4-6	DISABLE



LAN OPTION RESISTORS



LAN EEPROM



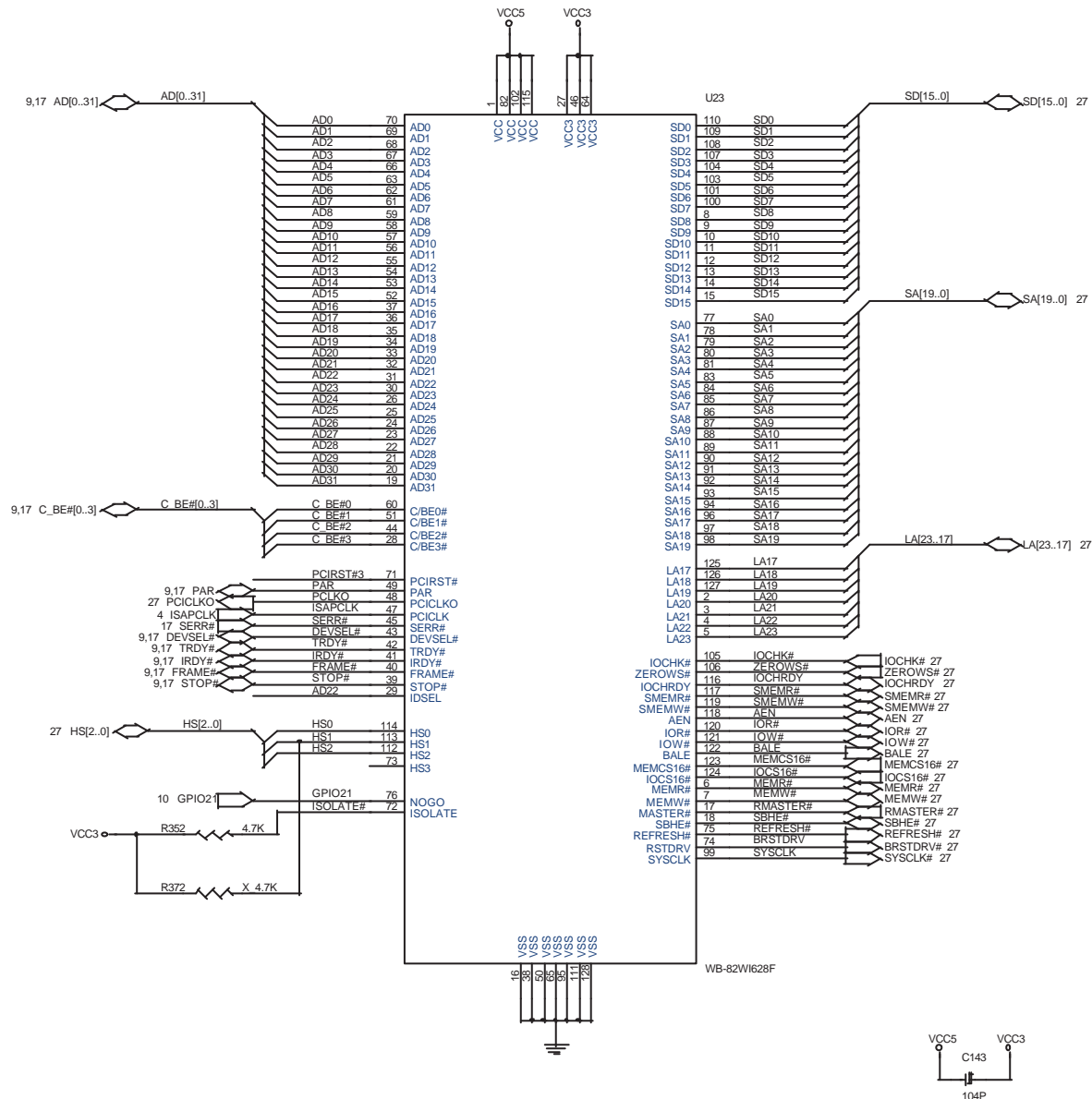
Remark:

82562EM with 93C66:M33-26N0103-A26

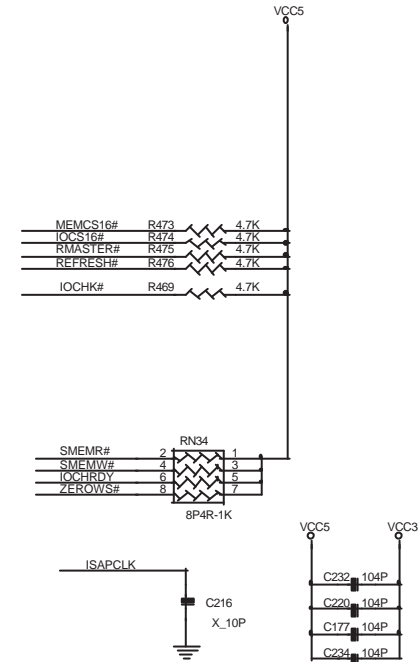
82562ET with 93C46:M33-1500203-A26 *

Micro-Star	Title	MS-6530	Rev	100
Document Number	LAN INTEL 82562EM/ET			
Last Revision Date:	Wednesday, July 04, 2001			
Sheet	25	of	33	

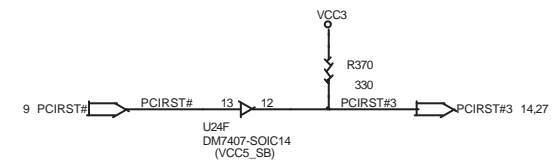
PCI To ISA Bridge, Part 1



PCI to ISA Bridge Pull Up / Low

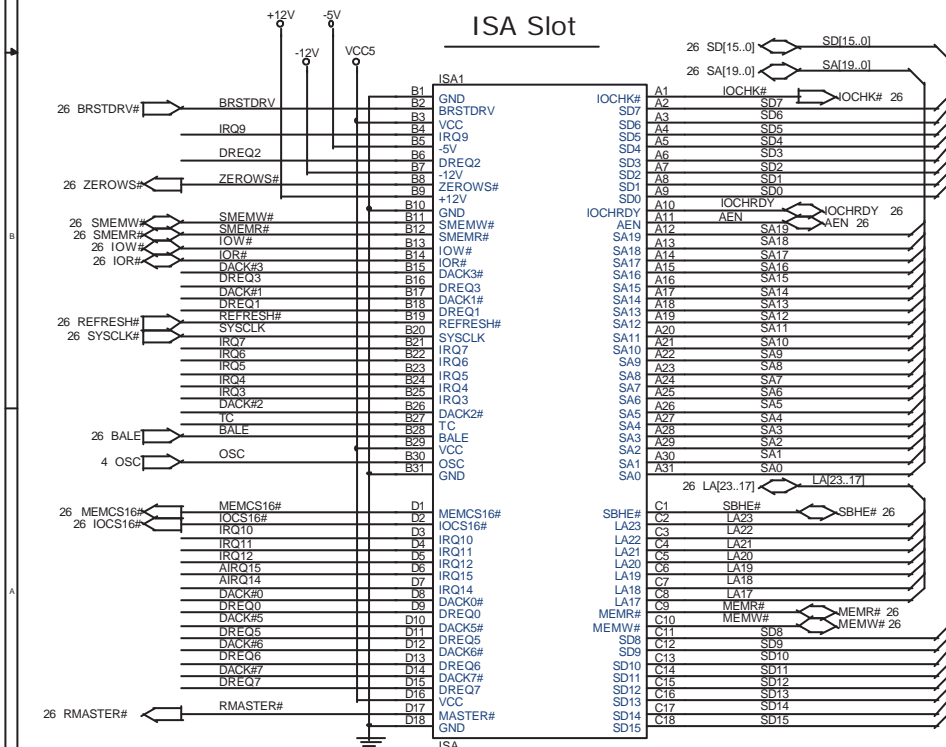
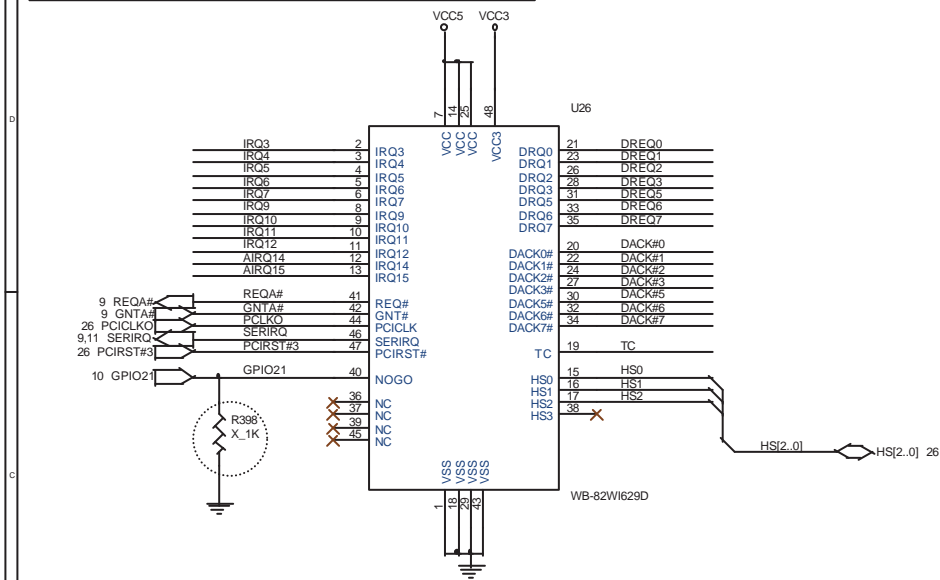


PCI to ISA Bridge Reset

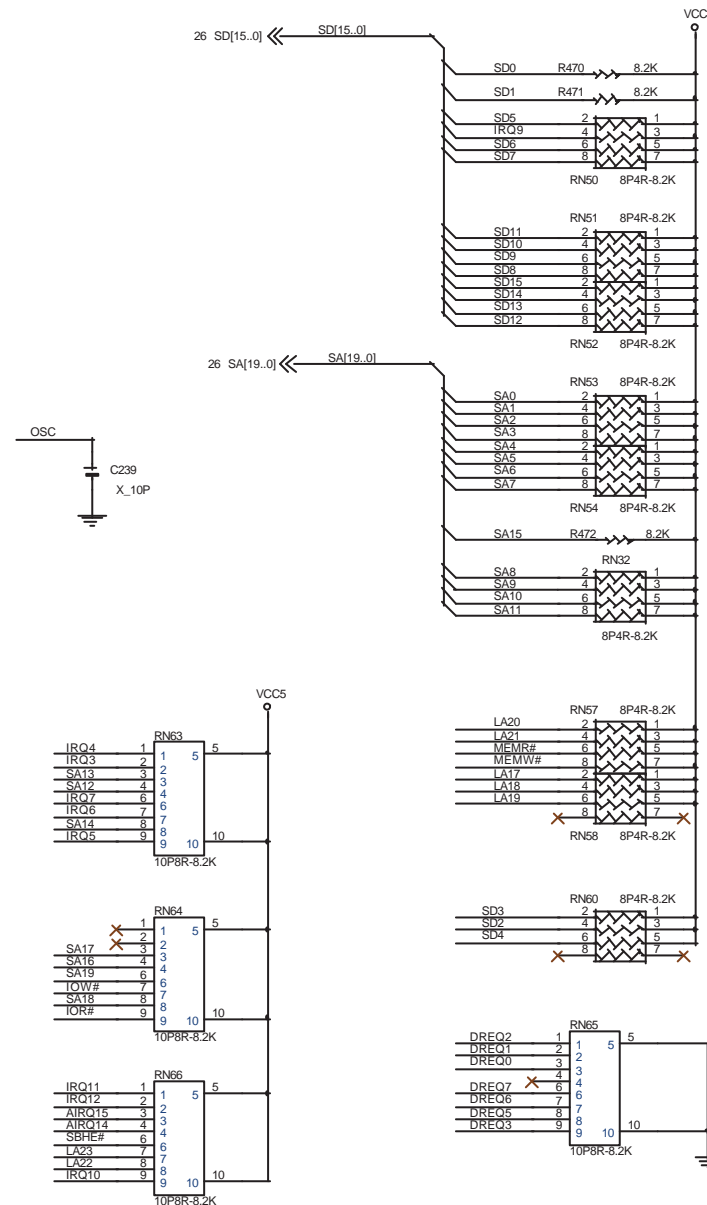


<i>Micro-Star</i>	Title	<i>MS-6530</i>	Rev	<i>100</i>
Document Number		ISA Bridge Part 1		
Last Revision Date: Wednesday, July 04, 2001		Sheet	26	of 33

PCI To ISA Bridge, Part 2



PCI to ISA Bridge Pull Up / Low



Micro-Star	Title	MS-6530	Rev	100
Document Number		ISA Bridge Part 2 / ISA SLOT		
Last Revision Date: Wednesday, July 04, 2001		Sheet	27	of 33

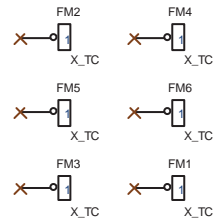
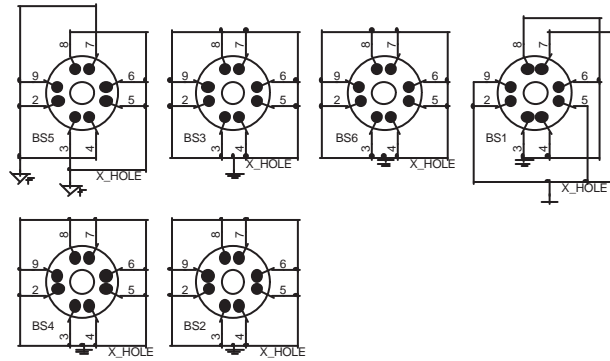
Jumper Setting & Connector Setting

Jumper	Description
J3	BIOS Protection function Open = Unlocked Short = Locked
J4	CHASSIS INTRUSION HEADER Low = Enable Hi = Disable
JBAT1	CLEAR CMOS 1-2 NORMAL (Default) 2-3 CLEAR CMOS
JP4	H/W Control On Board LAN Function Enable = Short 1-3 , 2-4 Disable = Short 3-5 ,4-6
JGS1	EXTSMI#

Connector	Description
U4	INTEL mPGA478-B CPU
IDE1 IDE2 FDD1	Primary Secondary Floppy
DIM1 DIM2	SDRAM DIMM1 SDRAM DIMM2
AGP1	AGP Slot
PCI1 PCI2 PCI3	PCI Slot1 PCI Slot2 PCI Slot3
COM1 COM2 LPT	Serial Port Serial Port Parallel Port
JMDM1 JWOL1	MODEM RING HEADER LAN WAKEUP HEADER
KBMS1 USB1 USB2	PS/2 Keyboard and PS/2 mouse USB REAR CONNECTOR USB INTERNAL HEADER
F_P1 IR1	Front Panel IR HEADER
POWER JPW1	ATX Power ATX12V Power
C_FAN1 S_FAN1 P_FAN1	CPU FAN HEADER SYS FAN HEADER ATX FAN HEADER
J2 JAUDIO1 CD_IN1 MDM_IN1	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN) AUDIO HEADER FOR LEGEND CD IN HEADER MODEM_IN HEADER

Micro-Star	Title MS-6530	Rev 0A
Document Number JUMPER SETTING		
Last Revision Date: Wednesday, July 04, 2001		Sheet 28 of 33

PCB OTHER COMPONENT



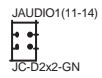
SIMULATION TRACE



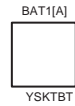
JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS



LEGEND AUDIO



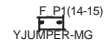
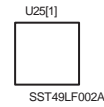
BAT SOCKET



J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *



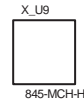
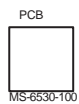
BIOS



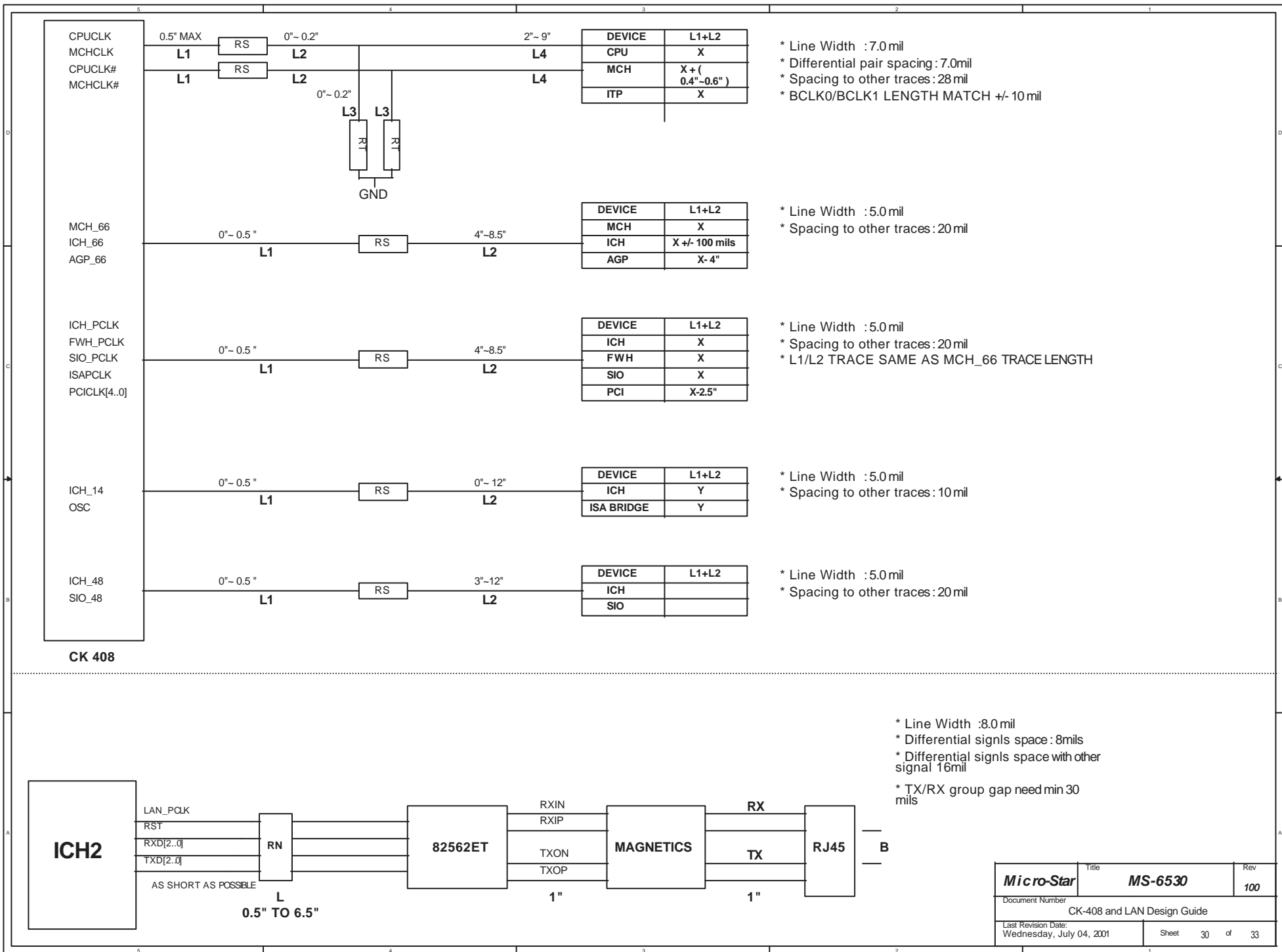
JP4 ON BOARD LAN	
1-3 / 2-4	ENABLE
3-5 / 4-6	DISABLE

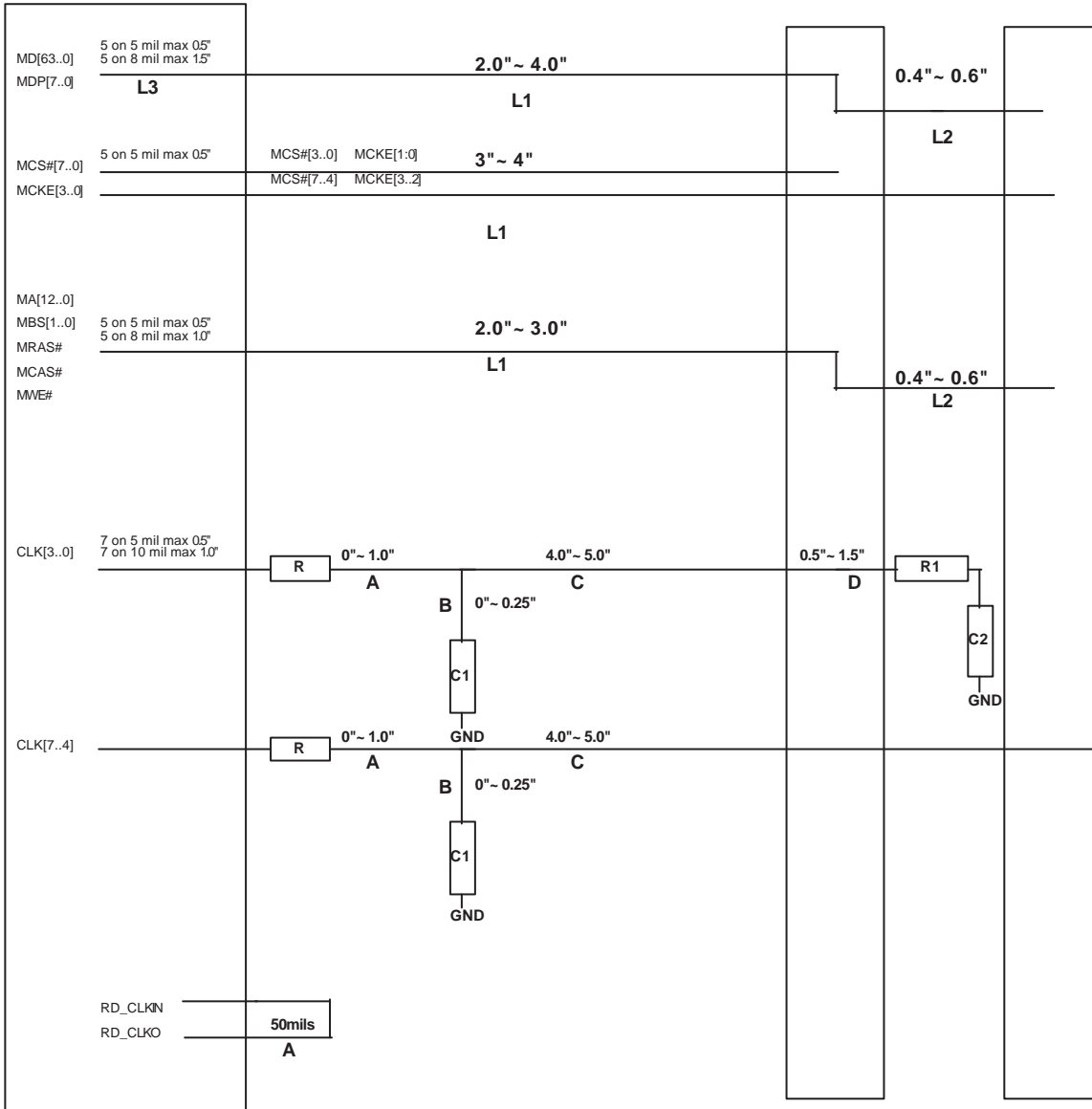


MS6530 PCB



Micro-Star	Title	MS-6530	Rev	100
	Document Number	MANUAL		
	Last Revision Date:	Wednesday, July 04, 2001	Sheet	29 of 33





* Trace Width : 5 mils
* Trace spacing : 12 mils

* Trace Width : 5 mils
* Trace spacing : 12 mils
MCS#
* Trace Width : 10 mils
* Trace spacing : 12 mils
MCKE

* Trace Width : 5 mils
* Trace spacing : 12 mils

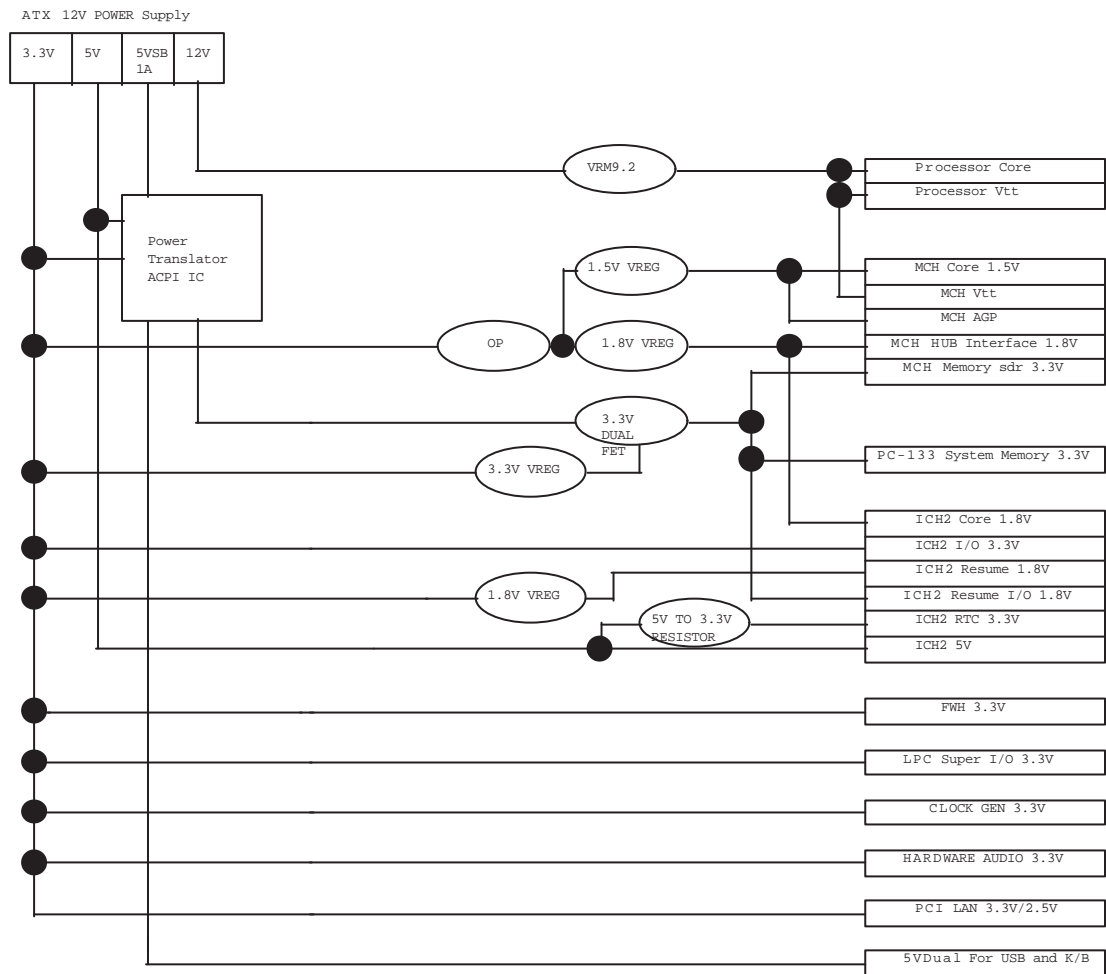
* Trace Width : 7 mils
* Trace spacing : 20 mils
* A+C < 5.9" +/- 0.05"
* 5.85" < A+C+D < 5.95"

RD_CLKIN
RD_CLKO
50mils
A

* Trace Width : 7 mils
* Trace spacing : 15 mils

Micro-Star	Title	MS-6530	Rev	100
	Document Number	PC133 DIMM DG		
	Last Revision Date:	Wednesday, July 04, 2001	Sheet	31 of 33

Power Delivery Map



Micro-Star	Title MS-6530	Rev 100
Document Number	Power Delivery Map	
Last Revision Date: Wednesday, July 04, 2001	Sheet	32 of 33

Revision	Date	Page	Description
0A	05/17/2001		Creat new schematics
1.0	07/03/2001	12	Add R462 for Modem-In (MONO_OUT) function . (Reserved for codec ADI1885)
			For audio PC2001 test : Delete CT40 , change C221 0.047uF->104pF and C217 104pF->0.047uF , add(reserved) R481 and R482 and C268 .
			Connect U20/pin41 to R214 , U20/pin39 to R213 for supporting ADI1885 phone-out function (ADI1885 integrated with apmlifier) .
			Add C269 , C270 , C266 , C267 for EMI issue .
		21	Add Intel CPU Thermal-stript circuit for future using .
		19	Connect F_P1/pin17 to "CLK_RST#" for solving H/W- reset issue .
		22	Add CT48 (1000uF/6.3V) at "VAGP_S" for "VCC_AGP" power stability .
		23	For "VCCP" stability change R104: 4.7k ->1.62KST ohm , add R113 = 470K ohm , delete R109 .
		25	Add R493 for auto(BIOS)-enable/disable LAN function . (Reserved)
			Add C271 for LAN EMI issue .
		8,23	For system stability add CB244 & CB245 at MCH's solder-side for "VCC_AGP" power , add CB246 & CB247 & CB248 at MCH's solder-side for "VCCP" power .

Micro-Star	Title	Rev
	MS-6530	100
	Document Number	
Revision History - 1		
Last Revision Date: Wednesday, July 04, 2001		Sheet 33 of 33