MH2M325CZJ/CNZJ-5,-6,-7

HYPER PAGE MODE 67108864-BIT (2097152-WORD BY 32-BIT) DYNAMIC RAM

DESCRIPTION

The MH2M325CZJ/CNZJ is 2097152-word × 32-bits dynamic RAM. This consists of four industry standard 2M × 8 dynamic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module,suitable for easy interchange or addition of modules.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH2M325CZJ/CNZJ-5	50	13	25	90	2620
MH2M325CZJ/CNZJ-6	60	15	30	110	2160
MH2M325CZJ/CNZJ-7	70	20	35	130	1900

- 72pin single in-line package
- Single 5.0V ±10% supply
- Low stand-by power dissipation
  22mW (Max) ····· CMOS input level
- Low operating power dissipation
  MH2M325CZJ/CNZJ- 5 ---------- 3.20W (Max)
  MH2M325CZJ/CNZJ- 6 ---------- 2.64W (Max)
  MH2M325CZJ/CNZJ- 7 ---------- 2.32W (Max)
- Hyper-page mode , $\overline{RAS}$-only refresh , $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- All inputs and output directly TTL compatible
  2048 refresh cycles every 32ms (A_0 ~A_{10})

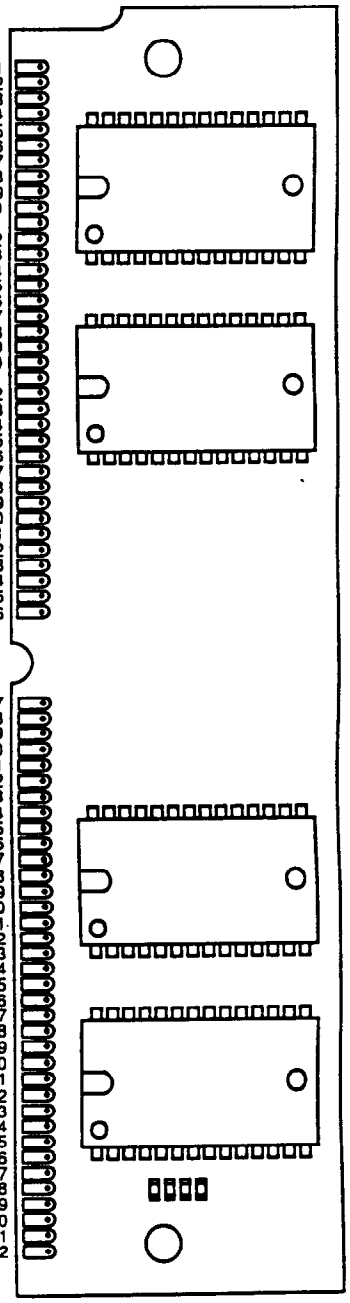
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)

[Single side]

1.Vss	37.NC	1	2
2.DQ0	38.NC	3	4
3.DQ16	39.Vss	5	6
4.DQ1	40.$\overline{CAS0}$	7	8
5.DQ17	41.$\overline{CAS2}$	9	10
6.DQ2	42.$\overline{CAS1}$	11	12
7.DQ18	43.$\overline{CAS3}$	13	14
8.DQ3	44.$\overline{RAS0}$	15	16
9.DQ19	45.NC	17	18
10.Vcc	46.NC	19	20
11.NC	47.$\overline{W}$	21	22
12.A0	48.NC	23	24
13.A1	49.DQ8	25	26
14.A2	50.DQ24	27	28
15.A3	51.DQ9	29	30
16.A4	52.DQ25	31	32
17.A5	53.DQ10	33	34
18.A6	54.DQ26	35	36
19.A10	55.DQ11		
20.DQ4	56.DQ27	37	38
21.DQ20	57.DQ12	39	40
22.DQ5	58.DQ28	41	42
23.DQ21	59.Vcc	43	44
24.DQ6	60.DQ29	45	46
25.DQ22	61.DQ13	47	48
26.DQ7	62.DQ30	49	50
27.DQ23	63.DQ14	51	52
28.A7	64.DQ31	53	54
29.NC	65.DQ15	55	56
30.Vcc	66.NC	57	58
31.A8	67.PD1	59	60
32.A9	68.PD2	61	62
33.NC	69.PD3	63	64
34.$\overline{RAS2}$	70.PD4	65	66
35.NC	71.NC	67	68
36.NC	72.Vss	69	70
		71	72



Outline 72N9X-C

	-5	-6	-7
PD0	NC	NC	NC
PD1	NC	NC	NC
PD2	Vss	NC	Vss
PD3	Vss	NC	NC

NC: NO CONNECTION

FUNCTION

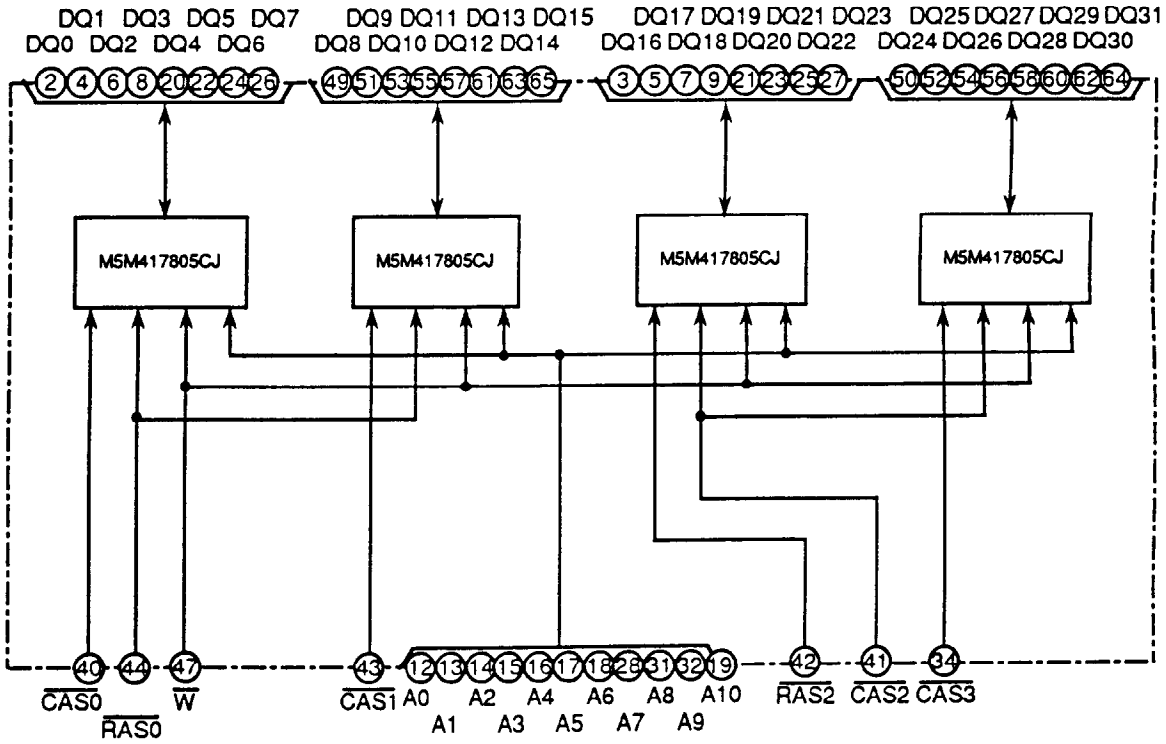
In addition to normal read, write, a number of other functions, e.g., hyper page mode, $\overline{RAS}$ only refresh, The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output
Read	ACT	ACT	NAC	APD	APD	OPN	VLD
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN
Hidden refresh	ACT	ACT	NAC	APD	DNC	OPN	VLD
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



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HYPER PAGE MODE 67108864-BIT (2097152-WORD BY 32-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1～7	V
V I	Input voltage		-1～7	V
V0	Output voltage		-1～7	V
I 0	Output current		50	mA
Pd	Power dissipation	Ta=25°C	4000	mW
Topr	Operating temperature		0～70	°C
Tstg	Storage temperature		-40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0～70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		5.5	V
V_{IL}	Low-level input voltage, all inputs	-0.5		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0～70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
Ioz	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	-10		10	μA
I I	Input current		0V≦V_{IN}≦6V, Other inputs pins=0V	-40		40	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	MH2M325C -5	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			580	mA
		MH2M325C -6				480	
		MH2M325C -7				420	
I_{CC2}	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =V_{IH}, output open			8	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2 V			4	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	MH2M325C -5	$\overline{RAS}$ cycling, $\overline{CAS}$= V_{IH} t_{RC}=min. output open			580	mA
		MH2M324C -6				480	
		MH2M325C -7				420	
I_{CC4}(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	MH2M325C -5	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			560	mA
		MH2M325C -6				460	
		MH2M325C -7				360	
I_{CC5}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH2M325C -5	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			580	mA
		MH2M325C -6				480	
		MH2M325C -7				420	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and $\overline{CAS}$=V_{IH} .

CAPACITANCE (Ta=0 ~ 70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance,address inputs	V_I=Vss f=1MHz V_I=25mVrms			30	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				35	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				23	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				23	pF
$C_{I/O}$	Input/Output capacitance, data ports				27	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			MH2M325C -5		MH2M325C -6		MH2M325C -7		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
tAA	Column address access time	(Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		13		15		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=-4.2mA) load 100pF.
The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{WEZ(max)}$,$t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ ±10 uA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~70℃, Vcc = 5V ±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		MH2M325C -5		MH2M325C -6		MH2M325C -7		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		32		32		32	ms
tRP	$\overline{RAS}$ high pulse width	30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	18	32	20	38	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width	8		10		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low (Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low (Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low	8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low	8		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		0		ns
tRDD	Delay time, RAS high to data (Note20)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data (Note20)	13		15		20		ns
tT	Transition time (Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed t_T =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH2M325C -5		MH2M325C -6		MH2M325C -7		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 22)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time	25		30		35		ns
tCAL	Column address to $\overline{CAS}$ hold time	13		18		23		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH2M325C -5		MH2M325C -6		MH2M325C -7		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width	8	10000	10	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	40		48		55		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		13		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	8		10		13		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		13		ns

Hyper page Mode Cycle (Read, Early Write, Read-Write, Read Write Mix Cycle, HI-Z control by $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		MH2M325C -5		MH2M325C -6		MH2M325C -7		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	20		25		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	57		66		79		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note24)	65	100000	77	100000	92	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note25)	8	13	10	16	13	16	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	28		33		38		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	43		50		60		ns
tCHOL	Hold time to maintain the data HI-Z until CAS access	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (HI-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	28		32		42		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	40		47		57		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	43		50		60		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

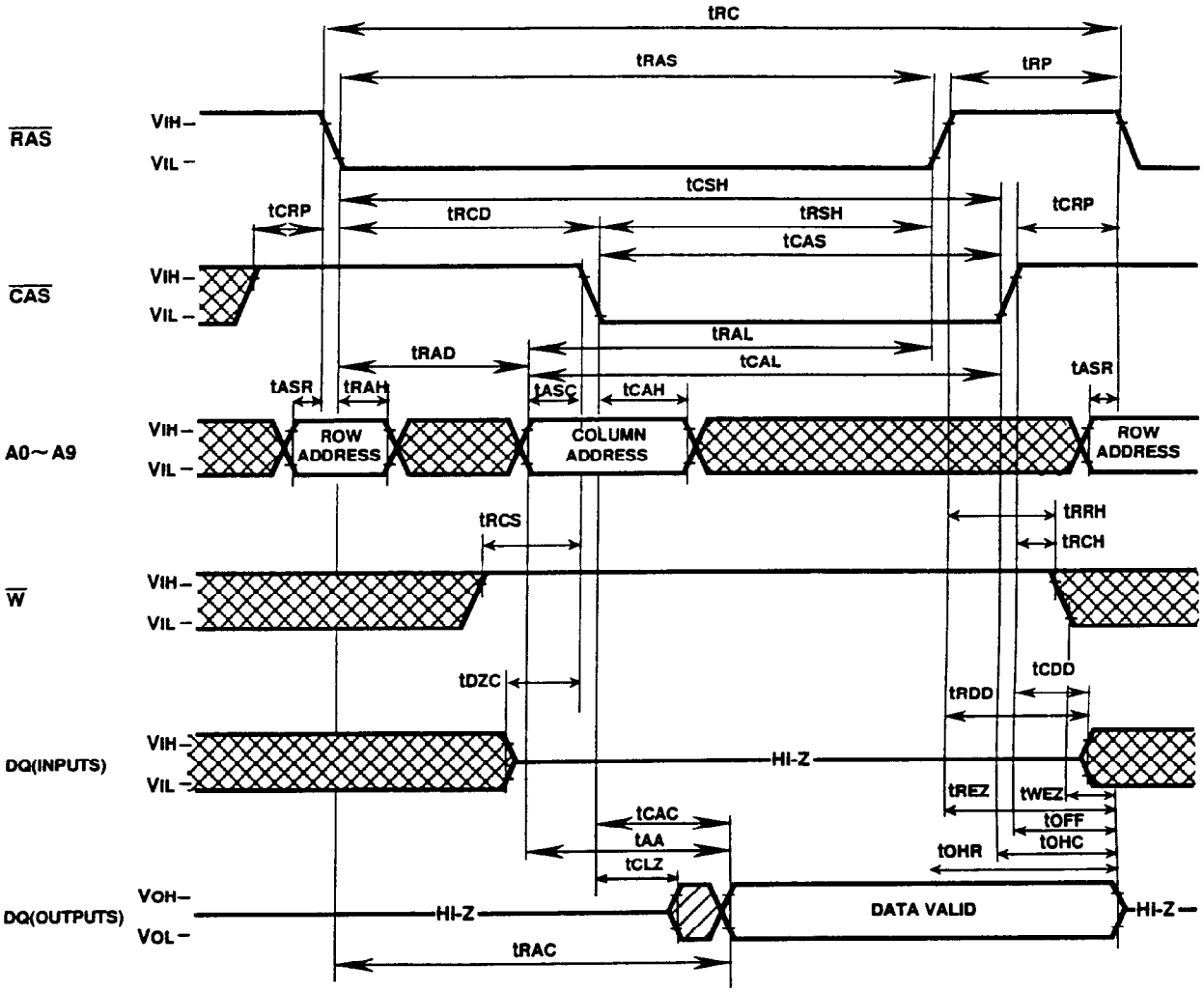
25: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		MH2M325C -5		MH2M325C -6		MH2M325C -7		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns

Note 26: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

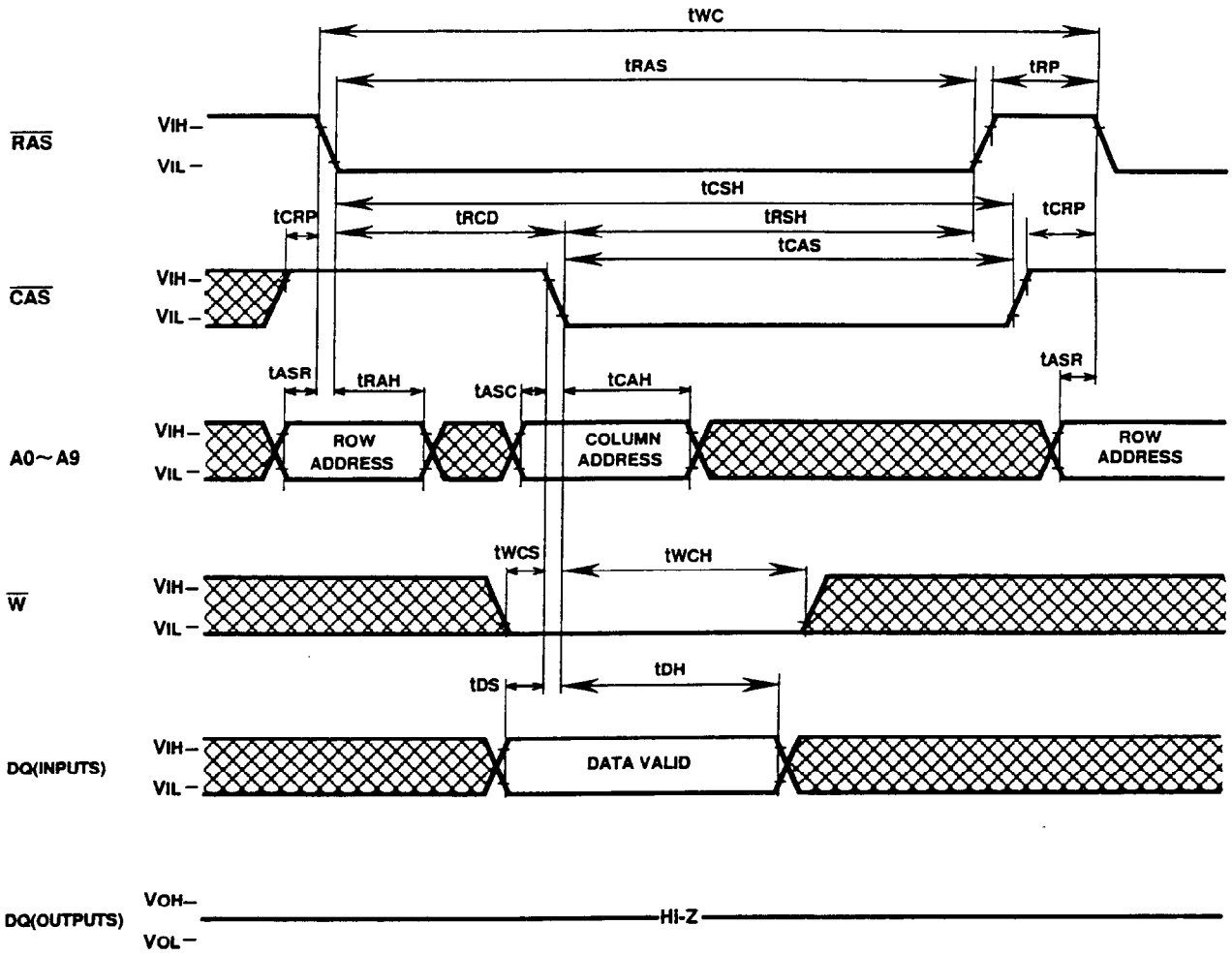
Timing Diagrams (Note 29)
Read Cycle



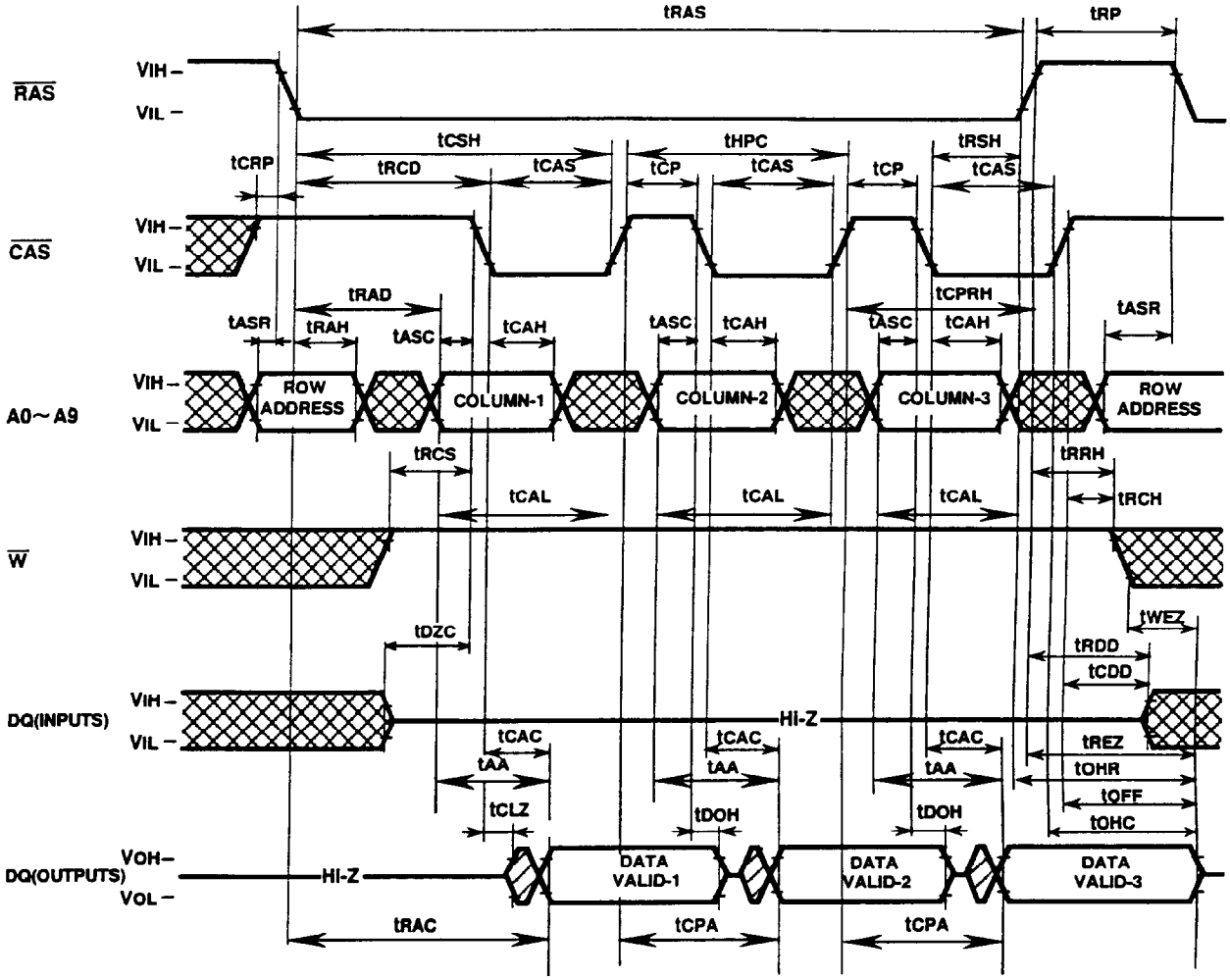
Note 29 Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output.

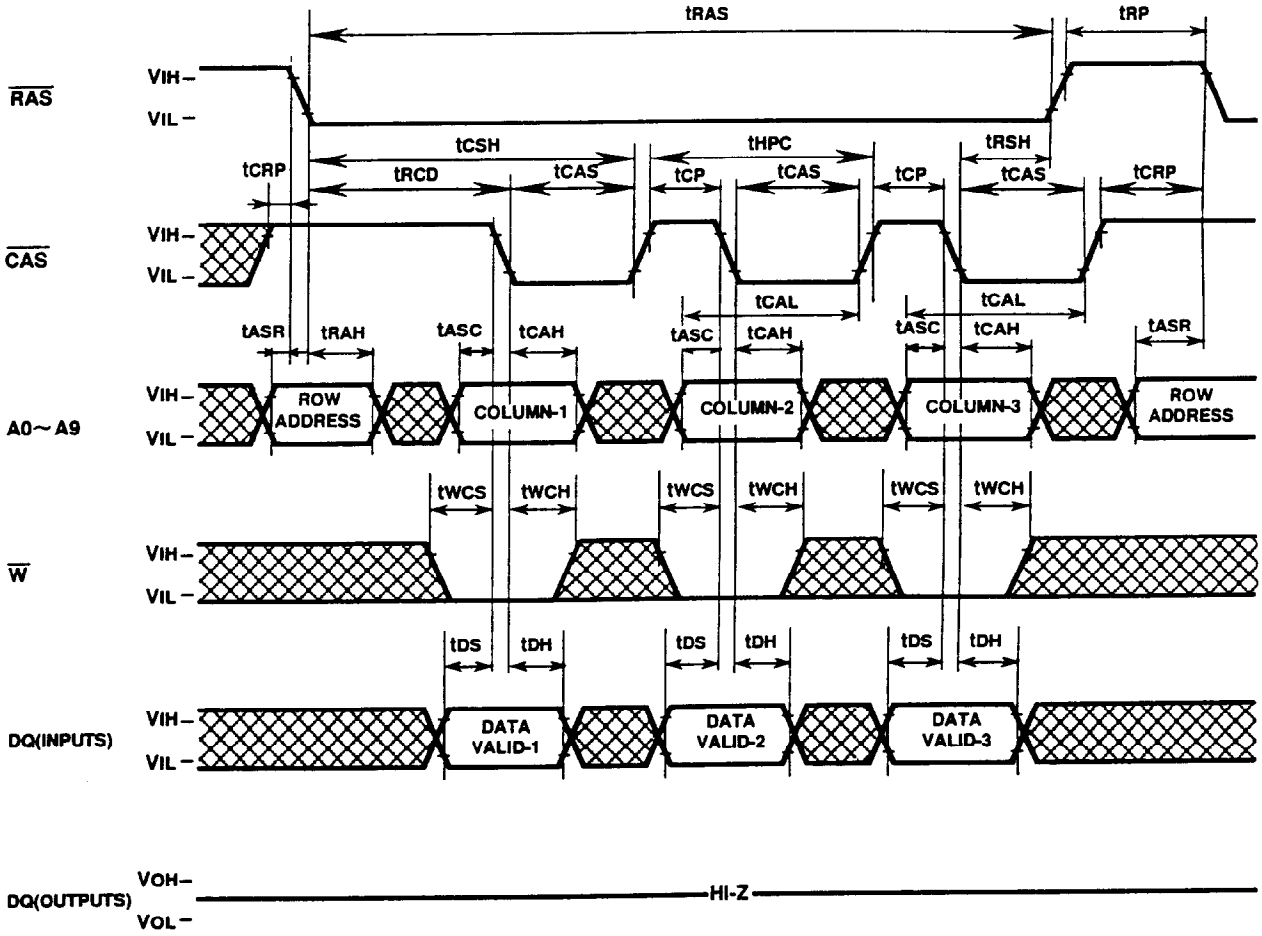
Early Write Cycle



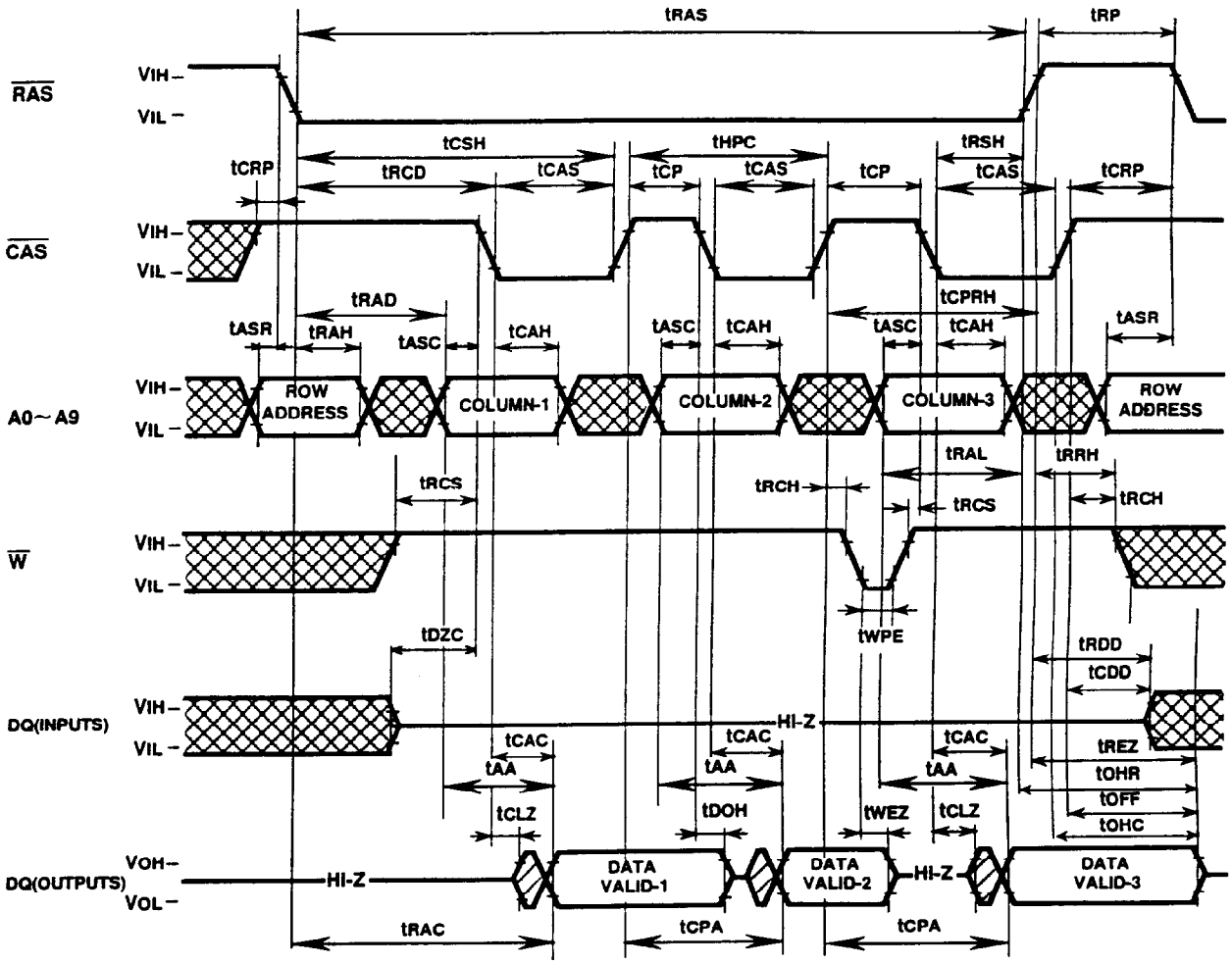
Hyper Page Mode Read Cycle



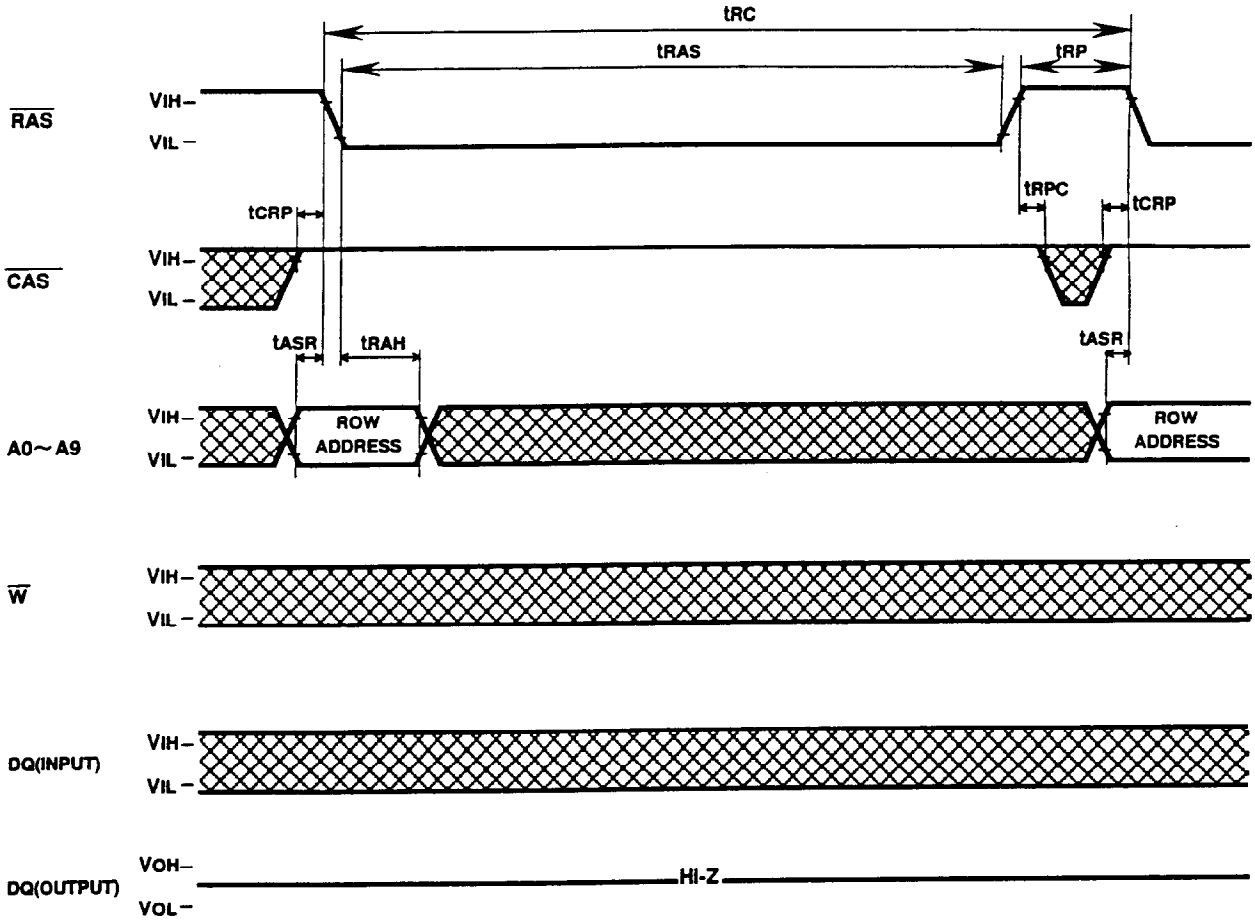
Hyper Page Mode Early Write Cycle



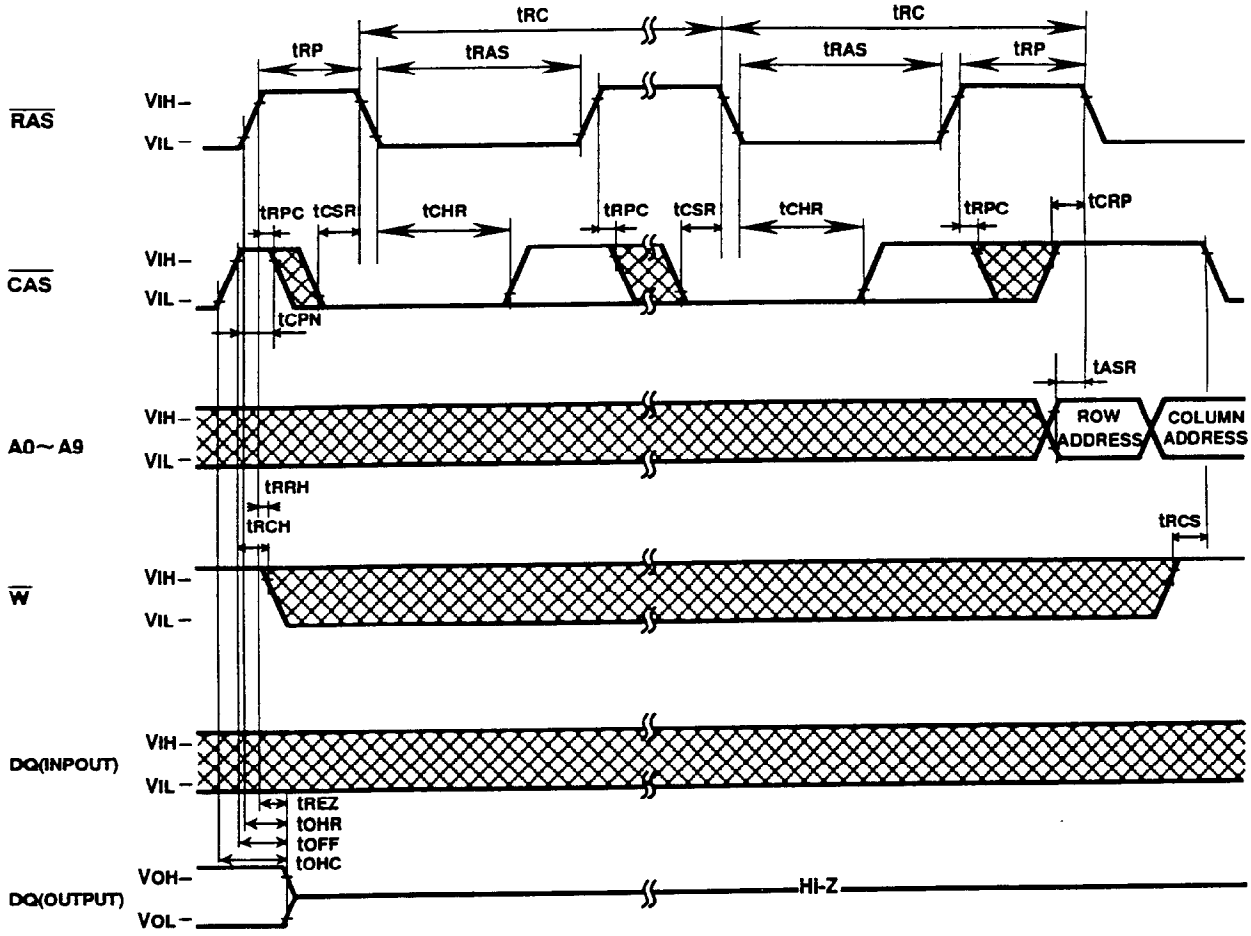
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



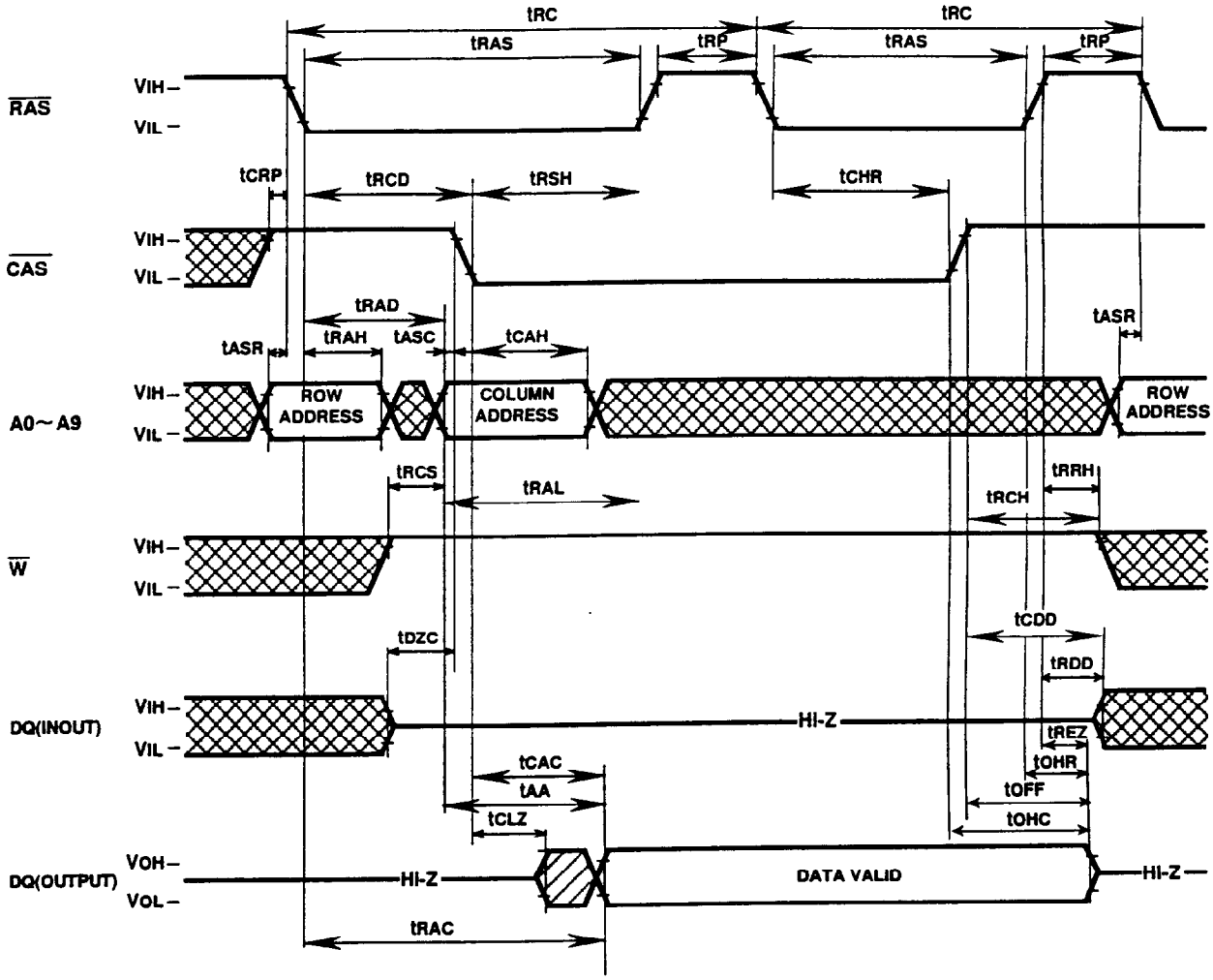
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

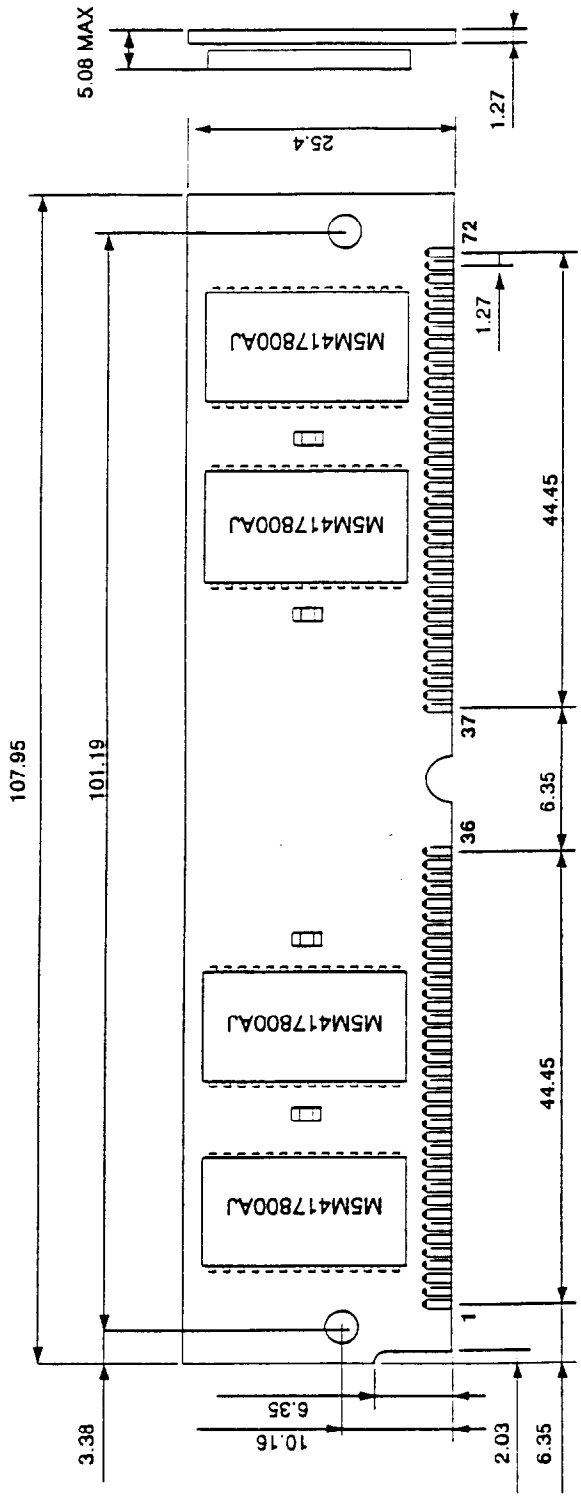


Hidden Refresh Cycle (Read) (Note 28)



Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

72pin DRAM Module Outline



Dimensions in mm