Award Modular BIOS v4.50G for Amptron DX-6900 ISA/VLB 486 board
09/08/95-UMC-498GP-2C4X6B13-00 Revision: 80486 UMC GREEN-PC BIOS VER 2.21r

CPU support list

Cmos_3Dh BIOS_uP_ID bit 0 = FPU	CPU string	Reset word	Other detection	Cmos_3Fh option flags	Detection sequence
00/01	Null				
02/03	"				
04/05	"				
06/07	80486DX	0400h – 041Fh/ 0 – FFFFh		00	10/ 13
08/09	80486SX	0420h – 042Fh		00	11
0A/0B	80486SX2/ 80486DX2	0430h – 04FFh	SX2+FPU -> DX2	40h	12/15
0C/0D	Null		Unkown CPU; Cx DIV OK; DIR0≠02h or 1Bh	00	16
0E/0F	"		80486SX; and Cx DIV OK	00	17
10/11	"				
12/13	"				
14/15	P24T		CPUID: Intel -> 1530h – 153Fh	58h	24
16/17	Cx486S	0440h – 0450h	Cx DIV OK and DIR0=12h	10h	8/3
18/19	Cx486S2	0451h – 0451h	Cx DIV OK and DIR0=13h	50h	9/4
1A/1B	Null				
1C/1D	"				
1E/1F	"				
20/21	"				
22/23	"				
24/25	Cx486DX		Cx DIV OK and DIR0=1Ah	10h	5
26/27	Cx486DX2 TI486DX2		Cx DIV OK and DIR0=1Bh TI if DIR1 bit 7=1	50h	6
28/29	Null		Unkown CPU; Cx DIV OK; DIR0=02h or 1Bh	50h	16
2A/2B	DX4		CPUID: Intel -> 0480h – 048Fh/ 1480h – 148Fh/ 0490h – 049Fh/ 1490h – 149Fh	90h 90h 98h 98h	20 21 22 23

2C/2D	TI486SXL		uP_ID 0Eh+TI test	10h	18
2E/2F	TI486SXL2		TI486SXL x2 test	50h	35
30/31	U486SX		FS: SALC -> EAX=AB6B1B07h CPUID: UMC -> 0420h – 042Fh	10h 10h	14 29
32/33	Am486DX				
34/35	Null				
36/37	TI486SXLC		80486SX+TI test	10h	18
38/39	TI486SXLC2		TI486SXLC x2 test	50h	35
3A/3B	Am486DX2				
3C/3D	P24D		CPUID: Intel -> 0470h – 047Fh	58h	19
3E/3F	Am486DX4		DX4 + non-green; DX2 ≤ 90MHz	80h	33 34
40/41	Null				
42/43	Enhanced Am486DX2		CPUID: AMD -> 0430h – 043Fh 0470h – 047Fh	50h 58h	25 26
44/45	Enhanced Am486DX4		CPUID: AMD -> 0480h – 048Fh 0490h – 049Fh	90h 98h	27 28
46/47	U486SX2		CPUID: UMC -> 0450h – 045Fh	50h	30
48/49	U486DX		CPUID: UMC -> 0410h – 041Fh	10h	31
4A/4B	U486DX2		CPUID: UMC -> 0430h – 043Fh	50h	32
4C/4D	Cx5x86		Cx DIV OK and DIR0=29h/2Bh DIR0=2Dh/2Fh	50h 90h	1 2
4E/4F	CxDX4		Cx DIV OK and DIR0=1Fh	90h	7
50/51	Null				
52/53	"				
54+	Unknown				

CMOS registers bit definition:

Bits 6-0 in the **CMOS_3D_uP_ID** byte represent the BIOS_uP_ID. A “1” in bit 7 means that a L1 cache is present, while bit 0 indicates if the CPU has a build-in FPU.
The bits in **CMOS_3Fh** byte represent additional CPU data:

Bit 7 = clock tripling CPU
Bit 6 = clock doubling CPU
Bit 5 = reserved (used for clock quadrupling CPU in later BIOS versions)
Bit 4 = Green CPU
Bit 3 = CPU in L1 cache Write-Back mode
Bits 2-0 are reserved.

Notes on software tests:

- FPU: A test to determine if the CPU has a Floating Point Unit (=Math coprocessor).
- Cx DIV: This is a test that identifies a Cyrix CPU, including IBM, ST, and TI CPUs based on the Cyrix design. These CPUs do not change unrelated flags in the Flags Register after a Divide operation. CPUs from other vendors do.
- DIR0: Device Identification Register 0 is present on all Cyrix design CPUs, except the Cx486S A-step. Its contents can be used to identify a specific Cyrix processor.
- TI test: This is a sequence of instructions acting on the test registers TR4 and TR5 that produces a specific result only on TI CPUs.
- FS: SALC: This undocumented instruction with opcodes 64h, 0D6h, produces a specific result in the EAX register only on UMC CPUs.
- CPUID: This instruction returns detailed information about a CPU. CPUID is supported by the Pentium and a handful of later 486’s. So most 486 CPUs don’t support this instruction and a more widespread use of CPUID is seen only in 1995 and later Award BIOSes.