Advance Information

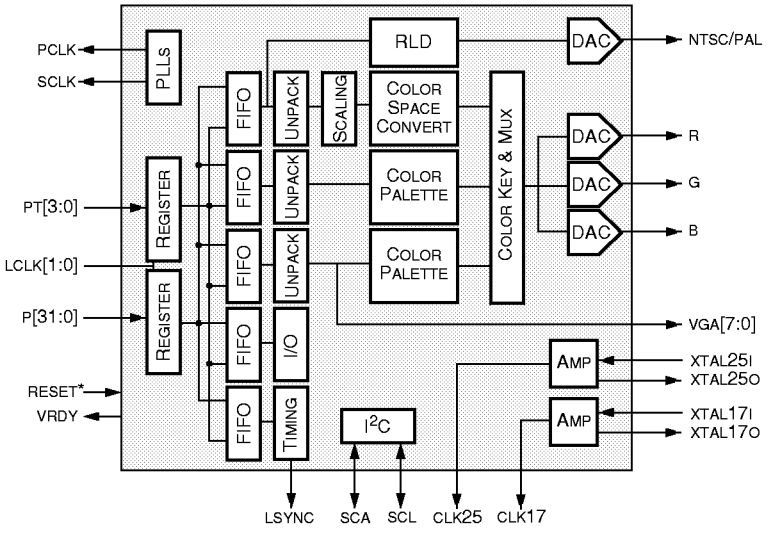
This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

BtV2487

PACDAC™ Packetized Data DAC

The BtV2487 Packetized Data DAC (PACDAC™) when used in conjunction with the BtV2115 MediaStream Controller, provides a fully integrated graphics and video subsystem, specifically targeted at multimedia applications. The MediaBuffer (BtV multimedia sub-system memory) sits in between the BtV MediaStream Controller and the PACDAC. To maximize storage efficiency and bandwidth between the MediaBuffer and the PACDAC, the MediaStream family incorporates the MediaPacket Architecture, a patented technique for managing the flow of graphics, video, cursor and control to the PACDAC. This unique architecture incorporates packet-style data flow from the MediaBuffer to the PACDAC such that graphics and video can utilize the entire serial bandwidth available from the MediaBuffer. Normally during horizontal and vertical blanking, the serial port is not providing serial data to the DAC and is inactive. This inactive time can represent up to 30% of the total horizontal line time. To take advantage of this time, the PACDAC contains internal FIFO's that can be filled during this inactive time. Furthermore, color space conversion bilinear interpolative scaling filters on the PACDAC reduce CPU software overhead and minimizes both the MediaBuffer Storage and bandwidth requirements. This results in video playback capabilities beyond that which could otherwise be done as a result of increased effective bandwidth between the MediaBuffer and the PACDAC.

Functional Block Diagram



Distinguishing Features

- Bilinear Interpolative Scaling for Video
- YCrCb to RGB Color Space Conversion
- 1024x768x8 Graphics and 1024x768x24 30 fps Video in 1 MB of Memory
- Embedded Chroma/Color Keying for games development and virtual reality apps
- Two full screen, 30 fps Video Windows, Playback or Live
- NTSC/PAL Output Capability
- 4:2:2, 4:1:1 YCrCb or RGB 15,16,24-bit Video Support
- PLL Pixel and Serial Clock Generation
- 135 Mhz Operation
- Multiple Pixel Depths Supported, 4-bits to 32-bits per pixel
- True Color Cursor Support
- Asynchronous, Packetized Data Input Port
- VGA Output Port

Related Products

- BtV2115 – MediaStream Controller
- BtV2811 – VideoStream Decoder
- BtV2300 – AudioStream Interface

Applications

- Video for Windows
- Video Printing
- High Resolution Color Graphics
- Videoconferencing Display Systems
- Multimedia Applications
- Video Decompression Acceleration

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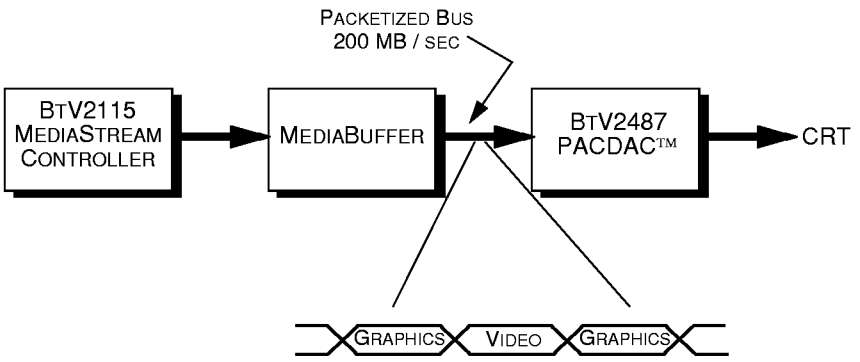

Because the graphics frame buffer and the video frame buffer(s) are logically separated within the physical MediaBuffer, each may reside in its own color space. The PACDAC performs the necessary color space conversions and scaling needed to generate the analog RGB outputs. The graphics buffer does not need to conform to the color depth of the video buffer, as is the case with competing solutions, thus resulting in more efficient use of MediaBuffer memory space. For example, a 1M memory configuration can support 1024 x 768 x 8 or 1280 x 1024 x 4 graphics while also supporting true color video playback at any arbitrary video window size. Another benefit of separate video and graphics storage areas is that higher video quality can be maintained even when graphics is operating in pseudo color modes. This is because graphics can be maintained in pseudo color space (4 or 8 bits per pixel) while still allowing the video buffer to be in video color space (true color - YCrCb). This improves the quality of the video presentation and eliminates palletized video commonly seen in other video implementations.

The packet interface and associated PACDAC FIFO's decouple the frame buffer's serial clock (SCLK) from the pixel clock (PCLK) of the PACDAC. Normally, the data rate that the frame buffer feeds pixel data to the RAMDAC must be matched to the pixel clock requirements. This is usually accomplished either by dividing the pixel clock (PCLK) or using a PLL to generate a synchronous serial clock to the frame buffer, depending on the specific multiplexing provided by the RAMDAC. This wastes considerable available bandwidth from the serial port. For example, a RAMDAC with a 135 MHz pixel clock and a 4:1 input multiplexer sets the serial clock at 33.75 MHz (135/4). With 50 MHz serial rate frame buffers, this results in 16.25 MHz of wasted bandwidth -- 33% of its capabilities.

Another source of unused bandwidth in conventional architectures may be found in the "dead" time of horizontal scan lines. Since no pixels are generated during horizontal retrace, the frame buffer serial port is inactive during this time. Because pixel data is synchronized within the PACDAC using FIFO buffers, this unused bandwidth is now available for transfer of additional graphics, cursor, or video data.

The packet interface takes advantage of this unused bandwidth to provide enhanced video capability. The PACDAC will support up to a 75 MHz SCLK so as higher speed frame buffers are introduced in the market, the increased bandwidth becomes instantly available to the BtV system.

In MediaStream systems, memory space in addition to memory bandwidth is also efficiently managed. For example, when displaying full motion video windows, the MediaBuffer only needs to store the video in its native size (for example 320 x 240). Full bi-linear interpolation is performed within the PACDAC to scale to larger windows minimizing both the MediaBuffer storage and bandwidth demands.

Since only the amount of MediaBuffer required for the desired feature set needs to be provided, feature-rich implementations may be configured using minimum memory. This represents a cost advantage over other DRAM and VRAM solutions by halving the memory requirements for this base line configuration.

The MediaStream Controller provides graphics performance that satisfies the needs of today's GUI environments such as Microsoft Windows. Integrated with the latest in GUI accelerator hardware, the MediaStream Controller provides a full compliment of graphics primitives. Graphics hardware acceleration is provided for a full range of pixel formats and pixel depths from 640 x 480 x 24 through 1280 x 1024 x 16.

From its inception, The BtV MediaStream family was designed with video in mind. The BtV MediaStream family incorporates the video functions necessary for a wide variety of multimedia applications -- from basic video playback to full multimedia authoring applications. Features range from highly efficient video playback acceleration to NTSC I/O options to a unique chroma-key capability.

As video playback in PC's becomes a standard and required feature, video quality will become a differentiating factor among PCs. The MediaStream Controller provides full motion video acceleration under Microsoft's Video for Windows (VfW). The controller accelerates up to two native format 30 fps 320 x 240 resolution VfW sessions including bi-linear interpolation for scaling to window size. For non-accelerated VfW playback, the number of video windows is only limited by the available MediaBuffer space.

The BtV MediaStream family contains hardware for accelerating software video decompression by off loading the time consuming color space conversion and scaling operations from the system CPU. The MediaStream controller provides multiple virtual frame buffer views into the same physical memory, allowing transparent bit, byte, word, and dword order flipping, as well as video component access. This allows software algorithms to take advantage of the CPU's large block move instructions rather than having to manually perform the component reordering within the innermost loops of the decompression algorithm. Depending on the algorithm, pixel throughput increases of 2-10 times are achievable over conventional linear-only frame buffer architectures. These features are important because an excess of 40% of processor time is spent in color space conversion and display management. In a MediaStream family system, the processor is off-loaded from much of this function allowing more processor cycles for multitasking chores. All color space conversion and scaling of video is performed right before data conversion in the PACDAC for maximum system and CPU efficiency. and maximum color fidelity.

Brooktree's BtV MediaStream family display drivers include the Microsoft's Display Control Interface (DCI) extensions that allow DCI compliant video decompression algorithms to efficiently take advantage of the MediaStream family's video acceleration capabilities. For older decompression algorithms that do not conform to DCI, Brooktree provides the capability to wrap DCI functionality around them. Thus, even older decompression algorithms that do not conform to DCI enjoy substantial acceleration within a BtV MediaStream system.

The PACDAC video path is also capable of handling RGB data. This ability can greatly enhance popular 3-D applications such as games. Using the PACDAC's interpolative scaling filters, 3-D games running under Windows can be up-scaled from their original 320 X 200 dimensions to any arbitrary window size and still keep their maximum frame rate and color fidelity.

The BtV MediaStream family provides a unique video acceleration feature that is ideally suited to leading edge video applications. Chroma-keying provides the ability to overlay a video source on top of a graphics display for applications ranging from high-performance gaming to virtual reality. Chroma-keying is based upon the application of a single bit alpha mask which when embedded in the video bit stream to the MediaStream Controller, provides the video keying necessary to overlay the video on top of the graphics display. To take advantage of MediaStream family chroma-keying, an alpha mask that identifies the extents of the video overlay must be created and encoded with the video stream when the application is authored. By doing this, playback of the keyed video is handled automatically in MediaStream hardware during playback. The BtV MediaStream family chroma-keying allows very complex keying to be embedded directly in the video stream that adds realism to high-performance games and virtual reality applications.

Live video display is handled extremely efficiently by the BtV MediaStream system. This can best be illustrated by comparing the flow of video within a traditional controller system versus the flow of video within a MediaStream system. Video, usually in component video format (YCbCr) is generated by a NTSC/PAL decoder (such as the BtV2811). The resultant video is written into an off-screen video buffer within the graphics subsystem. The controller is then responsible for color space converting (to RGB format), scaling, and rendering into the display frame buffer. For full frame rate video to occur, this must be done at 30 frames per second. This can result in required data rates in excess of 50 million bytes per second between the controller and the frame buffer (assuming full screen 1024 x 768 at 30 fps). Because this bandwidth is seldom available, compromises are made by reducing the frame update rate so that "jerky" video results. This consumption of bandwidth also cannibalizes the bandwidth normally available for graphics functions. As a result, graphics performance suffers when one or more video windows are displayed.

The BtV MediaStream family provides a more elegant solution. The MediaStream Controller and the PACDAC work in concert to bring video to the screen. The PACDAC contains on-chip FIFO's for graphics, cursor and video, on-chip color space conversion, and full arbitrary size bilinear X-Y interpolators for scaling to

fit any window size. As a result, only the bandwidth necessary to fill the video buffer is consumed on the DRAM port of the MediaBuffer. For a SIF resolution video stream at 30 fps, this is only 4.6M bytes per second. This results in approximately 95MB per second of unused bandwidth available for other functions such as graphic and/or additional video windows.

The BtV MediaStream family provides a unique ability to encode AVI or other video file formats for presentation on an NTSC/PAL composite video output from the PACDAC. This option is ideal for recording video from a Video for Windows (VfW) file to a standard VCR or playing an AVI file on a TV monitor.

Composite video encoding is achieved using a combination of software and hardware that encodes each frame of a video file sequence into a composite NTSC or PAL wave form. The result is output through a digital-to-analog converter (DAC) on the BtV2487 for NTSC or PAL video output. The size and format of the encoded video is 160 x 120 pixels in 4:1:1 video format.

Another capability with the BtV MediaStream family is a window-to-video output option. This feature allows a selected screen element to be output on the composite output pin of the PACDAC at typically 2-3 updates per second on a 486DX2-66. This feature is useful for recording to video tape or delivering presentations on TV monitors or projection systems.

At regular intervals, a background software task encodes the secondary buffer into a composite video wave form which the PACDAC outputs in standard NTSC or PAL video format. Any rectangular area up to 640x480 pixels of the graphics frame buffer may be selected for encoding. Since the encoding is performed entirely by software, video quality scales with processor power and can be traded for update rates. For example, the quality of filtering functions, such as flicker filtering can be balanced with the desired video update rate for optimum use. With the addition of frame-accurate computer-controlled VCRs or writable disk recorders, extremely high quality video animation sequences can be recorded.

Ordering Information

Part Number	Speed (MHz)	Package
BtV2487ASF	135	100-pin Power Quad
BtV2487CHF	135	100-pin MQFP

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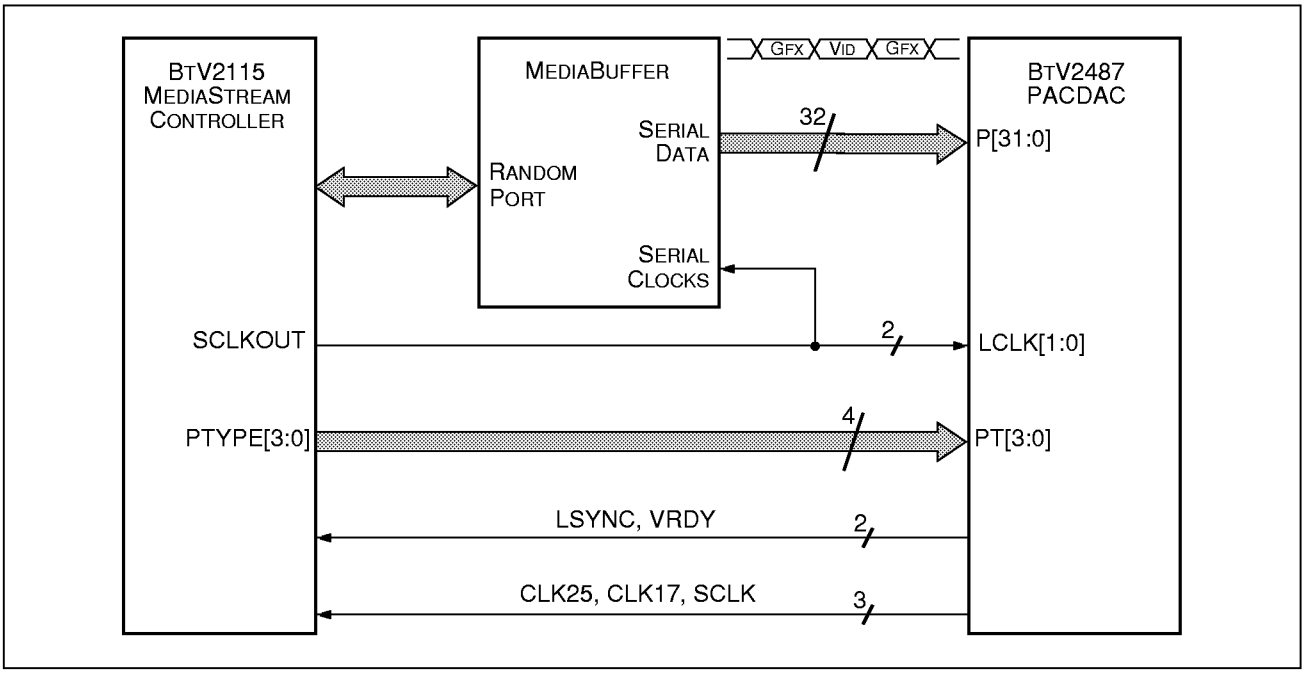
CIRCUIT DESCRIPTION

Introduction

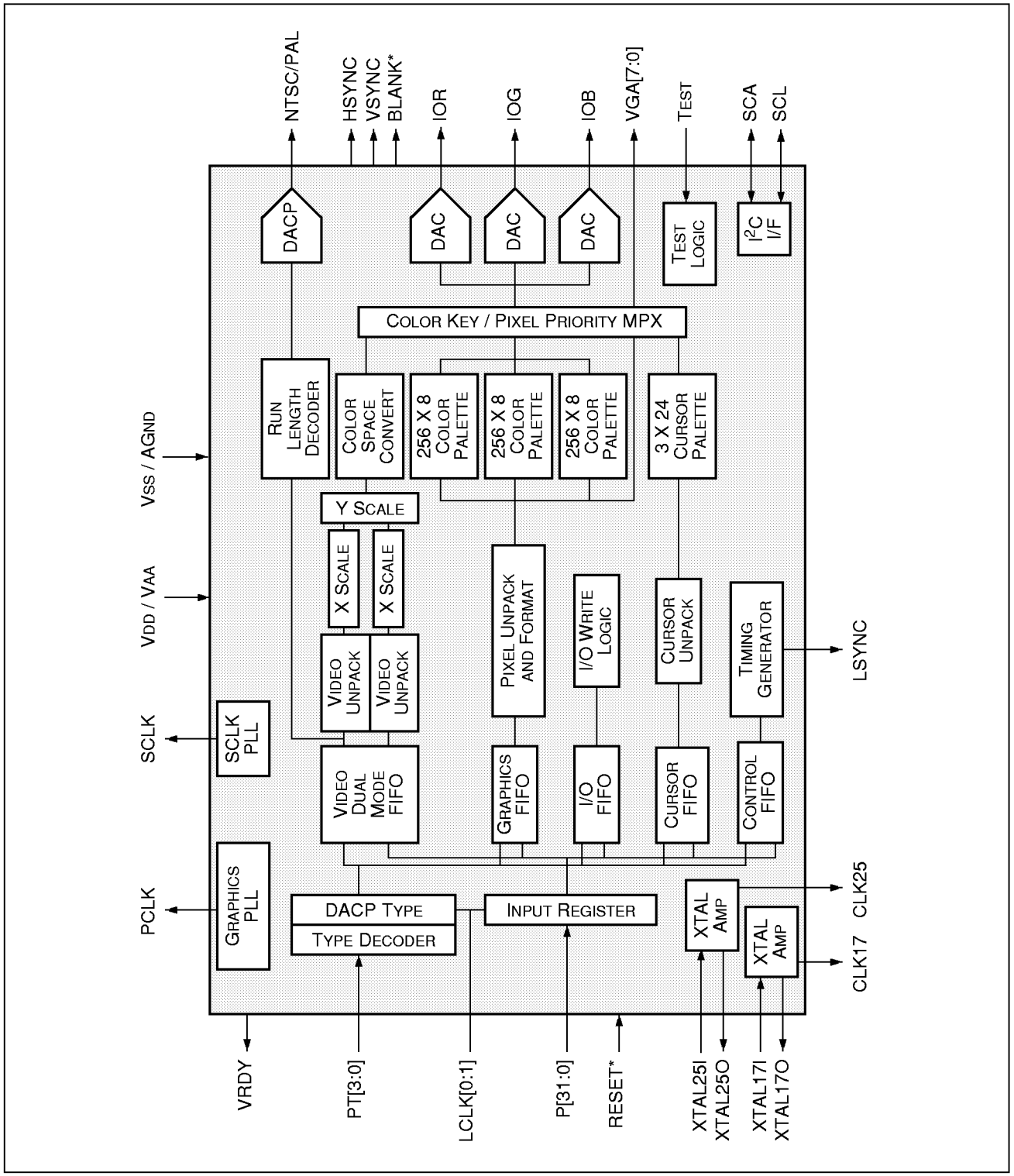
Figure 1 shows the interconnections between the BtV2487, the MediaBuffer, and the BtV2115 MediaStream controller. The serial clock is provided by the programmable integrated PLL (Phase Lock Loop) in the BtV2487. Typically the programmed frequency is optimized for the MediaBuffer memory speed. The LSYNC signal tells the MediaStream Controller when to start loading data for the subsequent scan line. The positioning of the LSYNC signal is determined by the horizontal timing state machine; it must be carefully programmed to prevent FIFO over- or under-run.

Figure 1. System Block Diagram



A more detailed block diagram of the BtV2487 is shown in Figure 2.

Figure 2. BtV2487 Detailed Block Diagram



Packet Types

Data sent to the BtV2487 on the pixel port is interpreted by the packet type value on the PT[3:0]. P[31:16] and PT[3:0] are latched on LCLK[0], and P[15:0] are latched on LCLK[1]. The packet type applies to all data pins p[31:0]. The packet types are listed in Table 1.

Table 1. Packet Types

PT(3–0)	Packet Type	Description
$0	Reserved	Ignored by the BtV2487.
$1	CURSOR	Bits 31–0 of the pixel port supply the pixel input to the cursor FIFO. The cursor FIFO unload is controlled by a counter in the BtV2487 which is initialized by the cursor origin position bit in the horizontal timing generator.
$2	GRAPHICS	Bits 31–0 of the pixel port supply the pixel input to the graphics FIFO. The graphics FIFO will continue to be unloaded, as needed, as long as the graphics unload signal is asserted from the horizontal timing generator.
$3	VIDEO 1	Bits 31–0 of the pixel port supply the pixel input to the video 1 FIFO, when the FIFOs are configured as two separate FIFOs, or to the concatenated FIFO, when the FIFOs are configured for use as a single FIFO. The video 1 FIFO will continue to be unloaded, as needed, as long as the video 1 unload signal is asserted from the horizontal timing generator; or the Softvideo Output function is enabled.
$4	VIDEO 2	Bits 31–0 of the pixel port supply the pixel input to the video 2 FIFO. If the video FIFOS are configured for use as a single FIFO, this packet will be ignored. The video 2 FIFO is unloaded, as needed, as long as the video 2 unload signal is asserted from the horizontal timing generator.
$5	I/O WRITES	Bits 31, 24–0 of the pixel port supply the I/O write data to the I/O FIFO. these packets contain address and data values to be written into the I/O registers of the BtV2487, things like cursor horizontal position, control registers, and color palette data. Bit configurations for this packet type are shown in Table 2.
$6	TIMING GENERATOR STATE	The BtV2487 contains a state machine that times all horizontal information on the line. The bits are defined in Table 20.
$7–$D	Reserved	Ignored by the BtV2487.
$E	NOOP	Ignored by the BtV2487
$F	RESET	This cycle causes a reset of all the BtV2487 functions. This reset is equivalent, with minor exceptions, to asserting the RESET* signal. At least fifteen consecutive RESET packets must be sent to reliably reset the BtV2487. See “RESET Actions” on page 46.

Programming and Internal Register Mapping

The internal I/O registers are accessed by writing packets to the I/O write FIFO. Internal locations are accessed by using the 10-bit I/O Address Register as an internal pointer for individual register selection. A small FIFO is provided for I/O write packet data. The I/O write FIFO is unloaded at the CLK25 rate during the time that BLANK* is asserted (i.e.: low) in the horizontal timing generator. The I/O Write FIFO should be loaded at times such that unloaded items will not extend through the end of the blanking interval. There is a minimum latency through the I/O Write FIFO of 4 CLK25 cycles. Table 2 shows the two I/O packet formats for writing the I/O Address Register and for writing an internal register. The contents of the I/O Address Register are not initialized.

Table 2. I/O Write Packet

P[31]	P[23:0]	Description
0	P[23:0]	Load the Internal Data Register. When this I/O packet is unloaded from the I/O write FIFO, it causes the internal register whose address is contained in the I/O Address Register to be written with the data contained in P[23:0]. The I/O Address Register is incremented after the data is stored.
1	ADDR[9:0]	Load the I/O Address Register. When this I/O packet is unloaded from the I/O write FIFO, the I/O Address Register is loaded with the data contained in P[9:0].

The internal I/O Address Register mapping are shown in Table 3.

Table 3. Internal Register Mapping *(1 of 2)*

I/O Address Register [9:0]	P[23:16]	P[15:8]	P[7:0]	Reset Value	Description
$000			P[7:0]	$00	Border Color Index Register.
$001		P[15:0]		VGA Text Mode	Pixel Clock PLL Control Register. See Table 5.
$002	—	P[15:0]		25 MHz	Serial Clock PLL Control Register. SeeTable 7.
$003	P[23:0]			$000000	Configuration Register. For the list of bit definitions, see Table 4.
$004	—	P[15:0]		$0000	Graphics Format Register. For the list of bit definitions, see Table 9.
$005	—	X[11:0]		$000	Cursor X Position Register.
$006	Write zeros only.			$00	Reserved
$007	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Graphics Diagnostic Register. See "Diagnostic Circuitry" on page 38.
$008	—		P[7:0]	N/A	Softvideo Diagnostic Register.

Table 3. Internal Register Mapping *(2 of 2)*

I/O Address Register [9:0]	P[23:16]	P[15:8]	P[7:0]	Reset Value	Description
$009 : $00D	Write zeros only.			N/A	Reserved
$00E	—	P[15:0]		$0000	FIFO Error Status Register. See Table 26.
$00F	Write zeros only			N/A	Reserved
$010	—	P[15:0]		$0000	Video Format Register. Refer to Table 13.
$011	P[23:0]			$000000	Video Window 1 Color Key Register.
$012	P[23:0]			$000000	Video Window 1 Color Key Mask Register.
$013	—	XS1INC[11:0]		$000	Video Window 1 X Scale Increment Register.
$014	P[23:0]			$000000	Video Window 2 Color Key Register.
$015	P[23:0]			$000000	Video Window 2 Color Key Mask Register.
$016	—	XS2INC[11:0]		$000	Video Window 2 X Scale Increment Register.
$017	—	YS1INC[11:0]		$000	Video Y Scale Increment Register.
$018 : $0FF	Write zeros only.			N/A	Reserved.
$100 : $1FF	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Color Palette Location 00 : Color Palette Location FF
$200	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Border Color Register.
$201	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Cursor Color 1 Register.
$202	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Cursor Color 2 Register.
$203	Red[7:0]	Green[7:0]	Blue[7:0]	N/A	Cursor Color 3 Register.
$204 : $3FF	Write zeros only.			N/A	Reserved

Configuration Register The bit mappings for Configuration Register are shown in Table 4.

Table 4. Configuration Register Bit Definitions *(1 of 2)*

Bit(s)	Field	Reset Value	Description
23–19	Reserved	N/A	Reserved. This field should be written with zero.
18	Video Plane 2 FIFO Standby (0) Standby Condition (1) Normal Operation	0	Writing a logical zero to either of these bits causes the corresponding video FIFO to enter a "standby" condition of reduced power consumption. In the standby condition, video FIFO unloads are inoperative. Writing a logical one powers up the corresponding video FIFO to allow normal unloading operation.
17	Video Plane 1 FIFO Standby (0) Standby Condition (1) Normal Operation	0	
16	Softvideo DAC powerdown (0) DAC turned off (1) Normal Operation	0	
15	Force Blank (0) Normal Operation (1) Force pixel data to blank level	0	Writing a logical one to this bit causes the pixel input data to the DACs to be at blank level; pixel data at the Graphics Diagnostic Register will also be zero. Sync and pedestal current levels are unaffected by this bit. On the VGA output port, the BLANK* output is driven active, and the VGA data is driven with the border color index value, if enabled.
14	Softvideo Output Sample Rate Select (0) CLK17 (1) CLK25/2	0	Writing a logical zero causes the softvideo output logic to process samples at the CLK17 rate. Writing a logical one causes the softvideo output logic to process samples at half of the CLK25 rate.
13	VRDY Output Enable (0) Three-state VRDY Output (1) Drive VRDY Output	0	When this bit is a logical one, the VRDY output is driven to indicate if the video plane 1 FIFO is at least half empty.
12	Reserved	N/A	Read only.
11	Video Path Clock Select (0) Pixel Clock Select (1) Softvideo Clock Select	0	This bit controls the video path clocking. It should only be switched while the video FIFOs are not being unloaded.
10	Diagnostic Mode (0) Signature Mode (1) Data Strobe Mode	0	When this bit is a logical zero, the diagnostic logic blocks for graphics and softvideo are configured to compute signatures. When this bit is a logical one, the diagnostic registers will capture each 24-bit or 8-bit word presented to the graphics or softvideo DACs, respectively. See "Diagnostic Circuitry" on page 38.
9	Border Mode Control (0) Use Border Color Index Register (1) Use Border Color Register	0	Writing a logical zero causes the Border Color Index Register to be used to access a location in the color palette whenever the border is to be displayed. Writing a logical one causes the 24-bit Border Color Register to be used as the displayed border color.

Table 4. Configuration Register Bit Definitions *(2 of 2)*

Bit(s)	Field	Reset Value	Description
8	VGA Output Port Disable (0) Driven with pixel data (1) Driven logical zero	0	Writing a logical zero causes the VGA output port to be enabled. Writing a logical one causes PCLK, VGA[7:0], and BLANK* to be a logical zero. This bit has no effect on the HSYNC and VSYNC outputs.
7,6	Cursor Mode Select (00) Cursor Disabled (01) Three-Color Cursor (10) Two-Color/Highlight Cursor (11) Two-Color/X-Windows Cursor	00	This field selects the cursor mode. See Table 19 for the actual colors which would be displayed.
5	Pedestal (0) 0 IRE Pedestal (1) 7.5 IRE Pedestal	0	
4	Sync Enable (0) No Sync on Green (1) Sync on Green	0	The composite sync used for sync on green comes from the SYNC state bit of the horizontal timing state machine. Composite sync is independent of the HSYNC and VSYNC bits of the horizontal timing state machine.
3	DAC Powerdown (0) Normal Operation (1) DACs turned off	0	
2	Palette RAM Powerdown (0) Normal Operation (1) RAMs Turned off	0	
1	Concatenate Video FIFOs (0) Independent FIFOs for Video 1 & 2 (1) Single long FIFO for Video window 1 or Softvideo output	0	This bit should be changed only while both video FIFOs are empty, otherwise the video FIFOs' operation will be unpredictable.
0	Softvideo output enable (0) Disabled (1) Enabled	0	When this bit is a logical zero, the softvideo logic is disabled. Prior to enabling the softvideo logic, the video path clock must be set to the softvideo clock.

Pixel Clock PLL

Using the XTAL17 or XTAL25 crystal reference input as a source, the BtV2487 can generate pixel clocks in the range of less than 10 and up to 136 MHz with typical granularity of less than 500 kHz. The frequency is selected by programming appropriate values into the Pixel Clock PLL Control Register. The pixel frequency is determined by the following relationship:

$$PixelRate = \left(\frac{M}{N \bullet L}\right) \times CrystalFrequency$$

The desired M, N, and L values are written into the Pixel Clock PLL Control Register as shown in Table 5.

Table 5. Pixel Clock PLL Control Register Bit Mappings

Bit(s)	Field Name	Reset Value	Description
15	Source Reference (0) XTAL25 (1) XTAL17	0	Source crystal reference selection.
14	N Diagnostic Read	—	MSB of N Counter. Read only.
13	M Diagnostic Read	—	MSB of M Counter. Read only.
12	Test Bit	0	Set to logical 1
11,10	L (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	10	Post-Scaler
9–6	N ($0) Reserved : ($3) Reserved ($4) 4 : ($F) 15	$D	
5–0	M ($00) Reserved : ($14) Reserved ($15) 21 : ($3F) 63	$3C	

PLL parameters for common graphics display formats are shown in Table 6.

Table 6. Pixel PLL Parameters for Common Graphics Display Formats

Nominal Pixel Rate (MHz)	Crystal Select[1]	M	N	L	Actual Pixel Rate (MHz)	Difference (%)	Graphics Display Format
28.3212	XTAL25	60	13	4	28.3569	+0.12	720 x 400 Standard Text VGA, 70 Hz
25.175	XTAL25	41	10	4	25.1904	+0.06	640 x 480 Standard Graphics VGA, 60 Hz[2]
31.500	XTAL25	41	8	4	31.4880	–0.04	VESA 640 x 480, 72 Hz
36.000	XTAL25	41	14	2	35.9863	–0.04	VESA 800 x 600, 56 Hz
50.000	XTAL25	61	15	2	49.9712	–0.06	VESA 800 x 600, 72 Hz
65.000	XTAL25	37	7	2	64.9509	–0.08	VESA 1024 x 768, 60 Hz
75.000	XTAL17	31	7	1	74.9934	–0.01	VESA 1024 x 768, 70 Hz
80.000	XTAL17	52	11	1	80.0516	+0.06	1024 x 768, 76 Hz
106.925	XTAL25	61	14	1	107.081	+0.15	NEC 5/6FG Preset Timing Chart 1280 x 1024, 60 Hz
126.997	XTAL17	30	4	1	127.005	+0.01	NEC 5/6FG Preset Timing Chart 1280 x 1024, 70 Hz
135.007	XTAL25	33	6	1	135.168	+0.12	NEC 5/6FG Preset Timing Chart 1280 x 1024, 74 Hz

1. XTAL25 is 24.576 MHz; XTAL17 is 16.9344 MHz
2. This format requires at least 0.1% pixel rate accuracy

Serial Clock PLL

Using the same crystal as the pixel clock PLL, the BtV2487 can generate serial clock rates of 25 to 75 MHz with typical granularity of 2 MHz. The frequency is selected by programming appropriate values into the Serial Clock PLL Control Register. See Table 3. The pixel frequency is determined by the following relationship:

$$SerialRate = \left(\frac{M}{N \bullet L}\right) \times CrystalFrequency$$

These values are written into the Serial Clock PLL Control Register as shown in Table 7.

Table 7. Serial Clock PLL Control Register Bit Mappings

Bit(s)	Field Name	Reset Value	Description
15	Source Reference (0) XTAL25 (1) XTAL17	0	Source crystal reference selection.
14	N Diagnostic Read	—	MSB of N Counter. Read only.
13	M Diagnostic Read	—	MSB of M Counter. Read only.
12	Test Bit	0	Set to logical 1
11,10	L (00) Divide by 1 (01) Divide by 2 (10) Divide by 4 (11) Divide by 8	10	Post-Scaler
9–6	N ($0) Reserved : ($3) Reserved ($4) 4 : ($F) 15	$F	
5–0	M ($00) Reserved : ($14) Reserved ($15) 21 : ($3F) 63	$3D	

Serial Clock PLL parameters for common load rate frequencies are shown in Table 8.

Table 8. Common Serial Rate Programming Parameters

Nominal Serial Rate (MHz)	Crystal Select	M	N	L	Actual Serial Rate (MHz)	Serial Port Bandwidth (MB/s)
25	XTAL25	61	15	4	24.9856	100
33	XTAL25	59	11	4	32.9542	132
40	XTAL25	26	8	2	39.9360	160
50	XTAL25	61	15	2	49.9712	200
66	XTAL25	59	11	2	65.9084	264

Note In small system designs, there should be enough margin to allow for jitter-induced cycle shortening (0.5 nS or less).

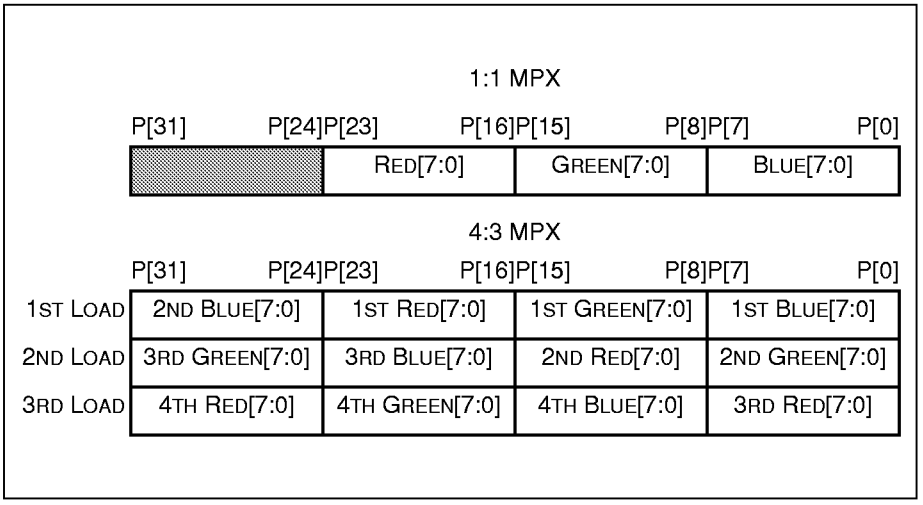
Graphics Modes Supported

The desired graphics pixel mode is selected by loading the Graphics Format Register. All graphics modes use the input pixel data as indices into the color palette RAM; no color palette bypass is provided.

24-Bit/Pixel True Color

24-Bit/Pixel formats are shown in Figure 3. In this mode, the Red, Green, and Blue channels are used to independently address the Red, Green, and Blue color palettes, respectively, to yield a 24-bit color.

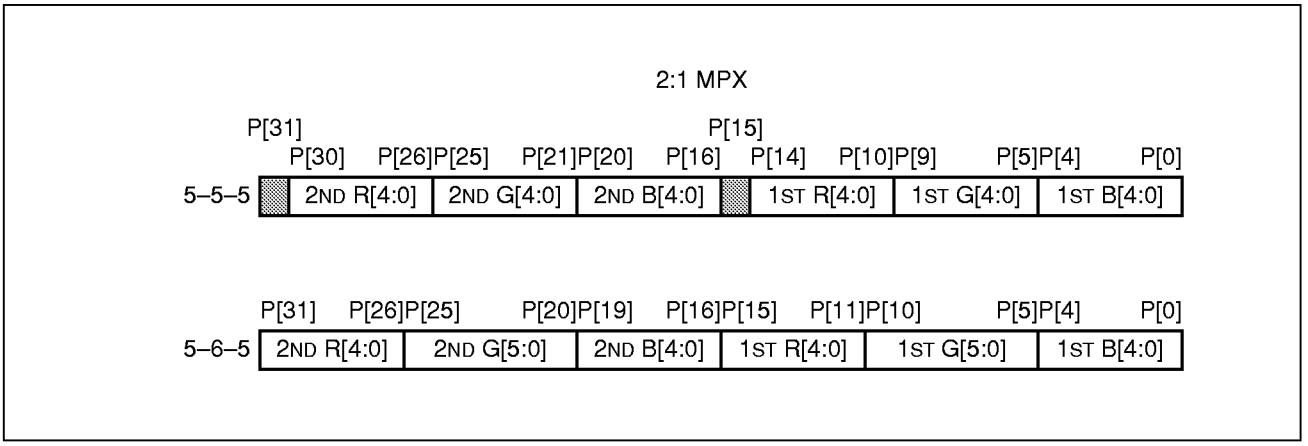
Figure 3. 24 Bits/Pixel Graphics Formats



16-Bit/Pixel True Color

16-Bit/Pixel formats are shown in Figure 4. Each color channel independently addresses the Red, Green, and Blue color palettes. The Red, Green, and Blue available channel widths of 5 and 6 use contiguous palette addressing; i.e. only the first 32 or 64 entries in the color palettes are used for channel widths of 5 or 6, respectively. The unused bit (i.e., P(15)) in 5-5-5 mode may be used as a colorkey by specifying P(15) in the color key mask, and turning on the Colorkey Enable Bit in the Video Format Register.

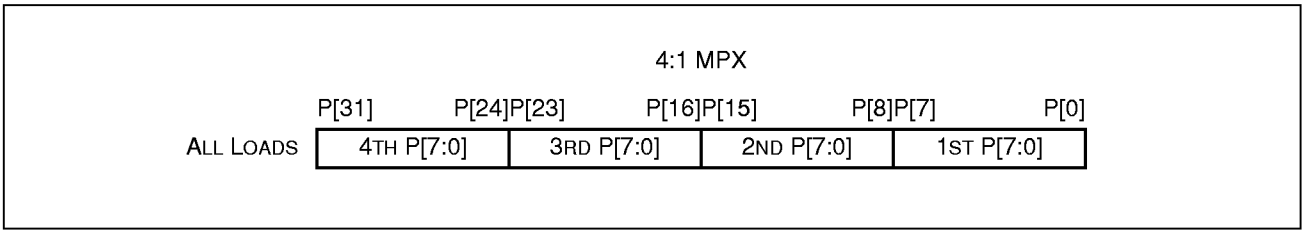
Figure 4. 16 Bits/Pixel Graphics Formats



8-Bit/Pixel Pseudo Color

The 8-Bit/Pixel format is shown in Figure 5. In this mode, the 8-bit pixel is used as an index into each of the Red, Green, and Blue color palettes to select a 24-bit color.

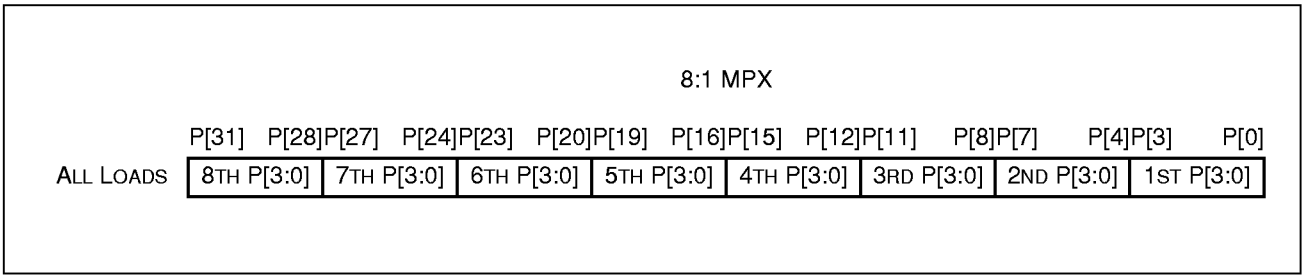
Figure 5. 8-Bit/Pixel Graphics Format



4-Bit/Pixel Pseudo Color

The 4-Bit/Pixel format is shown in Figure 6. In this mode, the 4-bit pixel is right-justified with zero fill, and used as in index into each of the Red, Green, and Blue color palettes to select a 24-bit color. Only the first 16 color palette locations are used.

Figure 6. 4-Bit/Pixel Graphics Format



Graphics Format Control Register

The Graphics Format Register bits are defined in Table 9.

Table 9. Graphics Format Register Bit Definitions

Bit(s)	Field	Reset Value	Description
15–3	Reserved		Reserved, write zeros only.
2	Graphics RGB Format In 16 Bit/Pixel mode: (0) 5-6-5 (1) 5-5-5 In 24 Bit/Pixel mode: (0) Planar RGB, 1:1 MPX (1) Packed RGB, 4:3 MPX	0	This bit is ignored when configured for other pixel depths other than 16 or 24.
1,0	Graphics Pixel Depth (00) 8 Bits/Pixel, 4:1 MPX (01) 4 Bits/Pixel, 8:1 MPX (10) 16 Bits/Pixel, 2:1 MPX (11) 24 Bits/Pixel, 1:1 or 4:3 MPX	00	

Graphics FIFO Underrun Condition

If the graphics FIFO is underrun (i.e. the horizontal timing state machine requests graphics pixel data, but the graphics FIFO is empty) the graphics contribution to the displayed pixel is undefined.

Video Modes Supported

The BtV2487 supports the display of source video in either of the 16-bit true color graphics formats, the 24-bit true color graphics format, the 4:1:1 video format or 4:2:2 video formats.

4:1:1 Video Format

The 4:1:1 format supported by the BtV2487 is shown in Table 10.

Table 10. 4:1:1 Video Input Format

Load Group Sequence	Pixel Port Pin			
	P[31:24]	P[23:16]	P[15:8]	P[7:0]
0	Y1[7:0]	C_r0[7:0]	Y0[7:0]	C_b0[7:0]
1	Y3[7:0]	C_r4[7:0]	Y2[7:0]	C_b4[7:0]
2	Y7[7:0]	Y6[7:0]	Y5[7:0]	Y4[7:0]
3	Y9[7:0]	C_r8[7:0]	Y8[7:0]	C_b8[7:0]
etc.				

Load Group 0 represents the first load group of the video plane, Load Group 1 is the subsequent load for that video plane, etc. The pattern repeats every three load groups. C_r and C_b values are then interpolated to produce the video stream shown in Table 11.

Table 11. Interpolated Video Data Stream

Video Pixel Sequence	Y	4:1:1 Video		4:2:2 Video	
		C_r	C_b	C_r	C_b
0	Y0	C_r0	C_b0	C_r0	C_b0
1	Y1	0.75 C_r0 + 0.25 C_r4	0.75 C_b0 + 0.25 C_b4	0.5 C_r0 + 0.5 C_r2	0.5 C_b0 + 0.5 C_b2
2	Y2	0.5 C_r0 + 0.5 C_r4	0.5 C_b0 + 0.5 C_b4	C_r2	C_b2
3	Y3	0.25 C_r0 + 0.75 C_r4	0.25 C_b0 + 0.75 C_b4	0.5 C_r2 + 0.5 C_r4	0.5 C_b2 + 0.5 C_b4
4	Y4	C_r4	C_b4	C_r4	C_b4
5	Y5	0.75 C_r4 + 0.25 C_r8	0.75 C_b4 + 0.25 C_b8	0.5 C_r4 + 0.5 C_r6	0.5 C_b4 + 0.5 C_b6
6	Y6	0.5 C_r4 + 0.5 C_r8	0.5 C_b4 + 0.5 C_b8	C_r6	C_b6
7	Y7	0.25 C_r4 + 0.75 C_r8	0.25 C_b4 + 0.75 C_b8	0.5 C_r6 + 0.5 C_r8	0.5 C_b6 + 0.5 C_b8
8	Y8	C_r8	C_b8	C_r8	C_b8
etc.					

For pixel port bandwidth calculations, 4:1:1 video requires 12 bits per prescaled video pixel. The least significant bit of luminance may be used for chroma keying in this mode.

4:2:2 Video Format

For 4:2:2 video, the bandwidth requirements are computed using 16 bits per prescaled video pixel. The format for this mode is shown in Table 12. The least significant bit of luminance may be used for chroma keying in this mode.

Table 12. 4:2:2 Video Input Format

Load Group Sequence	Pixel Port Pin			
	P[31:24]	P[23:16]	P[15:8]	P[7:0]
0	Y1[7:0]	C_r0[7:0]	Y0[7:0]	C_b0[7:0]
1	Y3[7:0]	C_r2[7:0]	Y2[7:0]	C_b2[7:0]
2	Y5[7:0]	C_r4[7:0]	Y4[7:0]	C_b4[7:0]
3	Y7[7:0]	C_r6[7:0]	Y6[7:0]	C_b6[7:0]
etc.				

Dual Mode FIFO

The configuration of the dual-mode video FIFO is selected by writing the FIFO Configuration Bits in the Configuration Register. See Table 4. The enabling of the display of each video plane is controlled by the horizontal timing state machine, and the control of the video plane priority and color/chroma key enabling are specified in the Video Format Register (See Table 13). The video format for each video plane is selected by programming the corresponding Video Format Register. These bits are mapped as shown in Table 13.

Table 13. Video Format Register Bit Definitions *(1 of 2)*

Bit(s)	Field	Reset Value	Description
15	Video Plane Priority (0) Video Plane 1 is higher priority (1) Video Plane 2 is higher priority	0	The priority bit must match the enabled planes, i.e. if plane 2 is disabled and plane 1 is enabled, this bit must be set to a logical 0.
14	Video Plane 2 Replicate Enable (0) Interpolate on upscaling (1) Replicate on upscaling	0	When this bit is a logical one, intermediate horizontally upscaled pixels will be generated by replicating from left to right.
13	Video Plane 2 Horizontal Upscale Enable (0) Disable horizontal upscaling (1) Enable horizontal upscaling	0	
12–10	Video Plane 2 Format (000) 4:1:1 YC_rC_b (001) 4:2:2 YC_rC_b (010) 16-Bit RGB (5-6-5) (011) 16-Bit RGB (5-5-5) (100) 24-Bit RGB (8-8-8) (101) Reserved : (111) Reserved	000	Video format control bits. 4:1:1 video requires 12-bits/pixel, 4:2:2 video requires 16-bits/pixel. RGB formats are MSB bit-replicated to achieve full-scale. See Table 16.
9	Video Plane 2 Graphics Color Key Enable (0) Color keying disabled (1) Color keying enabled	0	When this bit is a logical one, the graphics pixel is used to select between the display of graphics or video by comparing the graphics pixel to the video plane 2 color key (subject to the mask). When the criterion is met (i.e. equal), the video pixel is displayed, otherwise the graphics pixel is displayed.
8	Video Plane 2 Video Chroma Key Enable (0) Chroma keying disabled (1) Chroma keying enabled	0	When this bit is a logical one, the chroma bit of a video pixel to be displayed (after being subjected to priority and color keying) is used to select pixel display between the video and graphics stream. This bit should be a logical zero for non-chroma capable video formats.
7	Vertical Upscale Enable (0) Disable vertical upscaling (1) Enable vertical upscaling	0	When this bit is a logical one, the two video FIFO streams are interpolated to produce a single output video stream. The video FIFOs must be configured as two separate FIFOs for vertical upscaling.
6	Video Plane 1 Replicate Enable (0) Interpolate on upscaling (1) Replicate on upscaling	0	When this bit is a logical one, intermediate upscaled pixels will be generated by replicating from left to right (horizontal upscaling) and top to bottom (vertical upscaling).

Table 13. Video Format Register Bit Definitions *(2 of 2)*

Bit(s)	Field	Reset Value	Description
5	Video Plane 1 Horizontal Upscale Enable (0) Disable horizontal upscaling (1) Enable horizontal upscaling	0	
4–2	Video Plane 1 Format (000) 4:1:1 YC_rC_b (001) 4:2:2 YC_rC_b (010) 16-Bit RGB (5-6-5) (011) 16-Bit RGB (5-5-5) (100) 24-Bit RGB (8-8-8) (101) Reserved : (111) Reserved	000	Video format control bits. 4:1:1 video requires 12-bits/pixel, 4:2:2 video requires 16-bits/pixel. RGB formats are MSB bit-replicated to achieve full-scale. See Table 16.
1	Video Plane 1 Graphics Color Key Enable (0) Color keying disabled (1) Color keying enabled	0	When this bit is a logical one, the graphics pixel is used to select between the display of graphics or video by comparing the graphics pixel to the video plane 1 color key (subject to the mask). When the criterion is met (i.e. equal), the video pixel is displayed, otherwise the graphics pixel is displayed.
0	Video Plane 1 Video Chroma Key Enable (0) Chroma keying disabled (1) Chroma keying enabled	0	When this bit is a logical one, the chroma bit of a video pixel to be displayed (after being subjected to priority and color keying) is used to select pixel display between the video and graphics stream. This bit should be a logical zero for non-chroma capable video formats.

Color Key Using Graphics Source

Video color keying from the graphics stream is supported through the use of the 24-bit Color Key and Mask Registers. When a video plane is selected for display using the color key criteria (see Table 13), the serialized pixel graphics data is compared with the color keys. If the graphics pixel bits match a video plane's color key bits in the same positions that window's color key mask contains logical ones, then the video pixel will be displayed. The color key mask should contain a zero in those bit positions beyond the pixel size. The color key compare determination is made separately for each of the two video planes. A color key mask containing zero in all bits will match any graphics data.

Chroma Key Using Video Source

Chroma keying using the video source is supported for the 24-Bit True Color, the 5-5-5 16-Bit True Color, and the YC_rC_b video formats. When the chroma key in the video stream is a logical one, then video is displayed; when the chroma key in the video stream is a logical zero, then the video stream is transparent.

YC_rC_b/RGB Color Space Conversions

For the 4:1:1 and 4:2:2 video formats, the BtV2487 converts the interpolated YC_rC_b video data stream to 24 bits of RGB data (8 bits each) compliant with CCIR Recommendation 601-1 as follows:

$$R = 1.164\,(Y - 16) + 1.596\,(C_r - 128)$$

$$G = 1.164\,(Y - 16) - 0.813\,(C_r - 128) - 0.391\,(C_b - 128)$$

$$B = 1.164\,(Y - 16) + 2.018\,(C_b - 128)$$

Load Group Count

Since there is no automatic clearing of the FIFOs at the end of each line, it is imperative that the number of load groups for each FIFO be the exact number required for the given mode of operation and the desired video window size. Table 14 indicates the required number of load groups for each possible video mode of operation.

Table 14. Video Mode Load Count Requirements

Window Width (pixels)	YC_rC_b 4:1:1	YC_rC_b 4:2:2	RGB 5-5-5 or 5-6-5	RGB 8-8-8
1	1	1	1	1
2	2	2	1	2
3	2	2	2	3
4	2	3	2	4
5	3	3	3	5
6	4	4	3	6
7	4	4	4	7
8	4	5	4	8
9	4	5	5	9
10	5	6	5	10
:	:	:	:	:
n	1 + 3[(**n** – 1) div 8] + [(**n** – 1) div 2] % 4 + [(**n** % 4)==2]†	**n** div 2 + 1	int[(n+1)/2]	n
160 (NTSC QCIF)	61	81	80	160
192 (PAL QCIF)	73	97	96	192
320 (NTSC CIF)	121	161	160	320
384 (PAL CIF)	145	193	192	384
640 (NTSC CCIR 601)	241	321	320	640
768 (PAL CCIR 601)	289	385	384	768

† This term evaluates to a one when true, or zero, when false

Horizontal Upscaling (YC_rC_b Formats)

Horizontal upscaling is accomplished by using the output of overflowing 12-bit accumulators (one per video plane) to either move on to the next pair of video pixels or interpolate another video pixel using the current video pixel pair. At the start of each assertive transition of the corresponding video pixel unload bit in the horizontal timing state machine, the corresponding accumulator is initialized to $000. This transition also initializes the interpolation logic to interpret the current FIFO word as the first word.

For each video pixel leaving the interpolator, the value stored in the X Scale Increment (XSnINC) Register is added to the respective accumulator. If the addition results in a carry, a pixel is unloaded from the respective video stream FIFO. If no carry occurs, the previous video pixel's luminance value is interpolated with the next video pixel's luminance value. In non-replicate mode, the interpolation can yield up to three unique intermediate values between the pixels being interpolated. The chrominance values are repeated. This method of upscaling is known as a Digital Differential Algorithm (DDA). When chroma keying is enabled, if both chroma keys of the pixels being interpolated are asserted, then the interpolated pixel is opaque, otherwise it is transparent. The generation of chroma key for interpolated pixels is independent of the replicate mode bit.

Upscale Increment Computation

The system needs to pre-calculate and provide the DDA constants required for the desired scale factors and load the values into the appropriate X and Y increment registers. The increment value may be computed by using the following expression:

$$Increment = \frac{4095\,(SourcePixelCount - 1)}{DestinationPixelCount}$$

The source pixel count is the source window height or width, as given by Table 14. The destination pixel count is the size of the onscreen video window height or width. The destination pixel count equals the number of pixels for which unload video will be asserted within the timing word.

Horizontal Upscaling (RGB Formats)

In graphics formats, all channels (i.e., red, green, and blue) are interpolated when upscaled. When chroma keying is enabled, if both chroma keys of the pixels being interpolated are asserted, then the interpolated pixel is opaque, otherwise it is transparent.

Vertical Upscaling

To accomplish vertical scaling, the video FIFOs must be configured as two separate FIFOs. Video FIFO 1 is interpreted as containing the video stream for the upper line of video, and video FIFO 2 is interpreted as containing the video stream of the lower line of video. Two adjacent source lines of video must be sent for each displayed line of video. The unload bits in the timing generator must be both asserted simultaneously for proper operation. In non-replicate mode, three intermediate steps of interpolation are provided for all of the video formats; all channels are interpolated in both YC_rC_b and RGB formats.

The controller needs to duplicate the 12-bit vertical DDA accumulator logic to determine when to increment the VRAM pointers to the next pair of lines of source video. The number of load groups provided for any of the video modes must be exactly enough to provide any required data used either directly, or partially (i.e. interpolated) by the video logic to generate the video data. When color keying or chroma keying in the vertical upscaling mode, both the Video Plane 1 and Video Plane 2 bits need to be set identically in the Video Format Register.

The Video Format Register must be written to during each vertical interval to clear the DDA.

The scaling of source pixels for a given DDA accumulator value is shown in Table 15.

Table 15. Video Pixel Upscaling Weights

DDA Accumulator Bits (11,10)	Vertical Interpolation all channels	Horizontal Interpolation	
		Y, R, G, B channels	C_r, C_b channels
00	100% V_1	100% P_n	100% P_n
01	75% V_1[a] + 25% V_2[b]	75% P_n[c] + 25% P_{n+1}[d]	100% P_n
10	50% V_1 + 50% V_2	50% P_n + 50% P_{n+1}	100% P_n
11	25% V_1 + 75% V_2	25% P_n + 75% P_{n+1}	100% P_n

a. V_1 is Video Plane 1 FIFO luminance, chrominance, or R,G,B channel data (upper line of video)
b. V_2 is Video Plane 2 FIFO luminance, chrominance, or R,G,B channel data (lower line of video)
c. P_n is the earlier video pixel channel value
d. P_{n+1} is the later video pixel channel value

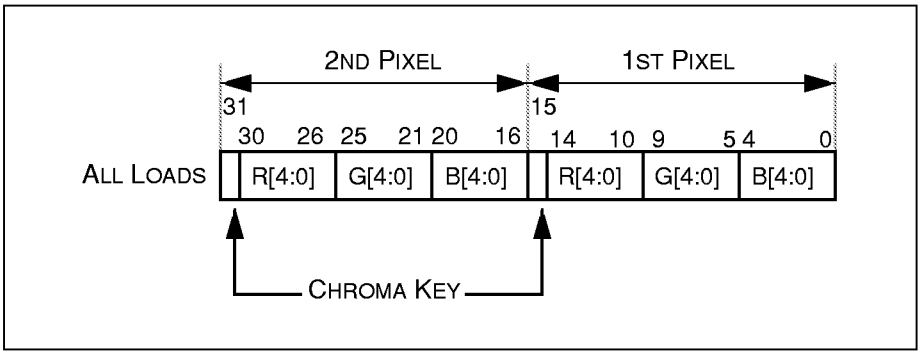
Video FIFO Underrun

If the video FIFO is underrun, (i.e. the horizontal timing state machine request that video data be displayed, but the corresponding video FIFO is empty), the video data will generally be unpredictable.

5-6-5 True Color Video Format

This format is shown in Figure 7. Chroma keying from the video source is accomplished by using pixel bit 15. A logical one in bit 15 causes the video data to be displayed; a logical zero causes the video pixel data to be transparent.

Figure 7. 5-5-5 True Color Video Format



5-5-5 True Color Video Format

This format is identical to the 5-6-5 True Color Graphics format shown in Figure 4. Chroma keying from the video source is not supported in this format.

Color Scaling

The 5-5-5 and 5-6-5 true color formats achieve 8-bit DAC full scale by repeating, from left to right, the supplied bits of each channel into the unspecified lower-order bits. The truth table is shown in Table 16.

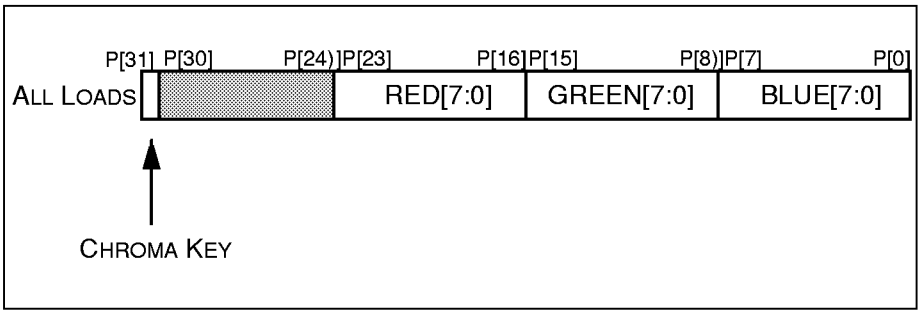
Table 16. Color Scaling Truth Table

Channel Width	Channel Input	DAC Input
5	00000 00001 00010 00011 00100 00101 00110 00111 01000 : 11100 11101 11110 11111	00000 000 00001 000 00010 000 00011 000 00100 001 00101 001 00110 001 00111 001 01000 010 : 11100 111 11101 111 11110 111 11111 111
6	000 000 000 001 : 001 110 001 111 010 000 010 001 : 011 110 011 111 100 000 100 001 : 101 110 101 111 110 000 110 001 : 111 110 111 111	000 000 00 000 001 00 : 001 110 00 001 111 00 010 000 01 010 001 01 : 011 110 01 011 111 01 100 000 10 100 001 10 : 101 110 10 101 111 10 110 000 11 110 001 11 : 111 110 11 111 111 11

24-Bit True Color Video Format

This format is illustrated in Figure 8. This format may be used to support a 24-bit True Color cursor. Bit 31 is used to control chroma keying from the video source. A logical one in bit 31 causes the video data to be displayed; a logical zero causes the graphics pixel data to be displayed.

Figure 8. 24-Bit True Color Video Format

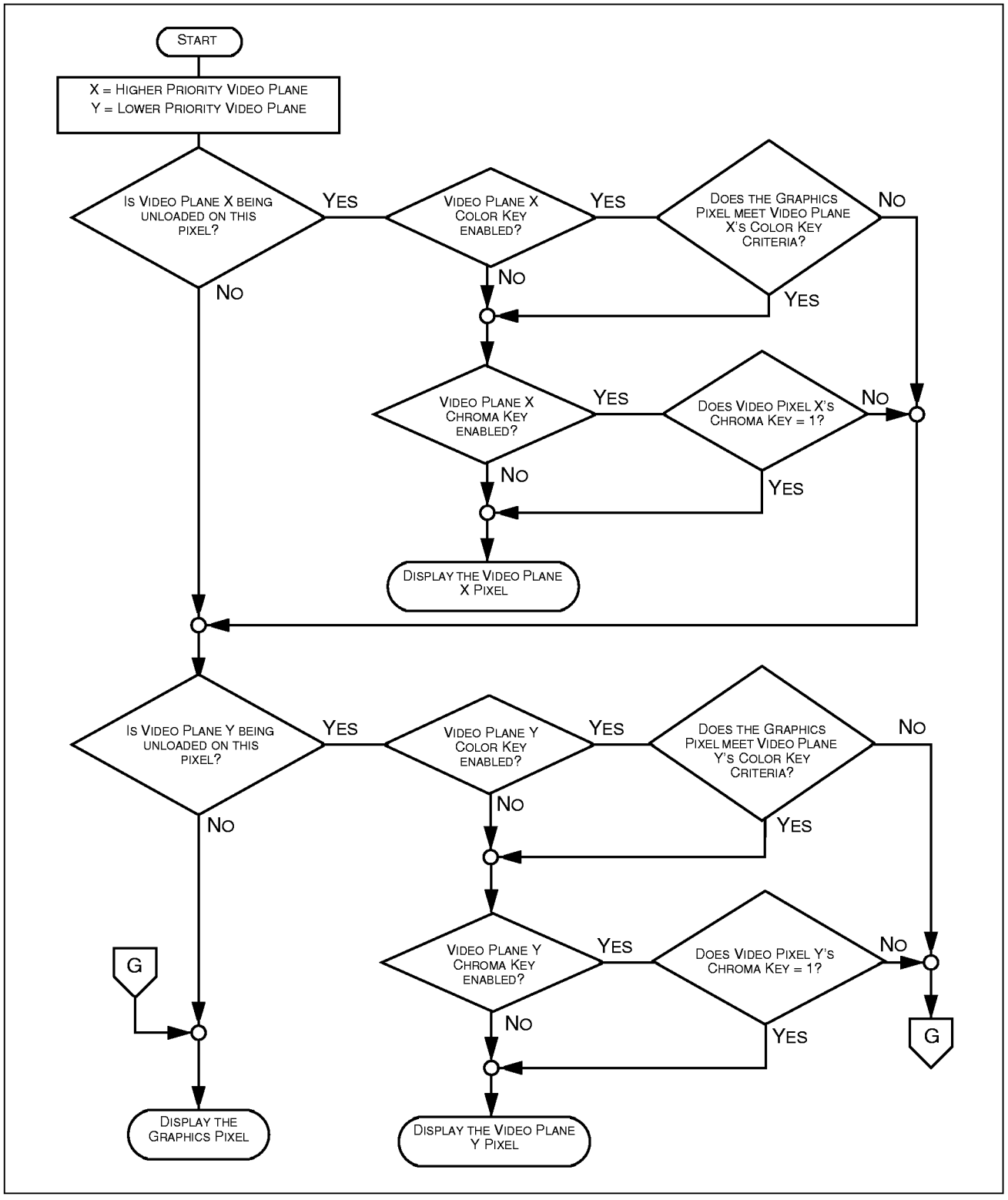


Using a Video Source to provide a True Color Cursor

To use a video plane as a true color cursor, the higher priority video plane is programmed as the cursor source. The video source should be configured in chroma key enabled mode, with color keying disabled. This will allow transparent showing of underlying graphics or video data. The video format selected should be a chroma key capable mode, or the video cursor will not be transparent anywhere within its window. The positioning of the video sourced cursor is controlled by the positioning of the video FIFO unload bit in the horizontal timing state machine.

The overall display selection logic is shown in flowchart form in Figure 9.

Figure 9. Video/Graphics Pixel Source Selection Flowchart



VGA Output Port

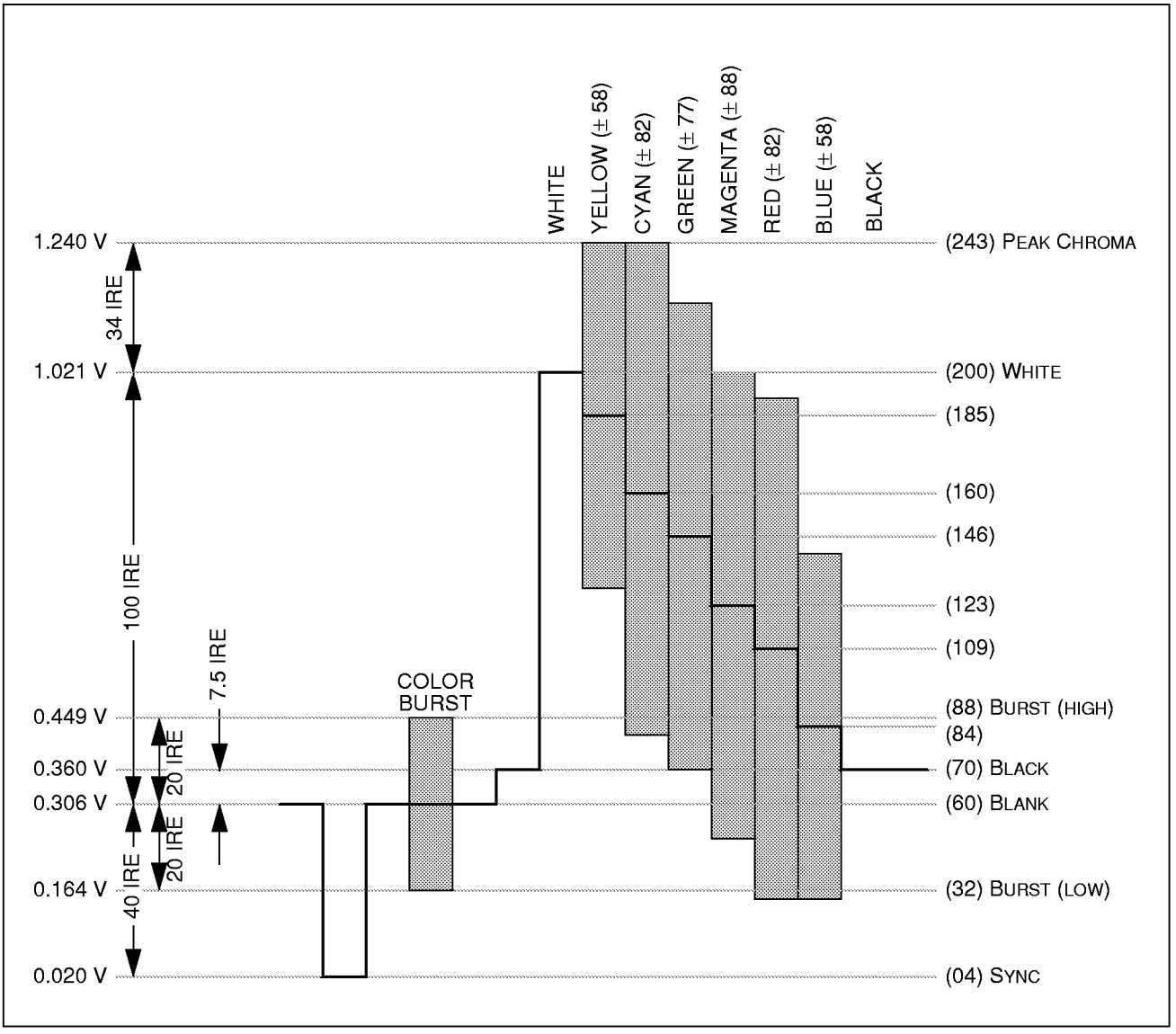
The VGA output port consists of the signals PCLK, VGA[7:0], and BLANK*. When enabled, these signals will be actively driven with the pixel clock, pixel index data, and blank, respectively. The VGA Output Port should not be enabled at pixel rates beyond 30 MHz. The output of this port is undefined for non-pseudo color pixel formats. The output of this port is also undefined during the blanking and border intervals, if true color border is selected. If color indexed border is selected, the border color index register will be output from this port during the blanking and border intervals. No video1 or video2 pixels are available from this port. When video is being displayed on the screen, this port will merely output the pseudo color key graphics data. The VGA output port signals may be up to 6 pixel clocks earlier than the corresponding HSYNC, VSYNC, and analog outputs.

Software Encoded Video (SEV) Output Operation

The BtV2487 may be used to generate NTSC or PAL video signals so that video clips in Video for Windows™, or screen data, can be written to video tape or shown on NTSC monitors. The software driver performs the conversion from successive RGB images to a softvideo PCM (Pulse Code Modulated) stream. By providing a video output DAC and using the video FIFO, along with a modest amount of logic in the run length decoder, the BtV2487 enables a significant reduction in the bandwidth required from system components such as the disk and the local bus.

The standard composite video NTSC colorbar signal for 100% amplitude, 100% saturated EIA color bars is shown in Figure 10. The values in parenthesis are the decimal values to code for the DAC data sample field. The softvideo output DAC is designed to operate into a single-ended 75Ω load.

Figure 10. Composite NTSC Video Output Waveform



First let's state a few assumptions:

- The sample rate is greater than $4*f_{sc}$. A 16.9 MHz clock is available for audio use and it is used by adding the sample rate conversion to the already non-real-time software encoder.
- The color burst will be encoded by the software encoder.
- The video formatting, e.g. sync, front porch, back porch, serrations, etc. is run length encoded, so that a complete hardware timing generator is not required.

Run Length Decoder

Assume that the softvideo FIFO feeds 8 bit bytes in a continuous stream to the softvideo run length decoder at its PCM sample rate. RLE (Run Length Encoded) elements are three bytes long while softvideo samples are eight bits each. In the unblanked portion of a scan line, each byte contains a sample that is fed directly to the video DAC. At the end of the unblanked period (see below) the byte stream is treated as the three-byte RLE codes. For the RLD (Run Length Decoder) logic to operate, it must be enabled via the Configuration Register. See Table 4.

Each RLE element contains a count field (12 bits), eight bits of running DAC code, and a bit that indicates whether the next byte is the first byte of the next RLE code or the next byte of PCM sample. In essence, the last RLE code before unblank decodes to the number of subsequent bytes that will be PCM samples and is followed by that number of PCM samples. At the end of that many samples, the decoder assumes that the next byte will be the first byte of an RLE code. The three byte RLE code is described in Table 17.

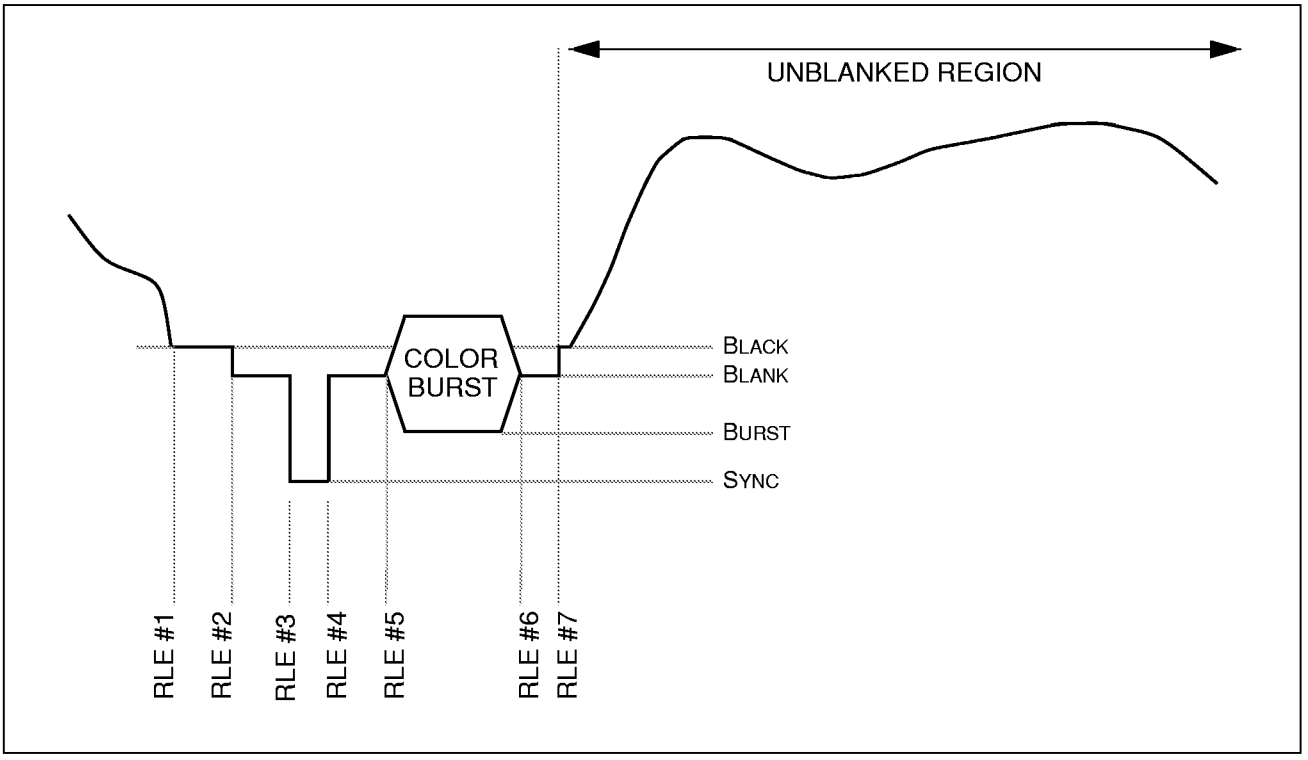
Table 17. Run Length Encoded Control Bit Definition

Bit(s)	Field Name	Description
23–12	Run Count ($000) Reserved ($001) 2 Bytes ($002) 3 Bytes ($003) 4 Bytes : ($FFE) 4095 Bytes ($FFF) 4096 Bytes	When the PCM Escape field is a logical zero, this field contains the number of sample times for which the DAC value in bits [7:0] is sent. When the PCM Escape field is a logical one, this field contains the number of 8-bit PCM samples to be moved from the video stream to the DAC. The count value must be at least 2 bytes. This field is ignored if bit 9 (Freeze) is a logical one.
11	Softvideo Diagnostic Logic Enable (0) Disable (1) Enable	When this bit is a logical zero, the Softvideo Diagnostic Logic is suspended. When this bit is a logical one, the Softvideo Diagnostic Logic will accumulate signatures over the sample presented to the video DAC (if in signature mode) or will latch each video DAC item (if in data strobe mode). This bit should be a logical zero in the freeze word.
10	PCM Escape (0) RLE Word Follows (1) PCM Samples Follow	Escape to PCM samples for the number of bytes specified in the run count field. The current source select bits active for this RLE element will be maintained for the duration of the PCM data which follows. The next RLE code will not be interpreted until after "count" pixel PCM samples have been output to the DAC. This bit is ignored if bit 9 (Freeze) is a logical one.
9	Freeze (0) Continue (1) Freeze	A logical one in this field causes the softvideo logic to end processing. The run count and PCM escape bit are ignored if this bit is a logical one. The run sample byte will be the value that is left stable on the softvideo output until the next point at which the SEV logic is again enabled. The SEV complete status will be asserted when this RLE word is loaded.
8	Reserved	
7–0	Run Sample	If the freeze bit is asserted, this sample is held on the softvideo output until the disabling of the softvideo logic. If the freeze bit in this word is a logical zero, and PCM Escape is a logical one, this sample is output for the current cycle. If PCM Escape is a logical zero, this sample is repeated for the run count duration.

The byte containing bits 7–0 is the first byte seen on the output of the video FIFO.

The Video FIFO receives 32 bit data values from the VRAM serial bus; it multiplexes its output down to a two byte stream. When operating, the video timing sequence for a single scan line looks like that seen in Figure 11.

Figure 11. Softvideo Run Length Decoding Timing Example



SEV Operation

The SEV logic is setup as follows:

1. Make sure the video FIFO is empty.
2. Turn off the video FIFO concatenate bit in the configuration register.
3. Select the desired SEV sample rate, enable the VRDY output, concatenate the video FIFO's to operate as a single larger FIFO, switch the video path clock to the softvideo clock, and power up the softvideo output DAC.
4. Load the video FIFO with SEV data until VRDY is de-asserted.
5. Enable the SEV logic.

At this point the video output will begin supplying the converted samples. Additional SEV data must be provided, as required, by the system. The VRDY output indicates that at least half of the video FIFO is empty, hence, the system is able to send a half-FIFO's worth of SEV data whenever VRDY is asserted.

The final RLE word should have the FREEZE bit asserted to indicate that the final sample produced by this word will be held at the video DAC's output. The last word unloaded from the FIFO by the SEV logic will be the word containing byte 2 of the RLE word that has the FREEZE bit set.

Due to pipelining considerations, an additional 3 packets of unused SEV data must be sent to the video FIFO to prevent a video FIFO underrun.

SEV Enable Control Bit

The SEV Output enable bit in the Configuration Register is used to control the softvideo logic. When this bit is a logical zero, the video DAC maintains its output at zero. The video FIFOs may be loaded with the starting data while this bit is a logical zero; and the VRDY output will reflect the status of the video FIFOs, if VRDY is configured for output. When this bit transitions from a logical one to a logical zero, the video FIFOs are cleared (i.e. emptied). When this bit becomes a logical one, the first word fetched from the FIFO will be interpreted as an RLE code, and the video DAC will begin clocking samples, based on the selected sample rate.

For the wave form shown in this figure, notice that the front porch samples are sent as one RLE element while the color burst is sent as a stream of PCM samples, just as the unblanked region is sent as a stream of PCM samples. The actual byte stream would look something like Table 18.

Table 18. Run Length Decoding Example

Byte Positions	Type	DAC Value	Count	Control Bits
0 : 2	RLE#1	Black level.	Overscan interval	—
3 : 5	RLE#2	Blank level.	Front porch time	—
6 : 8	RLE#3	$04	Sync width	—
9 : 11	RLE#4	Black level.	Back porch before burst	—
12 : 14	RLE#5	first sample of burst.	B_n, the number of PCM samples in burst minus one	PCM Escape
15 : 15 + B_n	PCM	PCM Samples of color burst, relative to 20 IRE	—	—
16 + B_n : 18 + B_n	RLE#6	Blank level.	Overscan interval	—
19 + B_n : 21 + B_n	RLE#7	First sample of scan line	#PCM samples in visible portion of scan line minus one	Enable PCM
22 + B_n : 22 + B_n + S_n	PCM	PCM samples of scan line (S_n bytes)	—	—

VRDY Output Signal

When the concatenated video FIFOs are configured for SEV output mode, the loading of the video FIFO is facilitated by the use of the BtV2487's VRDY output signal, which is asserted whenever the video FIFO is at least half empty (i.e. it is safe to transfer n/2 packets, where n is the total video FIFO size). As the softvideo output function requires the video FIFO to be used in a concatenated mode, the use of this function is mutually exclusive with on-screen video.

Underrun Condition

Due to internal pipelining, an additional 3 SEV packets must be loaded following the final SEV word containing the freeze bit assertion, to prevent video FIFO underrun. The data in these additional 3 packets is ignored. On underrun, the video DAC output will be unpredictable. The video plane 1 underrun bit will be set in the FIFO Error Status Register. This condition can be cleared by writing a logical zero to the Softvideo Output Enable Bit (in Table 4); however, this doesn't reset the FIFO Status Register bit, which can only be cleared by issuing a RESET or by reading the FIFO Error Status Register through the I^2C interface. Issuing a RESET (via the RESET* input or RESET packet) can also be used to reset this condition. See "RESET Actions" on page 46.

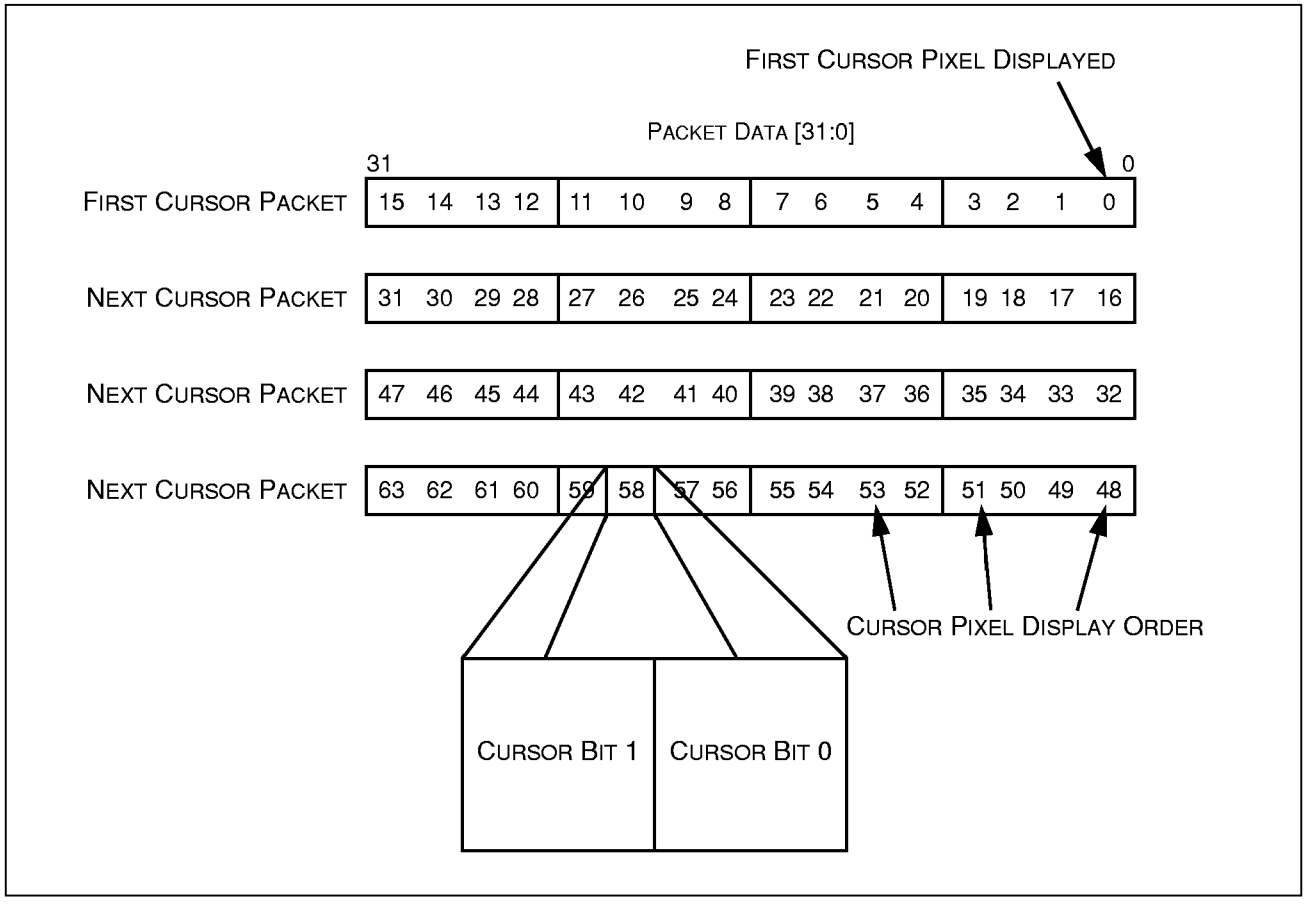
Cursor Operation

The cursor is positioned on the screen by loading the Cursor X Position Register. The value loaded is taken to be relative to the rising transition of the cursor origin bit in the horizontal timing state word. The cursor FIFO must be loaded prior to the assertion of cursor origin in the horizontal timing state machine; cursor packet data arriving after cursor origin will not be displayed until the next rising edge of cursor origin, after the cursor counter has expired. Four cursor words (i.e. 64 cursor pixels) may be displayed per scan line. Any remaining cursor packets will be held until the next time that the cursor counter expires.

If the cursor FIFO is underrun, then the cursor is transparent. When underrun, subsequent cursor packets when the cursor counter again expires. The display of the cursor has priority over video and graphics data, but not border. The cursor mode is selected by writing the Configuration Register. The bit definitions for this register are shown in Table 4.

The format of the cursor packet is shown in Figure 12.

Figure 12. Cursor Packet Format



Cursor Modes

The truth table for the colors displayed in each of the cursor modes is shown in Table 19. For the complement case, the data that would have been presented to the graphics DACs would be bit-wise complemented.

Table 19. Cursor Color Determination

Cursor Bits		Cursor Mode			
1	**0**	**00**	**01**	**10**	**11**
0	0	Cursor is disabled, i.e., always transparent.	Transparent	Cursor Color 1	Transparent
0	1		Cursor Color 1	Cursor Color 2	Transparent
1	0		Cursor Color 2	Transparent	Cursor Color 1
1	1		Cursor Color 3	Complement	Cursor Color 2

Cursor Positioning

The cursor origin is selected by the cursor origin bit in the horizontal timing state machine (refer to Table 20). Each transition of this bit from a zero to a one causes the Cursor Counter to be reloaded with the current Cursor X Position Register value. Generally, this bit is the same state as the Unload Graphics Bit, with the exception of the partial line displays required by interlaced video formats, or the requirement of positioning the cursor partially off the left edge of the screen. The Cursor Counter is decremented with each rising edge of the pixel clock; when the Cursor Counter reaches zero, the cursor FIFO will be unloaded. Two bits are unloaded for each subsequent pixel clock, until the first occurrence of either

- Four cursor words are unloaded

  - or -

- The cursor FIFO empties

The next cursor pixel can only be unloaded after the cursor counter is again exhausted.

Horizontal Timing State Machine Operation

The horizontal timing state machine is used to control the CRT timing signals (HSYNC, VSYNC, & BLANK), to position the video planes (unload video 1 and unload video 2 signals), and to inform the graphics controller when the input pixel port may begin to be loaded with information for the subsequent horizontal line (LSYNC).

The bits of the horizontal timing state machine word are shown in Table 20.

Table 20. Horizontal Timing State Bit Definitions *(1 of 2)*

Bit(s)	Field	Reset Value	Offset	Description
31	LSYNC	0	—	Line synchronization signal to graphics controller function. This signal is typically used by the controller to determine when data for the subsequent scan line can start being loaded.
30	HSYNC	0	0	Horizontal SYNC output state for current pixel.
29	VSYNC	0	0	Vertical SYNC output state for current pixel.
28	UNLOAD VIDEO 1 (0) Don't unload video 1 pixel (1) Unload video 1 pixel	0	7	For each pixel clock that this timing state bit is asserted, a post scaled video pixel will be unloaded from the video 1 FIFO. An assertive transition on this state bit causes the video 1 interpolator to interpret the current FIFO word as the first word (i.e., containing C_r0 in bits 7–0).
27	UNLOAD VIDEO 2 (0) Don't unload video 2 pixel (1) Unload video 2 pixel	0	7	For each pixel clock that this timing state bit is asserted, a post scaled video pixel will be unloaded from the video 2 FIFO. An assertive transition on this state bit causes the video 2 interpolator to interpret the current FIFO word as the first word (i.e., containing C_r0 in bits 7–0).
26	UNLOAD GRAPHICS (0) Don't unload graphics pixel (1) Unload graphics pixel	0	0	For each pixel clock that this timing state bit is asserted, a graphics pixel will be unloaded from the graphics FIFO. For any given pixel, if the graphics is not unloaded, and BLANK* is not active, then the border color will be displayed. An assertive transition on this state bit causes the graphics unpacking logic to reset to the beginning of the current graphics FIFO word.
25	BLANK*	0	0	Composite blank input to DACs for current pixel. Used internally by DACs.
24	SYNC*	0	0	Composite sync input to Green DAC for current pixel. This bit is a don't care if sync on green is not enabled.

Table 20. Horizontal Timing State Bit Definitions *(2 of 2)*

Bit(s)	Field	Reset Value	Offset	Description
23–18	Reserved	—	—	Reserved for other timing controls as needed. These bits will be ignored by the BtV2487.
17	Cursor Origin Position	0	2	Each rising edge of this signal is used by the cursor logic for the cursor origin.
16	Graphics Diagnostic Logic Enable (0) Diagnostic Logic Suspended (1) Diagnostic Logic Active	0	0	Used for controlling the diagnostic logic at the RGB DAC inputs. See "Diagnostic Circuitry" on page 38.
15–12	Reserved	—	—	Reserved for other timing controls as needed. These bits will be ignored by the BtV2487.
11–0	Pixel Count	1	N/A	Number of pixel clocks to maintain state bits 31–16. When this count is exhausted, the next word from the Horizontal Timing FIFO is loaded as the new horizontal timing state. Specifying a count of zero yields unpredictable results.

Due to pipelining differences between the individual state bits within the BtV2487, the actual pixel position at which a particular state bit transition will become effective may differ from other bits within the same word. This difference is indicated in the offset column of Table 20. It should be noted that, in general, to accomplish a simultaneous transition of two or more state bits may require two or more timing words.

If and when the timing generator FIFO is underrun, the outputs for the last received word will be maintained; the count will be suspended and a new timing word will become active as soon as it is received.

Overrun/Underrun Error Conditions

The horizontal timing state machine has error indicators in the FIFO Error Status Register for FIFO overrun and underrun conditions. The overrun status bit is set whenever a timing word load is attempted with a full timing FIFO. The underrun status bit is set whenever new timing state word is required, but the timing FIFO is empty, except that, after reset, the underrun status bit is prevented from being set until two timing words have been loaded. The first word loaded into the timing FIFO after reset will not be unloaded until a second timing word is loaded.

Diagnostic Circuitry

The BtV2487 incorporates circuitry in the graphics and softvideo output paths to provide diagnostic capabilities. This circuitry operates in two modes, signature analysis and data strobe. The mode is selected by programming an internal control register. See Table 4. The diagnostic circuitry should be disabled to reduce power consumption during normal operation.

Signature Analysis Mode

When this mode is enabled, each sample presented to an output DAC is used to generate an accumulated signature over a number of samples. The idea is that, when starting with the same seed (i.e., initial value) the same signature will be generated if the same sequence of sample data is applied to the signature logic. The resulting signature is then read and compared with a "golden" signature which is known.

Data Strobe Mode

When this mode is enabled, each sample data item presented to an output DAC is loaded into the Diagnostic Register. As each new sample overwrites the old one, only the last sample presented with this logic enabled will be in the Diagnostic Register.

Graphics Diagnostic Register

The Graphics Diagnostic Register is 24 bits wide and, when enabled, operates on each of the 8-bit samples presented to the Red, Green, and Blue graphics DAC inputs. The mapping of the fields is shown in Table 3. The composite sync and blank signals are not captured. The representative circuit used to acquire signatures is shown in Figure 13. The representative circuit for each signature register bit is shown in Figure 14. The signature registers capture zeroes when sampling pixel data during the blanking interval.

Figure 13. Graphics Signature Analysis Register Circuit

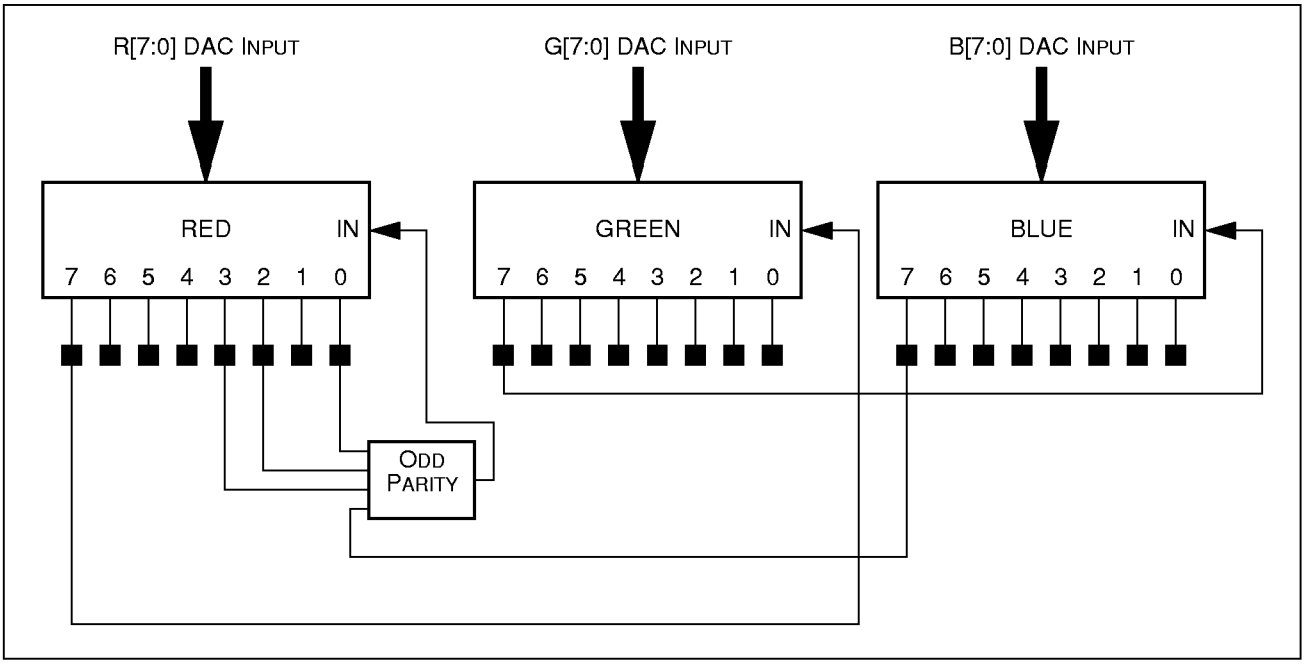
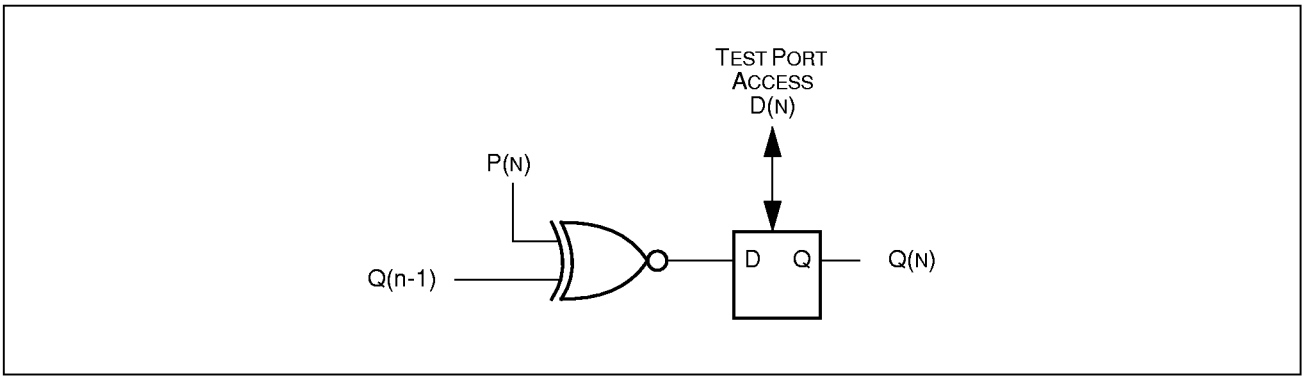


Figure 14. SAR Register Bit Detail



SEV Diagnostic Register

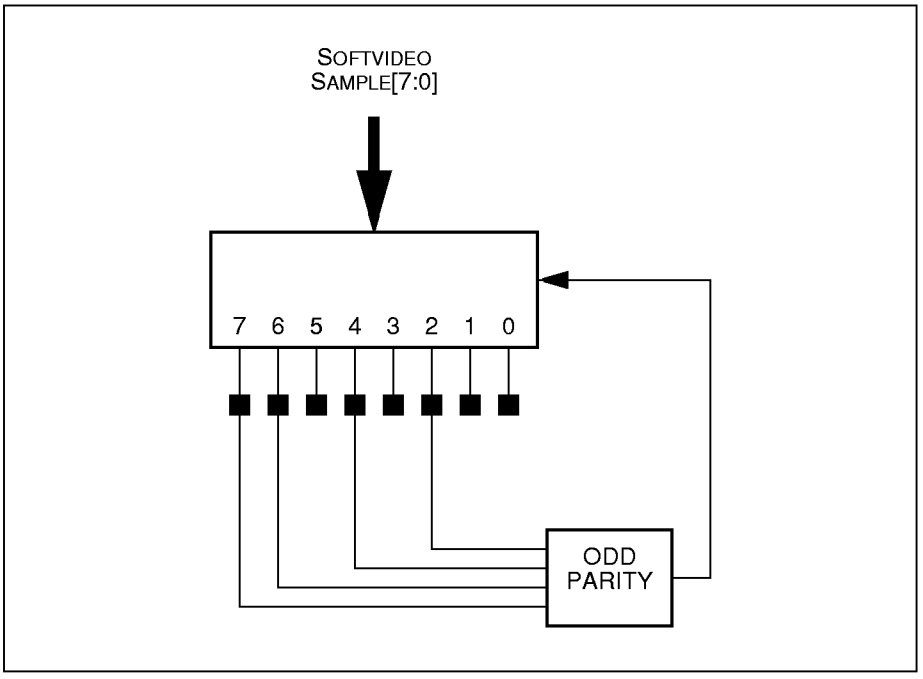
The SEV Diagnostic Register is 8 bits wide and, when enabled, operates on the 8-bit sample of the softvideo DAC. The mapping of the bits is shown in Table 22. The bit positions show where the data is captured (data strobe mode) or applied for signature acquisition (signature mode). The representative circuit used to acquire signatures is shown in Figure 15.

The exact data over which signatures are acquired is controlled by the SEV Diagnostic Logic Enable bit in the RLE word See Table 17. The SEV Diagnostic Register is automatically disabled when the SEV logic is not enabled, or completes processing an RLE word which has the FREEZE bit asserted.

Table 22. SEV Diagnostic Register

Bit(s)	Field Name	Description
7–0	SEV Sample	

Figure 15. Softvideo Signature Analysis Register Circuit



I²C Interface

A standard I²C interface is provided for in-circuit diagnostic and test capability. This interface is provided on two pins, SDA (Serial DAta), and SCL (Serial CLock). This general I²C specification is contained in the 1992 Phillips *I²C Peripherals for Microcontrollers Data Handbook*. Specific commands to which the BtV2487 respond are described in this section. The BtV2487 operates as a slave device on this interface.

This interface may be used to read back the chip ID information, version, features, diagnostic registers, and comparator circuitry status. This is a read back interface only. The BtV2487 I²C implementation uses the 10-bit extended addressing mode. The BtV2487's I²C address is binary 10 1110 0000. The BtV2487 I²C controller is a slave only device supporting one write command and two read commands. See Table 23 for a description of the supported commands.

Table 23. I²C Commands

Command	Name	Description
$12	Read Long Scan Data	This command causes the BtV2487 to return the long scan data chain on the subsequent I²C read.
$13	Read Short Scan Data	This command causes the BtV2487 to return the short scan data chain on the subsequent I²C read.
All Others	Noop	The write command will be ACK'ed, the subsequent read command will be ignored.

The I²C short scan map is shown in Table 24. The I²C long read scan map is shown in Table 25.

Table 24. I²C Short Read Scan Map

Byte	Bit(s)	Field	Description
0	7–3	Revision(4–0) $0A	
	2–0	Chip ID(4–0) $13	
1	7,6		
	5–1	Model(4–0) ($04) BtV2487CHF/ASF	
	0	Monitor Sense	This output is used to determine the presence of a CRT monitor, and, with diagnostic code, the difference between a loaded or an unloaded rgb line can be discerned. The reference is generated by a voltage divider the external 1.235 V voltage reference on the VREF pin. For the proper operation of the comparator circuit, the levels shown in the operating conditions should be applied to the comparator by the IOR, IOG, and IOB outputs. Note: SENSE voltages are subject to change upon completion of characterization. There is an additional ±10-percent tolerance on the above levels when the internal voltage reference is used. If SYNC* is logical zero, SENSE* is stable. The SENSE* output can drive only one CMOS load.
2	7–1	Reserved	These bits read back as zero.
	0	Softvideo Complete	
3	7–0	Reserved	These bits read back as zero.

Table 25. I²C Long Read Scan Map

Scan Byte	Scan Bit(s)	Internal Register Bit
0	7–0	SEV Diagnostic Register, Bits 7–0
1	7–0	Graphics Diagnostic Register, Blue Bits 7–0
2	7–0	Graphics Diagnostic Register, Green Bits 7–0
3	7–0	Graphics Diagnostic Register, Red Bits 7–0
4	7	I/O Write FIFO Overrun
	6	Timing Generator FIFO Underrun
	5	Timing Generator FIFO Overrun
	4	Cursor FIFO Overrun
	3	Video 2 FIFO Underrun
	2	Video 2 FIFO Overrun
	1	Video 1 FIFO Underrun
	0	Video 1 FIFO Overrun
5	7	Graphics FIFO Underrun
	6	Graphics FIFO Overrun
	5–0	Reserved. These bits will read back as zero.

I²C 10 Bit Addressing Mode

When a 10-bit address match occurs on a write command and the command byte is a 0x12, a Read Long Scan command is specified. Immediately after an I²C read is received by the BtV2487, it begins to return the data specified in Table 25.

The Diagnostic Registers should be disabled before issuing an I²C write command addressing the long scan path. FESR updates are discarded during the long scan data read.

I²C 10-bit devices must first be addressed by a 10-bit write before they can be read, via the repeated start mechanism. In the BtV2487, one must immediately follow the write command byte with a repeated start pulse followed by the read command.

The protocol for a Read Long Scan Data looks like:

1. Start Pulse
2. Address Byte (I²C standard) (write)
3. 10-Bit Address Byte (I²C 10 bit addressing)
4. Command Byte (0x12)
5. Start Pulse (repeated)
6. Address Byte (I²C standard) (read)
7. Long Scan Data (from the BtV2487) (6 bytes)

When a 10-bit address match occurs on a write command and the command byte is a $13, a Read Short Scan Data command is specified. Immediately after an I²C read is received by the BtV2487, it begins to return the data shown in Table 24.

As is the case with the Read Long Scan Data command, 10-bit devices must first be addressed by a 10 bit write before they can be read, via the repeated start mechanism. In the BtV2487, one must immediately follow the write command byte with a repeated start pulse followed by the read command.

The protocol for the Read Short Scan Data looks like:

1. Start Pulse
2. Address Byte, (w/2 high bits of 10-bit address) (I²C standard) (write)
3. Low 8 bits of 10-Bit Address Byte (I²C 10-bit addressing)
4. Command Byte (0x13)
5. Start Pulse (repeated)
6. Address Byte (I²C standard) (read)
7. Read Short Scan Data (from the BtV2487) (4 bytes)

All other commands addressed to the BtV2487's 10 bit address are acked and ignored.

Note: you must read all bytes from the BtV2487 on the Read Long Scan Data command. Failure to do so will leave the scan loop registers in the BtV2487 in an unknown and ill defined state. Furthermore, such BtV2487 functions as

- SEV Diagnostic Register
- Graphics Diagnostic Register

must be disabled within the BtV2487 before this command is attempted. All other commands addressed to the BtV2487's 10 bit address are acked and ignored.

FIFO Error Status Register

The bits in the FIFO Error Status Register are mapped as shown in Table 26. Error conditions in the FIFO Error Status Register bits are reset on each read of this register. Secondary errors occurring within the same FIFO will not cause additional error bits to be asserted (e.g., an underrun condition occurring after an overrun in the same FIFO). When this register is being read from the I^2C Interface, the setting of bits is blocked for the duration of the I^2C scan read.

Table 26. FIFO Error Status Register *(1 of 2)*

Bit(s)	Field	Reset Value	Description
15	Monitor Sense (0) At least one DAC output exceeds reference (1) No DAC output exceeds reference	—	This bit is a logical zero if one or more of the IOR, IOG, or IOB outputs have exceeded the internal voltage reference level of the sense comparator circuit.
14–11	Reserved	0	
10	I/O Write FIFO Overrun (0) Didn't occur (1) Occurred	0	
9	Timing Generator Underrun (0) Didn't occur (1) Occurred	0	Indicates that an underrun condition has occurred in the horizontal timing state machine after at least one valid timing word had been loaded after reset.
8	Timing Generator Overrun (0) Didn't occur (1) Occurred	0	
7	Reserved	0	
6	Cursor FIFO Overrun (0) Didn't occur (1) Occurred	0	
5	Video 2 FIFO Underrun (0) Didn't occur (1) Occurred	0	
4	Video 2 FIFO Overrun (0) Didn't occur (1) Occurred	0	

Table 26. FIFO Error Status Register *(2 of 2)*

Bit(s)	Field	Reset Value	Description
3	Video 1 FIFO Underrun (0) Didn't occur (1) Occurred	0	
2	Video 1 FIFO Overrun (0) Didn't occur (1) Occurred	0	
1	Graphics FIFO Underrun (0) Didn't occur (1) Occurred	0	
0	Graphics FIFO Overrun (0) Didn't occur (1) Occurred	0	

RESET Actions

When the external reset pin is asserted, or a packet reset sequence is issued, the following actions occur:

1. All internal registers are loaded with their reset values. See Table 3. Note exceptions stated for PLL Control Registers.
2. All FIFO's are reset (emptied).
3. The Timing Generator enters its reset state. See Table 20.
4. The SEV decoder logic is reset.

To issue a packet reset, at least 15 consecutive reset packets must be sent; to issue a pin reset, RESET* must be asserted for at least 10 CLK25 cycles. This assumes that the power supplies have stabilized *before* counting the assertion of any RESET* signal.

PIN INFORMATION

Pin Descriptions

(1 of 2)

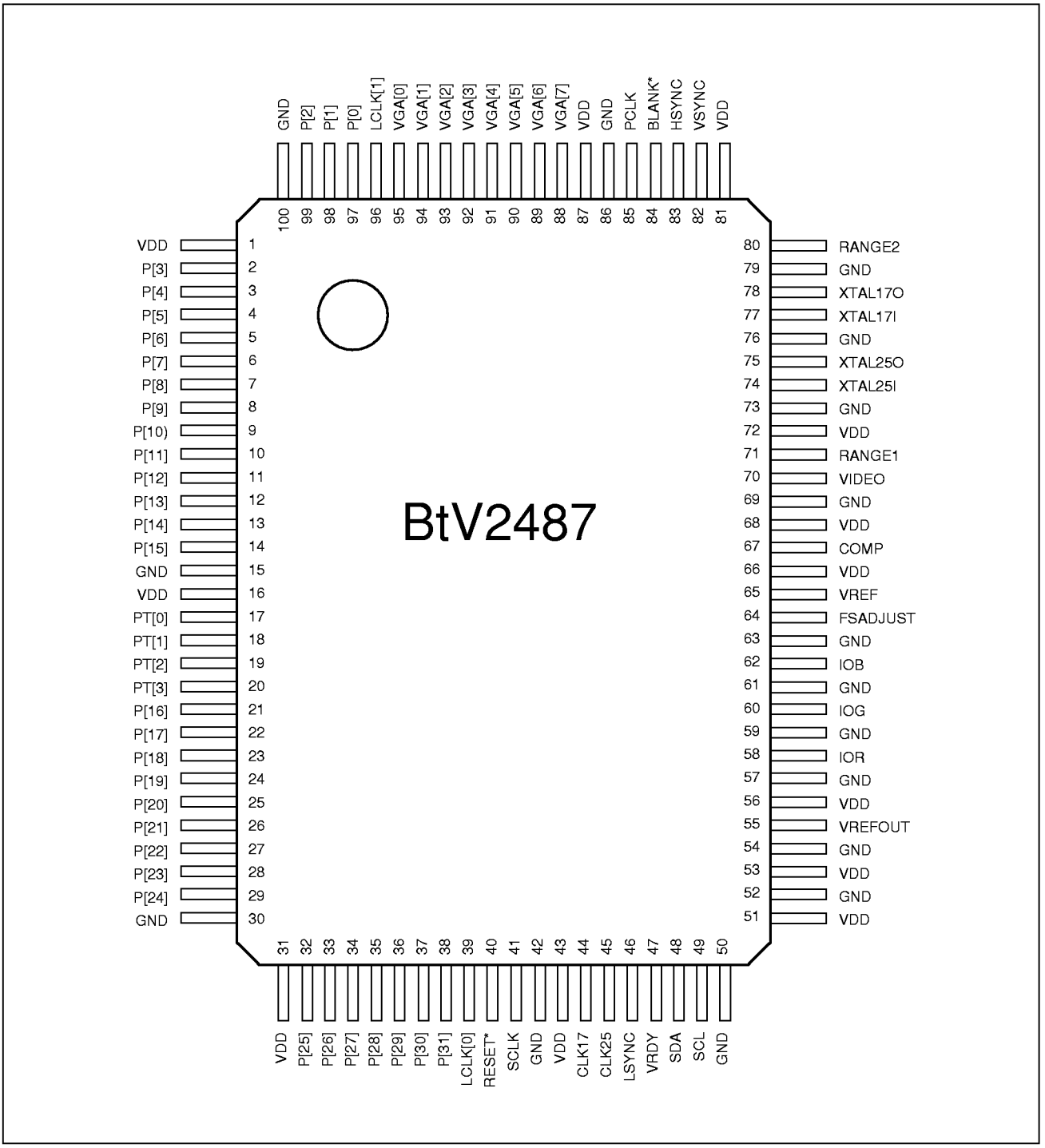
Pin Count	Signal Name	I/O	Description
2	LCLK[0:1]	I	Input Pixel and Pixel Type Load Clock (TTL Compatible). Packet and packet type data from PT[3:0] and P[31:16] are loaded with each rising edge of LCLK[0]; P[15:0] are loaded with each rising edge of LCLK[1].
32	P[31:0]	I	Packet Input Data Bus (TTL Compatible). These are internally registered with the rising edge of LCLK[0] and LCLK[1] for P[31:16] and P[15:0], respectively.
4	PT[3:0]	I	Packet Type Data Bus (TTL Compatible). These inputs are registered with the rising edge of LCLK[0].
1	VIDEO	O	NTSC/PAL analog composite video output channel.
1	XTAL25I	I	24.576 MHz Crystal Input.
1	XTAL25O	O	24.576 MHz Crystal Output.
1	CLK25	O	24.576 MHz Clock Output.
1	XTAL17I	I	16.9344 MHz Crystal Input.
1	XTAL17O	O	16.9344 MHz Crystal Output.
1	CLK17	O	16.9344 MHz Clock Output.
1	SCLK	O	Serial Clock Output (TTL Compatible).
1	LSYNC	O	Horizontal State Machine Status Output (TTL Compatible).
1	VRDY	O/Z	Video FIFO Ready Status Output (TTL Compatible). This signal is three-stated on reset assertion and is enabled via an internal control register bit.
3	IOR, IOG, IOB	O	Analog Current Outputs.
1	HSYNC	I/O	Horizontal Sync Output (TTL Compatible).
1	VSYNC	I/O	Vertical Sync Output (TTL Compatible).
8	VGA[7:0]	I/O/Z	VGA Connector Output (TTL Compatible).

(2 of 2)

Pin Count	Signal Name	I/O	Description
1	BLANK*	I/O	VGA Connector Blank Output (TTL Compatible)
1	PCLK	I/O	VGA Pixel Clock Output (TTL Compatible).
1	FSADJUST	I	Full scale adjust input.
1	VREF	I	Voltage Reference input.[1]
1	N/C		No Connection. This pin should remain floating.
1	COMP	O	Compensation.
1	SCL	I/O/Z	I^2C Interface Serial Clock (Open Drain).
1	SDA	I/O/Z	I^2C Interface Serial Data (Open Drain).
2	RANGE1,2		PLL Range
1	RESET*	I	Reset Input (TTL Compatible).
12	VDD		Power. All VDD pins must be connected together on the same PCB plane to prevent latchup.
16	GND		Ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
100	Total Pin Count		

1. If an external voltage reference is used, it must supply this input with a 1.235 V (typical) reference.

Pin Assignments



Absolute Maximum Ratings

Table 27. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA, VDD (measured to GND)				7.0	V
Voltage on Any Signal Pin		GND – 0.5		VDD + 0.5	V
Analog Output Short Circuit Duration to Any Power Supply or Common	I_{SC}		indefinite		
Ambient Operating Temperature	T_A	–55		+125	°C
Storage Temperature	T_S	–65		+150	°C
Junction Temperature	T_J			+150	°C
Vapor Phase Soldering (1 minute)	T_{VSOL}			220	°C

Stresses above those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage values on any signal pin that extend beyond the power supply rails by more than the amount(s) specified above can cause destructive latchup.

Recommended Operating Conditions

Table 28. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Load Capacitance on digital outputs: VGA[7:0], BLANK*, HSYNC, VSYNC, PCLK			25	pF
Load Capacitance on clock outputs: CLK17, CLK25, SCLK, VRDY, LSYNC			30	pF
Supply Voltage	4.75	5.00	5.25	V
Junction Temperature T_j	0		125	°C
LCLK[0] to LCLK[1] delay	5			ns
Ambient Operating Temperature. See the "Power Dissipation" section.	0		50	°C
RSET Resistor (Setup = 7.5 IRE)		442		Ω
RSET Resistor (Setup = 0 IRE)		409		Ω

Target DC Characteristics

Target DC Characteristics are shown in Table 29. Power dissipation figures are shown in Table 35.

Table 29. Target DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
DAC Low Voltage Sense (external VREF)				260	mV
DAC Low Voltage Sense (internal VREF)				234	mV
DAC High Voltage Sense (external VREF)		410			mV
DAC High Voltage Sense (internal VREF)		451			mV
Analog Outputs (IOR, IOG, IOB)					
Resolution (each DAC)		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			Guaran-teed		
Coding					Binary
Analog Output (VIDEO)					
Resolution		8			Bits
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			Guaran-teed		
Coding					Binary

Table 29. Target DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	V_{IH}	2.0		V_{DD} + 0.5	V
Input Low Voltage	V_{IL}	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	I_{IH}	–1		1	µA
Input Low Current (Vin = 0.4 V)	I_{IL}	–1		1	µA
Input Capacitance (v = 1 MHz, Vin = 2.4 V)	C_{IN}			7	pF
Hysteresis			0.3		V
Digital Outputs					
Output High Voltage (I_{OH} = –400 µA)	V_{OH}	2.4			V
Output Low Voltage (I_{OL} = 3.2 mA)	V_{OL}			0.4	V
Three-State Current (0–2.4V)	I_{OZ}			50	µA
Output Capacitance (f = 1 MHz, Vout = 2.4 V)	CDOUT			7	pF
Analog Outputs (VIDEO, IOR, IOG, IOB)					
Gray-Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black[1]		16.74	17.62	18.5	mA
Black Level Relative to Blank[1]			1.44		mA
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
RGB DAC-to-DAC Matching		0	2	5	%
Output Compliance	V_{OC}	–0.3		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, Iout = 0 mA, Vout = 1.0 V)	CAOUT			30	pF
Voltage Reference Input Current	IVR IN		0.5		mA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

1. When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

Note: Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, RSET = 442 Ω, VREF = 1.235 V, or alternatively, SETUP = 0 IRE, RSET = 409 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required.

Table 30. Characteristics for SDA and SCL I/O (Fast Mode)

Parameter	Symbol	Min.	Max.	Units
Low level input voltage	V_{IL}	–0.5	1.5	V
High level input voltage	V_{IH}	3.0	V_{DD} + 0.5	V
Hysteresis	V_{hys}	0.2		V
Spike suppression	t_{SP}	0	50	ns
Low level output voltage (open drain) at 3 mA sink current at 6 mA sink current	 V_{OL1} V_{OL2}		 0.4 0.6	 V V
Input current (Vi = 0.4–0.9$V_{DD\ max.}$)	I_i	–10	10	µA
Capacitance	C_i		10	pF

Target AC Characteristics

Table 31. Target AC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typical	Max	Units
LCLK0,1 Input Rate		0		66	MHz
LCLK0,1 Cycle Time	1	15.15			ns
LCLK0,1 Pulse Width High	2	5			ns
LCLK0,1 Pulse Width Low	3	5			ns
RESET* Pin assertion duration to guarantee reset[1]		10			CLK25 cycles
P[31:16], PT[3:0] setup before LCLK[0] rise; P[15:0] setup before LCLK[1] rise	4	1			ns
P[31:16], PT[3:0] hold after LCLK[0] rise P[15:0] hold after LCLK[1] rise	5	2			ns
Internal pixel clock rate		25		110	MHz
SCLK Output Rate		25		66	MHz
SCLK, CLK25, CLK17 Output Duty Cycle		40	50	60	%
I^2C Interface Clock Rate				400	kHz
PCLK Output Rate				30	MHz
PCLK duty cycle		40	50	60	%
Digital output rise time (at maximum capacitive load)	t_r		tbd		ns
Digital output fall time (at maximum capacitive load)	t_f		tbd		ns
LCLK[0] to LCLK[1] delay	6	0			ns
LCLK[1] setup before next LCLK[0]	6a	2			ns
PCLK to VGA[7:0], BLANK* Delay	7	2		10	ns
IOR, IOB skew from IOG		–2	0	2	ns
IOR, IOB IOG settling time			5		ns
HSYNC, VSYNC skew from IOG			2		ns
Analog Output Rise/Fall Time IOR, IOG, IOB VIDEO[2]			 3.7 3.7		 ns ns
Analog Output Settling Time IOR, IOG, IOB VIDEO[3]			 5 tbd		 ns ns

Table 31. Target AC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typical	Max	Units
Clock and Data Feedthrough			–30		db
Glitch Impulse			75		pV-sec
IOR/IOG/IOB Crosstalk			–23		db
IOR/IOG/IOB output skew			0	2	ns

1. See the "RESET Actions" section on page 46.
2. Output rise/fall time is measured between the 10 and 90% points of full scale transition.
3. Settling time is measured from the 50% point of full scale transition to the point at which the output remains within ± 1 LSB of its DC level.

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with external voltage reference, SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 442 Ω. Digital inputs are 0–3 V with input rise/fall times ≤ 3 ns, measured between the 10 and 90% points. Timing reference points are at 50% for inputs and outputs. Analog output load ≤ 10 pf.

Table 32. AC Characteristics for SDA and SCL Bus Lines (Fast Mode)

Parameter	Symbol	Min.	Max	Units
SCL clock frequency		0	400	kHz
Bus free time between a STOP and START condition		1.3		µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6		µs
Low period of the SCL clock		1.3		µs
High period of the SCL clock		0.6		µs
Set-up time for a repeated START condition		0.6		µs
Data hold time		0	0.9	µs
Data set-up time		100		µs
Rise time of both SDA and SCL signals		$20 + 0.1Cb^{1}$	300	ns
Fall time of both SDA and SCL signals		$20 + 0.1Cb^{1}$	300	ns
Set-up time for STOP condition		0.6		µs
Output fall time (10–400pF bus capacitance)	t_{OF}	$20 + 0.1C_b^{2}$	250^{3}	ns
Capacitive load for each bus line			400	pF

1. SDA and SCL lines will not be obstructed if V_{DD} is switched off.
2. C_b = capacitance of one bus line in pF.
3. SDA and SCL lines will not be obstructed if V_{DD} is switched off.

Figure 16. Pixel and Packet Input Timings

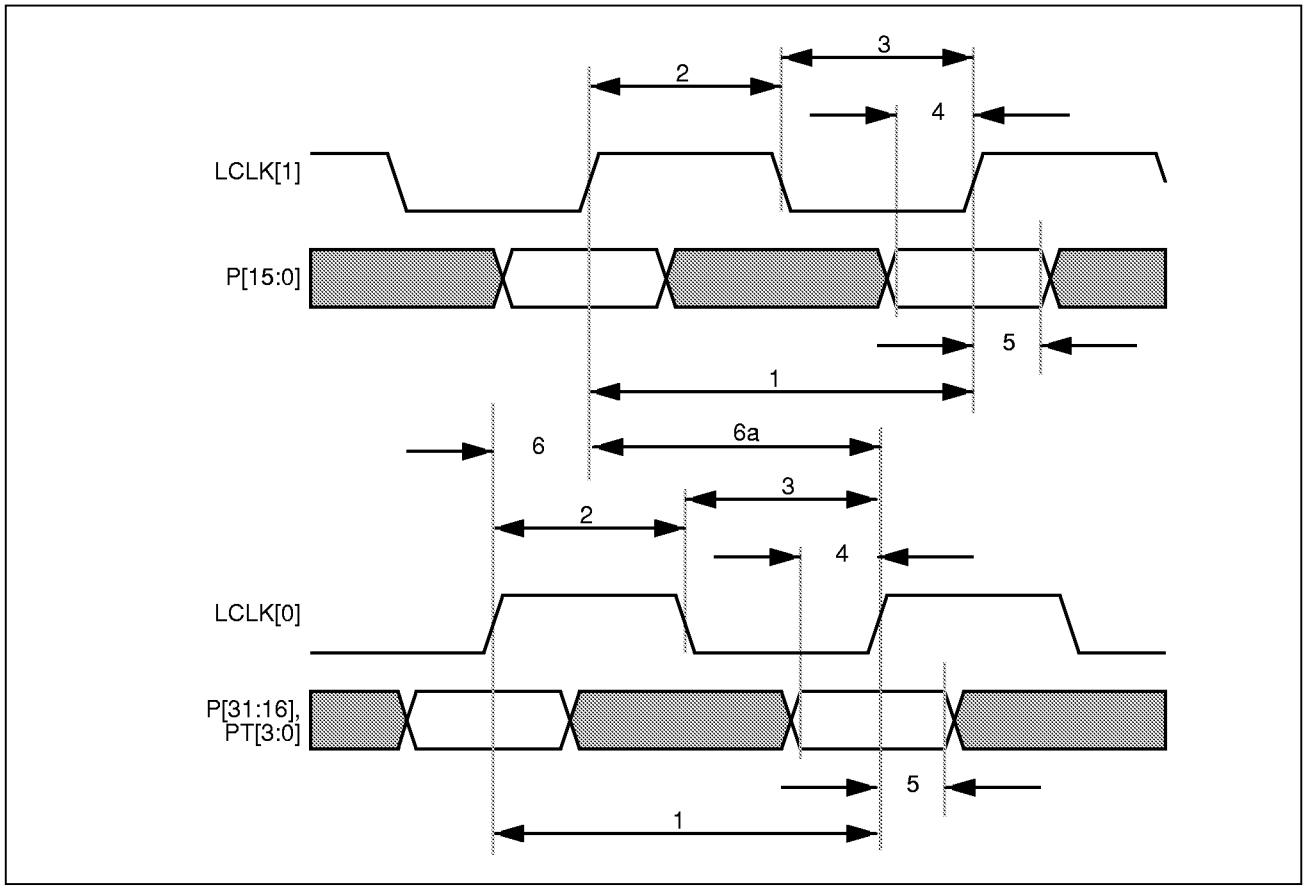
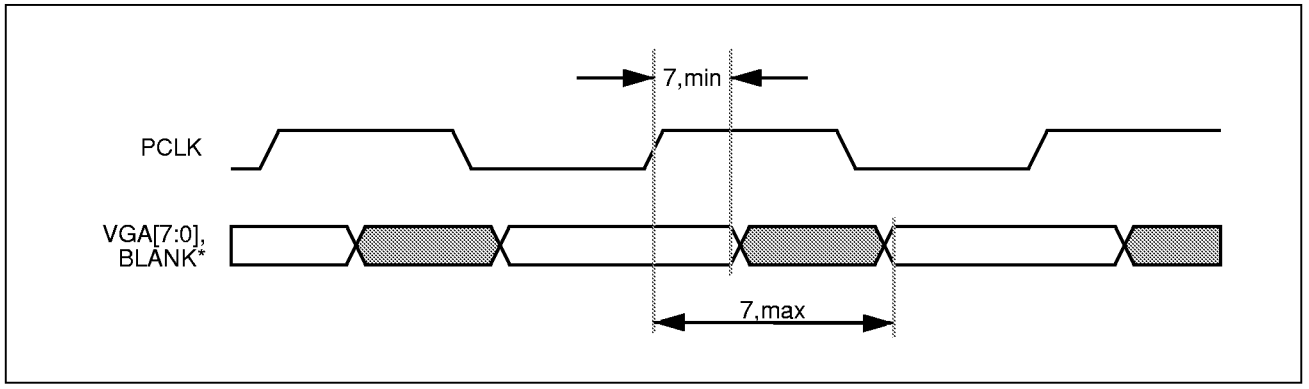


Figure 17. VGA Output Port Timings



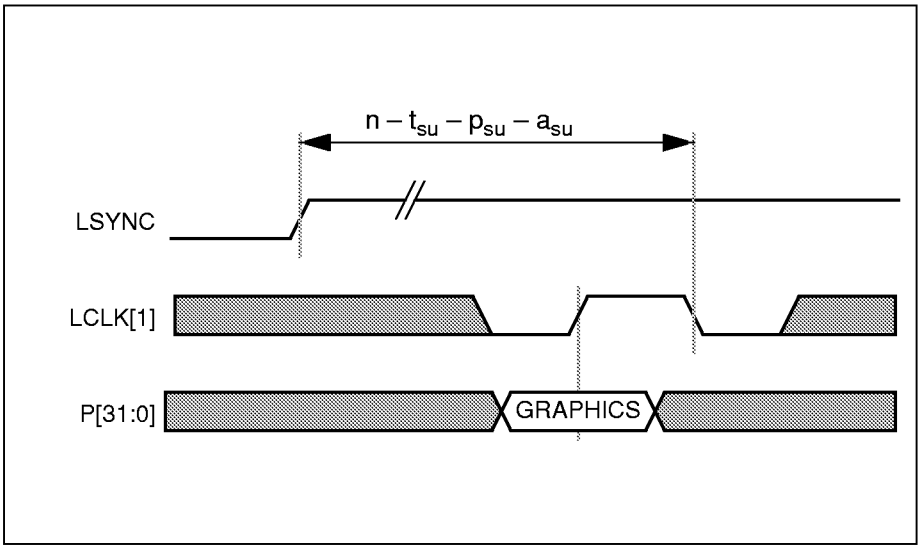
Target FIFO Characteristics

Target FIFO Characteristics are shown in Table 33. These characteristics must be met to prevent FIFO underrun conditions from occurring. The timing diagram corresponding to the Graphics FIFO setup parameters is shown in Figure 18. The variable *n* corresponds to the horizontal timing offset (in pixel clocks) between the assertion of LSYNC and the timing state asserting the unload graphics state bit requiring data supplied at the rising edge of LCLK[1] shown in Figure 18. Not shown, but likewise specified, is the setup time requirements for video 1 and video 2 packet data. The a_{su} applies only to I/O Writes.

Table 33. Target FIFO Characteristics

Parameter	Symbol	Min	Typical	Max	Units
Graphics FIFO Setup	p_{su} t_{su}	3 5			Pixel Clocks ns
Cursor FIFO Setup	p_{su} t_{su}	3 5			Pixel Clocks ns
Video FIFOs Setup	p_{su} t_{su}	5 5			Pixel Clocks ns
Horizontal Timing FIFO Setup	p_{su} t_{su}	3 5			Pixel Clocks ns
I/O Write FIFO Setup	p_{su} a_{su} t_{su}	2 2 5			Pixel Clocks CLKA Clocks ns

Figure 18. Graphics FIFO Setup Requirements



In the case of cursor packet data, *n* applies to the offset (in pixel clocks) to the timing state containing the cursor origin leading edge, where the packet data supplied at the rising edge of LCLK[1] would be the first cursor packet.

I/O Write FIFO Unloading

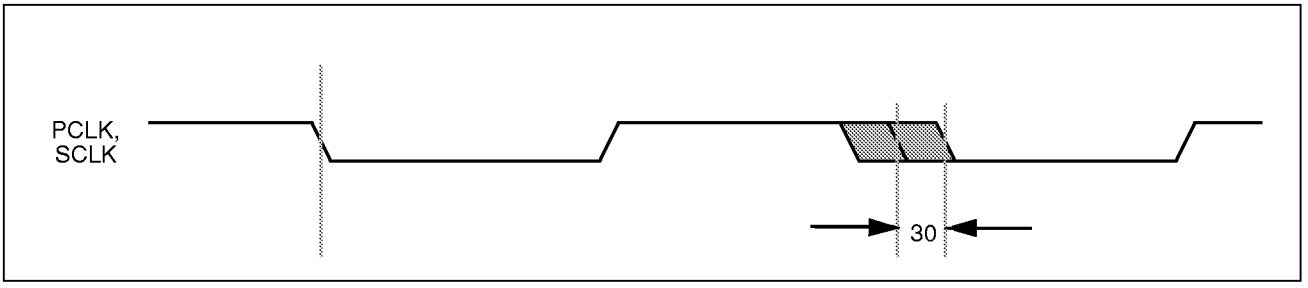
For the I/O Write operation, *n* is the offset (in pixel clocks) to the de-assertion of composite blank to guarantee that the I/O Write packet loaded with the rising edge of LCLK[1], written to an empty I/O Write FIFO would be unloaded within the current blanking interval.

PLL Characteristics

Table 34. Target PLL Characteristics

Parameter	Symbol	Min	Typical	Max	Units
Clock Rate Transition Time				100	ms
VCO Rate		65		170	MHz
M		21		63	
N		4		15	
Total jitter	30	–200		+200	ps

Figure 19. PLL Characteristics



Power Dissipation

Introduction

It is important for the system designer to be aware of the trade-offs regarding cost and reliability in determining package selection and cooling requirements. As a rule, the device junction temperature should not exceed 125 °C to prevent compromising device reliability. The information given in this section is provided to provide the system designer with the data for making these trade-offs.

Power Dissipation

There are a number of factors affecting device thermal performance: air flow, ambient temperature, board thermal characteristics (including copper area and thickness), package thermal characteristics, device power dissipation, power dissipation of surrounding devices, and board power dissipation. The information given in this section assumes that the surrounding devices do not contribute nor block heat dissipation and do not block airflow. It is also assumed that the circuit board contains tbd oz. of copper (combined weight, all layers).

Thermal Resistance

The ability of a package to dissipate power is characterized by the overall thermal resistance of the package. The thermal resistance of the available packages are determined based on experimental data. Device junction to ambient thermal resistance is commonly denoted by the symbol θ_{ja}. Packages having decreased thermal resistance are generally more expensive due to the inclusion of heat slugs, heat spreaders, more expensive lead frames, etc. The thermal resistance of a given package can also be reduced by providing airflow over the package.

Package Power Dissipation

The thermal resistance of a package as a function of power dissipation, junction and ambient temperatures, and is computed using the following expression:

$$\theta_{ja} = \frac{T_j - T_a}{P}$$

where:
- T_j = junction temperature
- T_a = ambient temperature
- θ_{ja} = package thermal resistance
- P = resulting package power dissipation

The thermal resistance at various airflows for the two available BtV2487 packages are shown in Table 36, "Package Thermal Resistance," on page 63.

Recommendations

By using the worst case power dissipation figures for a desired mode of operation and environment, one can deduce the required package thermal resistance. The system designer may then choose the appropriate package. As an example, suppose that the system designer wants to support one video plane at 135MHz, with an ambient temperature of up to 70 °C, and the recommended maximum junction temperature is not to exceed 125 °C. The power dissipation under this mode of operation is 2.37 W. Substituting this into the thermal resistance expression yields a required θ_{ja} of (125 °C–70 °C)/2.37 W = 23 °C/W.

Additional power saving can be made by turning off power to the video FIFOs and softvideo output DAC.

Table 35. Worst Case Power Dissipation

Operating Speed	Max Icc	Max Power[1]
85 MHz	534 mA	2.70 W
110 MHz	587 mA	3.08 W
135 MHz	646 mA	3.39 W
1. Power dissipation numbers are calculated under worst case conditions of 5.25 V, max Icc given a partucular operating speed while not exceeding 125 °C junction temperature. Patterns under which worst case dissipation numbers are obtained, are: Graphics - One Pixel On, One Pixel Off: FF,00,FF,00,... Video - Four Pixels On, Four Pixels Off: FF,FF,FF,FF,00,00,00,00,...		

Table 36. Package Thermal Resistance

Package	Airflow (Linear Feet per Minute)					Units
	0	50	100	200	400	
100-pin Power QUAD	25.3	22.7	21.0	19.0	15.9	°C/W
100-pin MQFP	31.0	28.6	28.0	26.0	24.2	°C/W

Note: Final values are subject to change after device characterization.

Figure 20. MQFP with Heat Spreader Maximum Power vs. Air Flow (Junction Temperature = 125˚C)

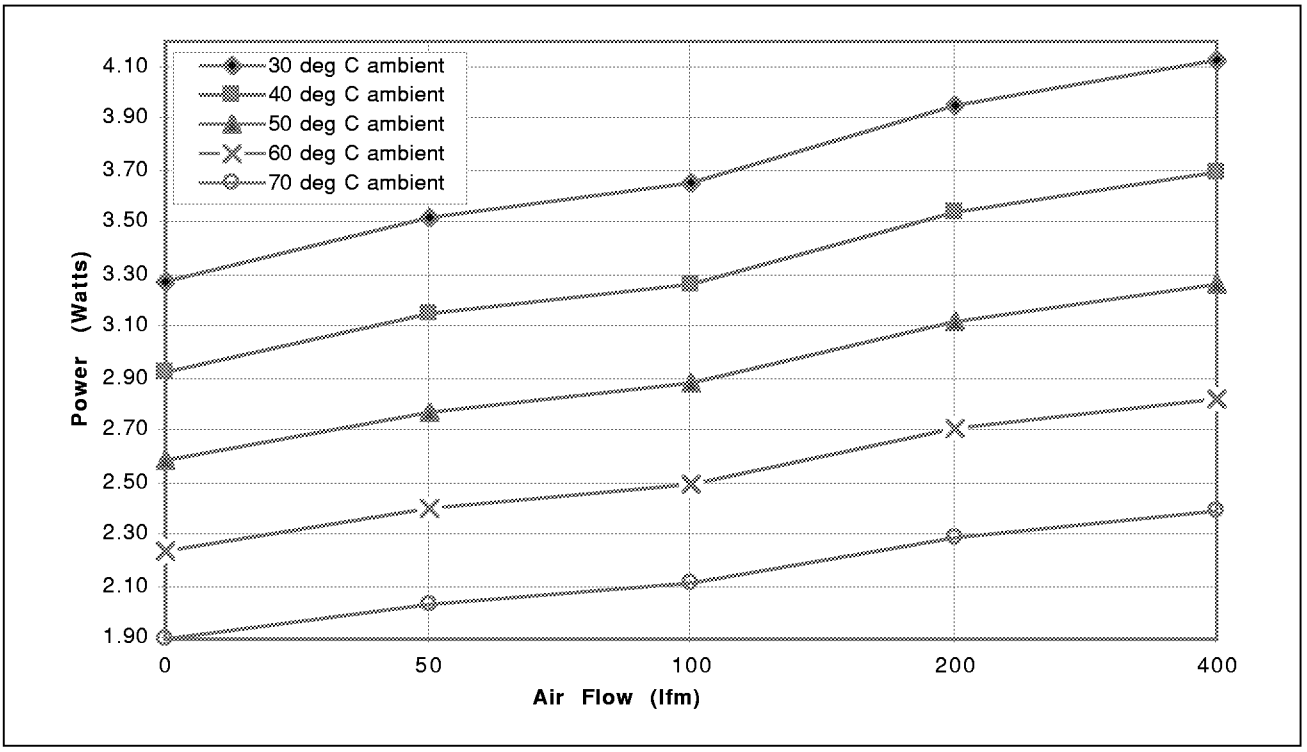
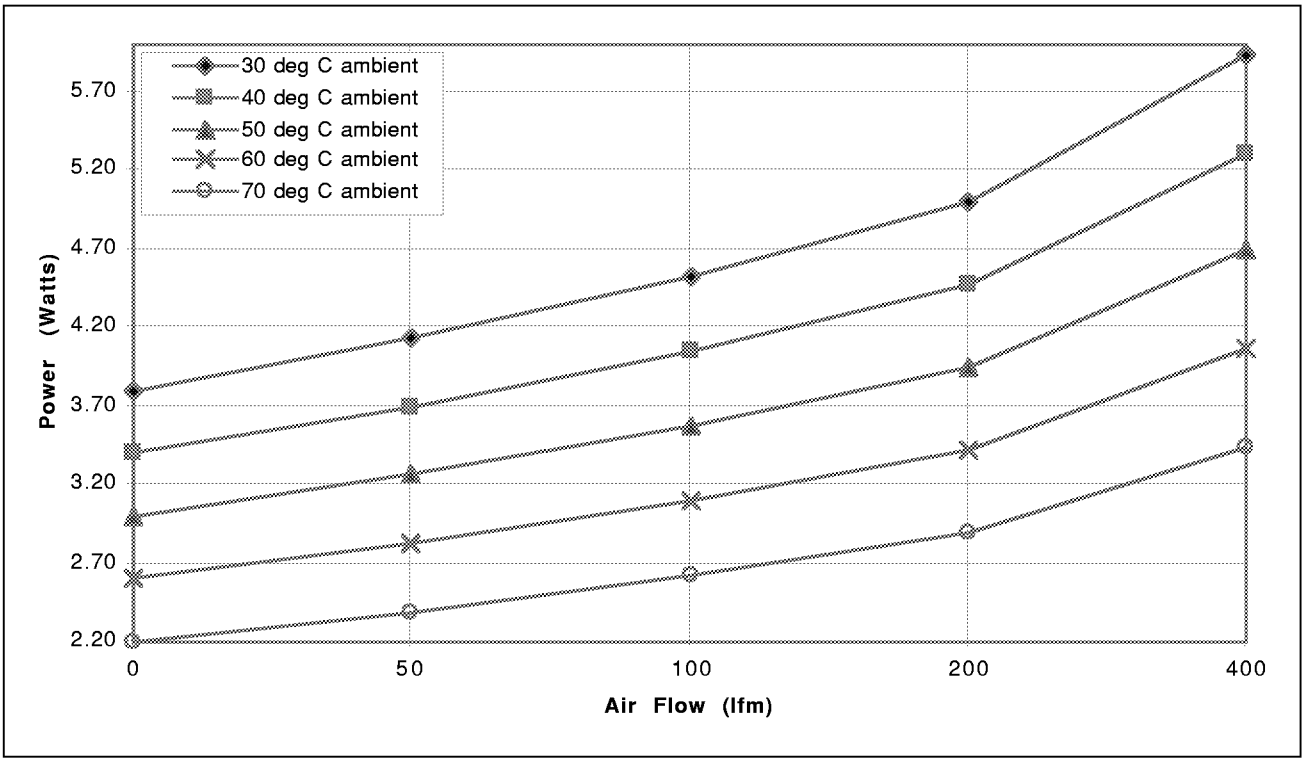
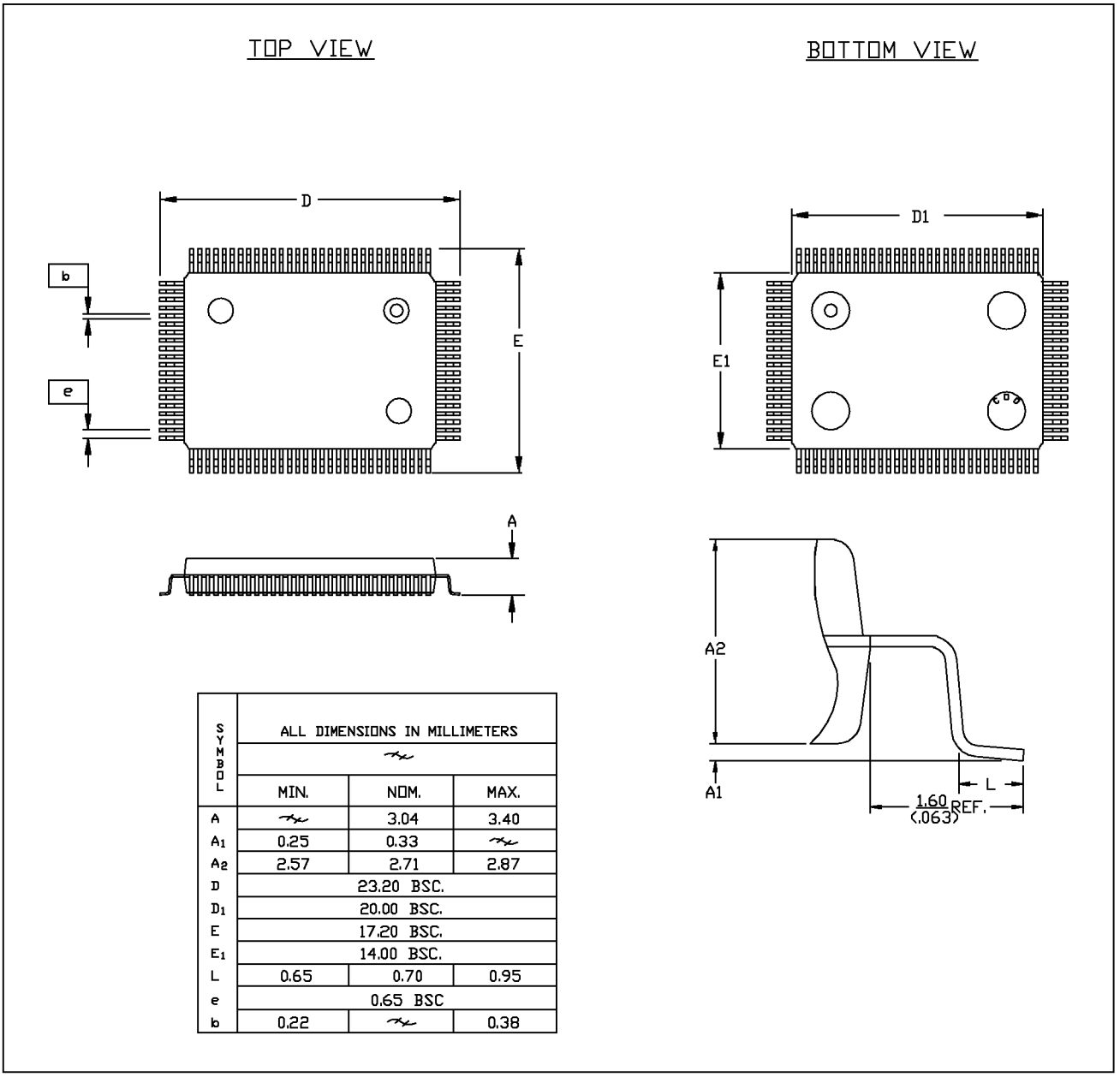


Figure 21. PowerQuad Maximum Power vs. Air Flow (Junction Temperature = 125˚C)



Package Mechanical Drawing

Figure 22. 100MQFP Package Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A		3.04	3.40
A_1	0.25	0.33	
A_2	2.57	2.71	2.87
D		23.20 BSC.	
D_1		20.00 BSC.	
E		17.20 BSC.	
E_1		14.00 BSC.	
L	0.65	0.70	0.95
e		0.65 BSC	
b	0.22		0.38

PC Board Considerations

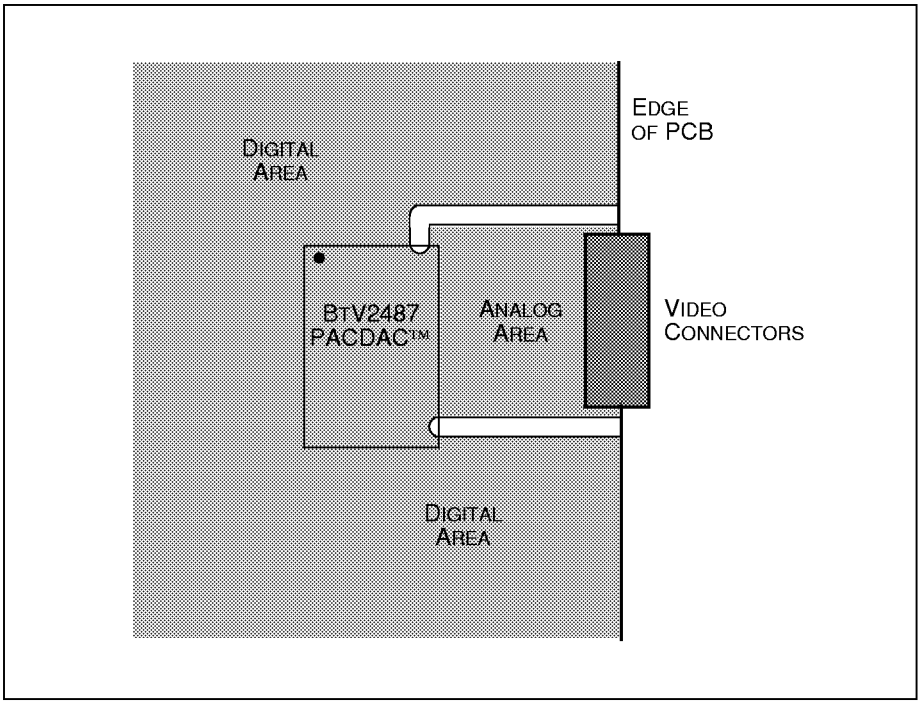
The BtV2487 layout should be optimized for lowest noise on the BtV2487 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length to power and ground pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground planes must provide a low-impedance return path for the digital circuits. A PCB (printed circuit board) with a minimum of four layers is recommended.

Power and Ground Planes

The power and ground planes need isolation gaps to create a quiet area for minimizing digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8" wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. Digital signals should not be routed through the analog area. A sample layout is shown in Figure 23. The upper gap shown originates from the PACDAC™ device between pins 81 and 82; the lower gap originates between pins 52 and 53.

Figure 23. Representative PCB Power/Ground Layout



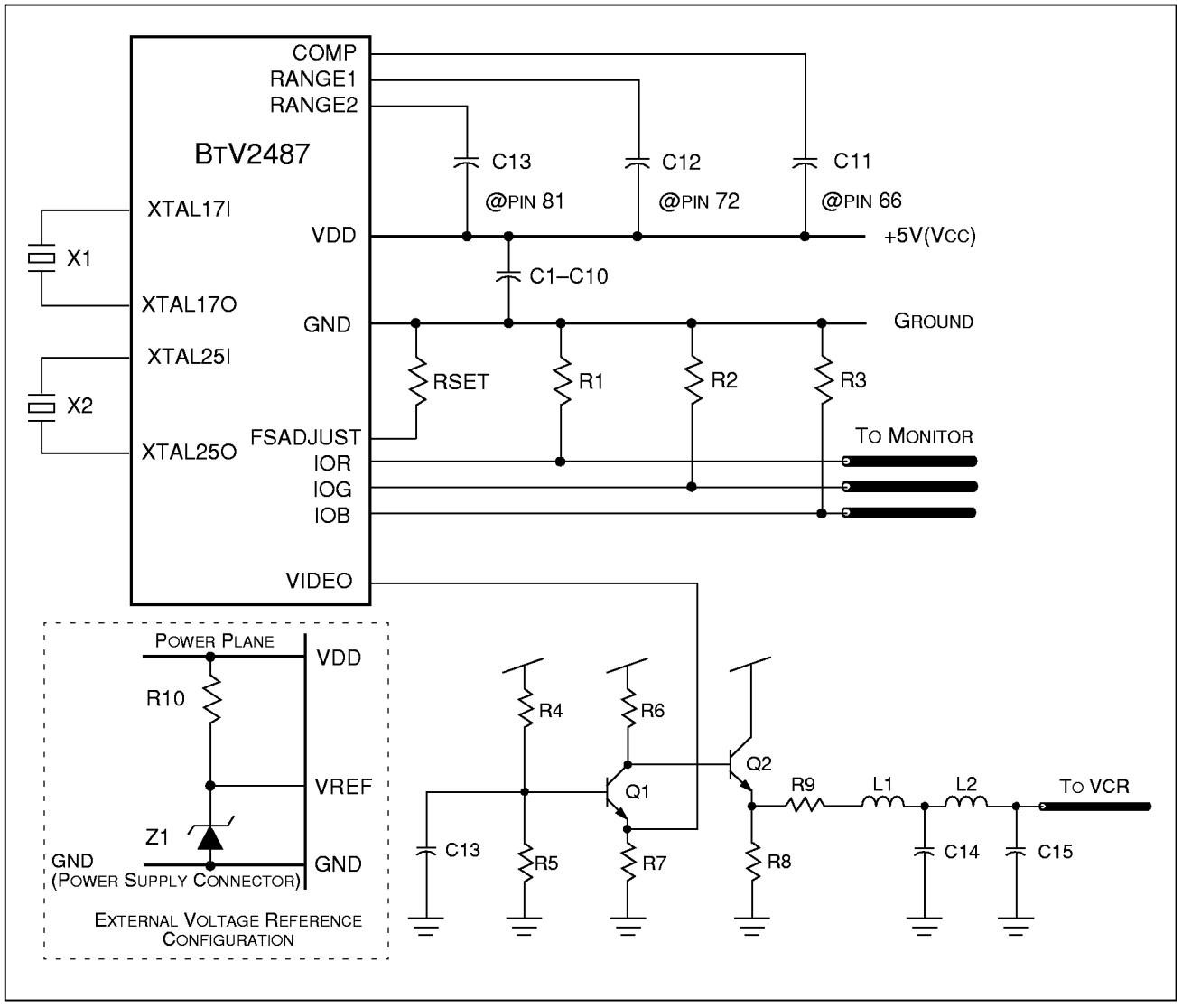
Device Decoupling

The recommended schematic diagram showing power supply decoupling, device decoupling, and analog signal interconnection is shown in Figure 24. The parts list and suggested component placement is shown in Table 37.

Table 37. Parts List

Component(s)	Description	Vendor Part Number	Suggested Placement
C1–C13	0.1 µF ceramic capacitor		C1: between pins 1–100, digital area. C2: between pins 15–16, digital area. C3: between pins 30–31, digital area. C4: between pins 42–43, digital area. C5: between pins 50–51, digital area. C6: between pins 63–66, analog area. C7: between pins 68–69, analog area. C8: between pins 72–73, analog area. C9: between pins 79–81, analog area. C10: between pins 86–87, digital area. C11: between pins 66–67, analog area. C12: between pins 71–72, analog area. C13: between pins 80–81, analog area.
C14	560 pF 5% NPO capacitor		Analog area.
C15	220 pF 5% NPO capacitor		Analog area.
L1	1.5 µH 5% inductor		Analog area.
L2	3.3 µH 5% inductor		Analog area.
Q1, Q2	2N2222 transistor		Analog area.
R1–R3	75 Ω 1% metal film resistor		As close as possible to BtV2487, analog area.
R4	750 Ω resistor		Analog area.
R5	604 Ω resistor		Analog area.
R6	137 Ω resistor		Analog area.
R7	61.9 Ω resistor		Analog area.
R8	210 Ω resistor		Analog area.
R9	75 Ω resistor		Analog area.
R10	1 KΩ 5% resistor		Analog area.
RSET	1% metal film resistor 442 Ω if setup = 7.5 IRE 409 Ω if setup = 0 IRE		Analog area.
Z1	1.2 V voltage regulator	National Semiconductor LM 385 BZ-1.2	Analog area.
X1	16.9344 MHz crystal		As close as possible to BtV2487, analog area. The crystal characteristics are: fundamental mode ONLY parallel res. 20 pf load cap or less 35 ohms ESR or less low holder (aka shunt) cap (<5 pF) AT or BT cut
X2	24.576 MHz crystal		

Figure 24. Typical Connection Diagram



Device Placement

The BtV2487 should be located close to the video output connectors. The graphics video connector and software encoded video output connector should be within the analog board area.

Power Supply Decoupling

A linear regulator is recommended to filter the power supply if the power supply noise is more than 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10 percent of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

Comp Decoupling

The COMP pin must be decoupled to VAA, typically by using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as physically possible to the COMP and VAA at pin 66. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance, which degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital I/O to the BtV2487 should be isolated as much as possible from the analog outputs and other analog circuitry. These signals should not enter any layer of the analog PCB area.

It is also recommended that the P[31:16] and P[15:0] data inputs be skewed from each other to reduce feedthrough noise.

Transmission lines will ring if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time. Line termination or line length reduction are the solutions. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PCB capacitance by routing 90 degrees to any analog signals.

Analog Signal Interconnect

The BtV2487 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The analog video output signal (i.e.: IOR, IOG, IOB) routing should remain on the side of the PCB which is over the ground plane, and within the analog area. By not routing over the power plane, high-frequency power supply rejection is maximized.

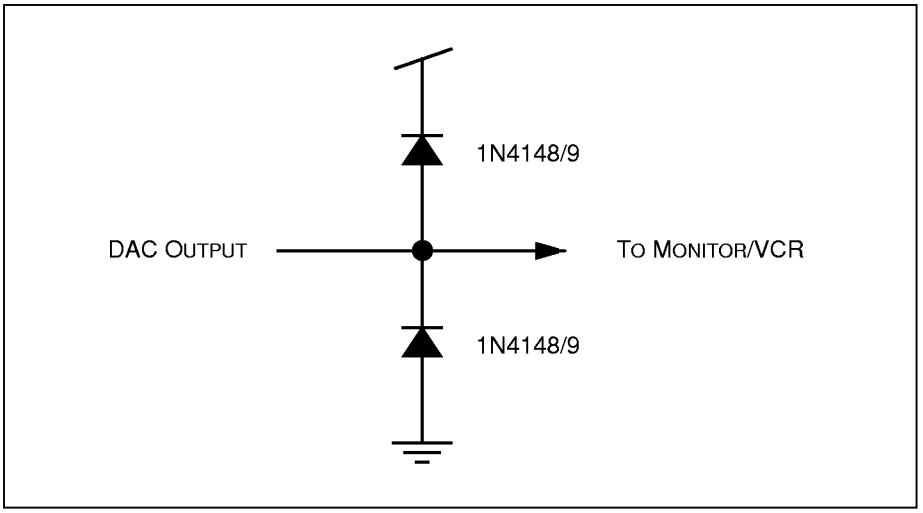
For maximum performance, the analog video output impedance, trace impedance, cable impedance, and load impedance should be the same.

Analog Output Protection

The BtV2487 analog outputs IOR, IOG, IOB, and VIDEO should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 25 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMMBD7001).

Figure 25. Analog Output Protection Circuit



Softvideo Output Filter

The components comprising the SEV output filter, shown in Figure 24, should be contained within the analog area of the PCB. The SEV output connector should also be located within the PCB analog area.

Revision History

Table 38. BtV2487 Datasheet Revision History

Revision	Date	Change	Description
A	9/20/94	Initial Release	
B	12/16/94		
C	2/3/95		
D	8/11/95		