UM61M512 Series

64K X 8, 3.3V I/O High Speed CMOS SRAM

Features

- Single +5V power supply
- Access times: 15/20 ns (max.)
- Current: Operating: 160mA (max.)
  Standby: 10mA (max.)
- Full static operation, no clock or refreshing required
- 3.3V I/O compatible
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 3V (min.)
- Available in 32-pin SKINNY DIP package

General Description

The UM61M512 is a low operating current 524,288-bit static random access memory organized as 65,536 words by 8 bits and operates on a single 5V power supply. It is built using UMC's high performance CMOS process.

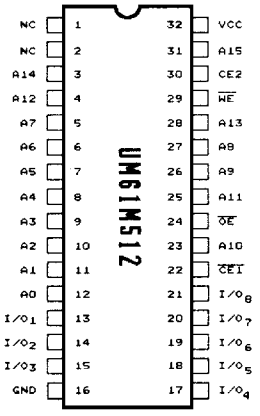
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

Special designed output circuitry allows for easy interfacing with 5V or 3V system bus and is ideal for mixed voltage system design.

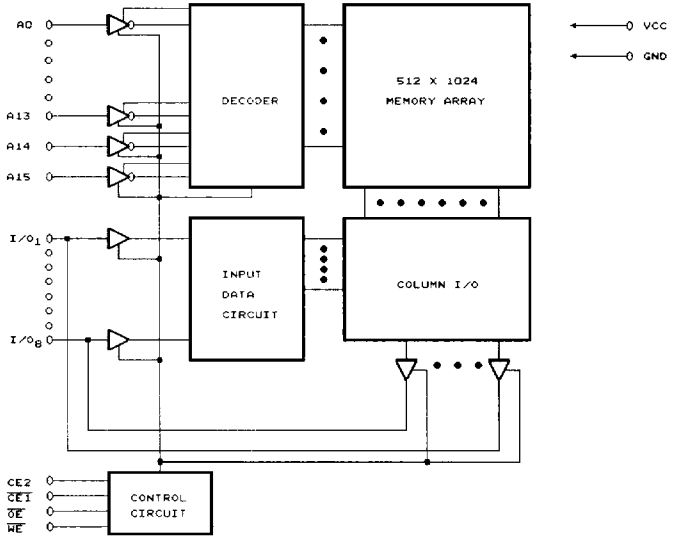
Two chip enable inputs are provided for power down and device enable and an output enable input is included for easy interfacing.

Data retention is guaranteed at power supply voltage as low as 3V.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	Description
3 - 12, 23, 25 - 28, 31	A0 - A15	Address Input
29	$\overline{WE}$	Write Enable
24	$\overline{OE}$	Output Enable
22	$\overline{CE1}$	Chip Enable
30	CE2	Chip Enable
1, 2	NC	No Connection
13-15, 17-21	I/O1 - I/O8	Data Input/Output
32	VCC	Power Supply
16	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.8	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature Under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, P_T 1.0W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 5%, GND = 0V)

Symbol	Parameter	UM61M512-15/20		Unit	Conditions
		Min.	Max.		
$\|I_{LI}\|$	Input Leakage Current	-	2	μA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	-	2	μA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC1} (1)	Dynamic Operating Current	-	160	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0 mA

DC Electrical Characteristics (continued)

Symbol	Parameter	UM61M512-15/20		Unit	Conditions
		Min.	Max.		
I_{SB}	Standby Power Supply Current	–	30	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		–	10	mA	$\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V, V_{IN} ≥ VCC - 0.2V or V_{IH} ≤ 0.2V
I_{SB2}		–	10	mA	$\overline{CE1}$ ≤ 0.2V, CE2 ≤ 0.2V V_{IN} ≥ VCC - 0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	–	0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4	3.3	V	I_{OH} = -4 mA (VCC = 5V)

Note: 1. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns.

Truth Table

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disable	L	H	H	H	High Z	I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC1}

Note: X: H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		8	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 5V ± 5%)

Symbol	Parameter		UM61M512-15		UM61M512-20		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		15	–	20	–	ns
t_{AA}	Address Access Time		–	15	–	20	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	–	15	–	20	ns
t_{ACE2}		CE2	–	15	–	20	ns
t_{OE}	Output Enable to Output Valid		–	7	–	9	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	5	–	5	–	ns
t_{CLZ2}		CE2	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z		2	–	2	–	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	–	10	–	10	ns
t_{CHZ2}		CE2	–	10	–	10	ns
t_{OHZ}	Output Disable to Output in High Z		2	9	2	9	ns
t_{OH}	Output Hold from Address Change		3	–	5	–	ns
Write Cycle							
t_{WC}	Write Cycle Time		15	–	20	–	ns
t_{CW}	Chip Enable to End of Write		12	–	15	–	ns
t_{AS}	Address Setup Time of Write		0	–	0	–	ns
t_{AW}	Address Valid to End of Write		12	–	15	–	ns

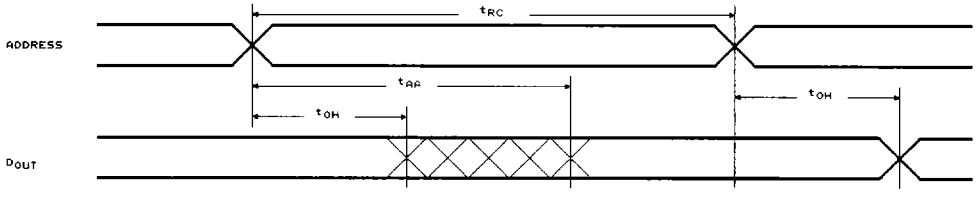
AC Characteristics (continued)

Symbol	Parameter	UM61M512-15		UM61M512-20		Unit
		Min.	Max.	Min.	Max.	
t_{WP}	Write Pulse Width	9	–	11	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z	0	8	0	13	ns
t_{DW}	Data to Write Time Overlap	7	–	7	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	ns

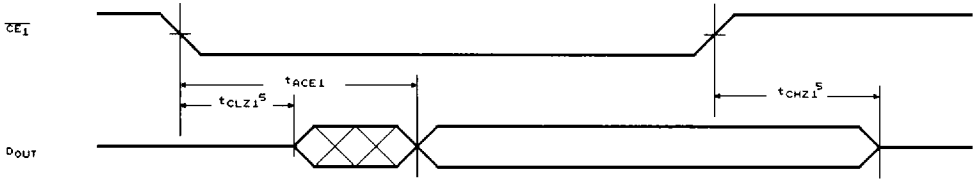
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1, 2, 4)

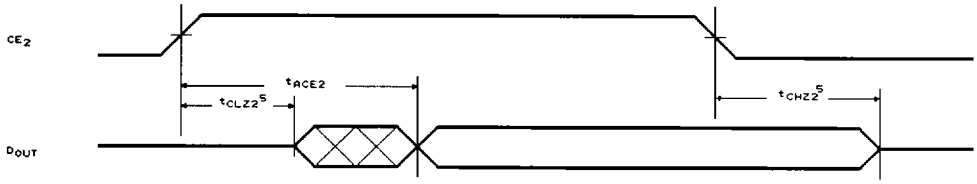


Read Cycle 2 (1, 3, 4, 6)

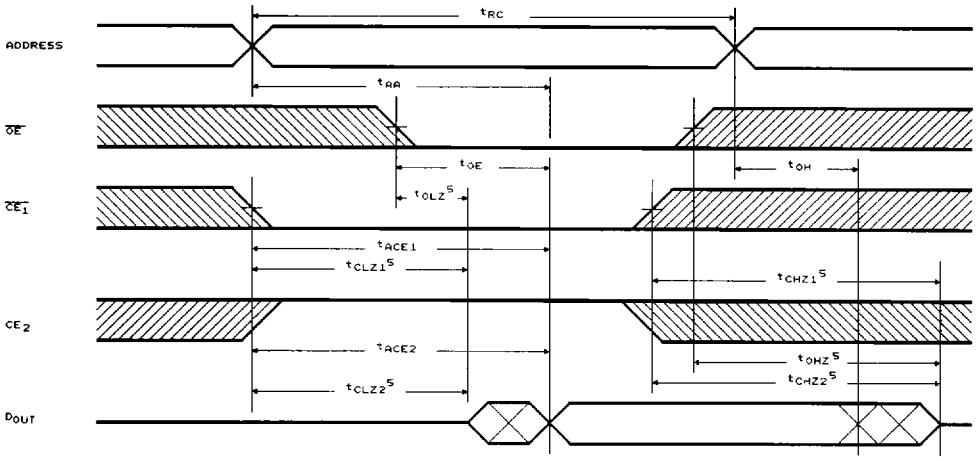


Timing Waveforms (continued)

Read Cycle 3 (1, 4, 7, 8)



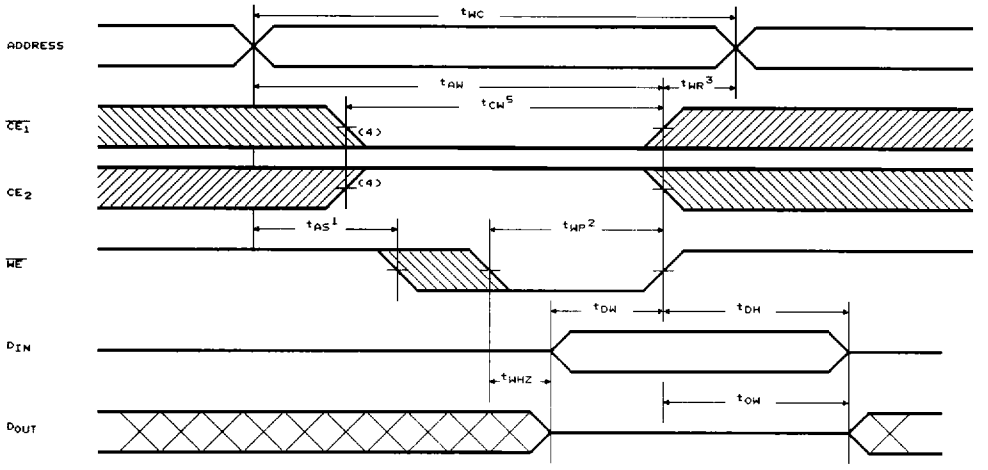
Read Cycle 4 (1)



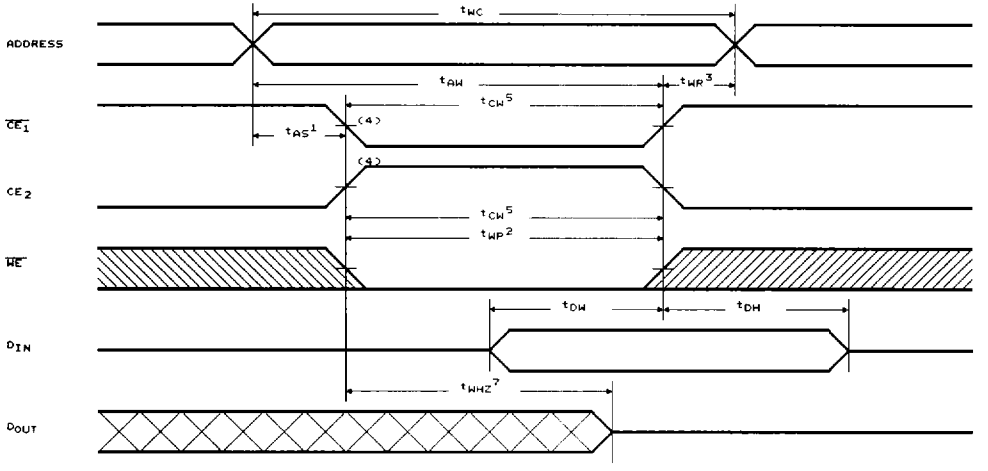
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

Timing Waveforms (continued)

Write Cycle 1 [6]
(Write Enable Controlled)



Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

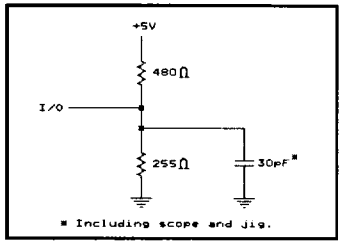


Figure 1. Output Load

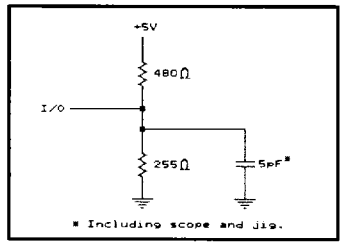
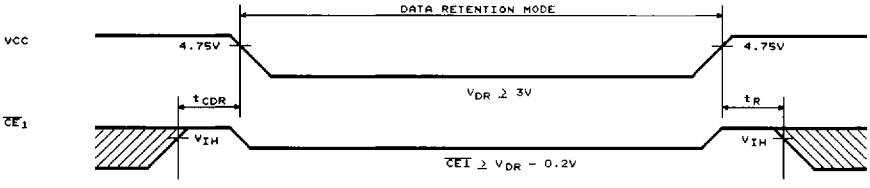


Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{WHZ}, and t_{OW}

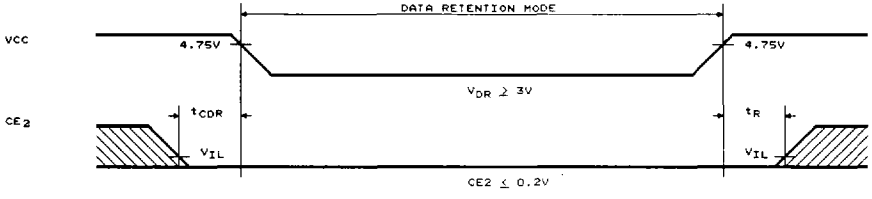
Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention	3	5.25	V	$\overline{CE1}$ ≥ VCC - 0.2V CE2 ≥ VCC - 0.2V or CE2 ≤ 0.2V
V_{DR2}		3	5.25	V	CE2 ≤ 0.2V $\overline{CE1}$ ≥ VCC - 0.2C or $\overline{CE1}$ ≤ 0.2V
I_{CCDR1}	Data Retention Current	–	5	mA	VCC = 3.0V $\overline{CE1}$ ≥ VCC - 0.2V CE2 ≥ VCC - 0.2V V_{IN} ≥ VCC - 0.2V or V_{IN} ≤ 0.2V
I_{CCDR2}		–	5	mA	VCC = 3.0V CE2 ≤ 0.2V $\overline{CE1}$ ≤ 0.2V V_{IN} ≥ VCC - 0.2V or V_{IN} ≤ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	5	–	ms	

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2 Controlled)



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM61M512K-15	15	160	10	32L SKINNY
UM61M512K-20	20	160	10	32L SKINNY