Mainboard Layout

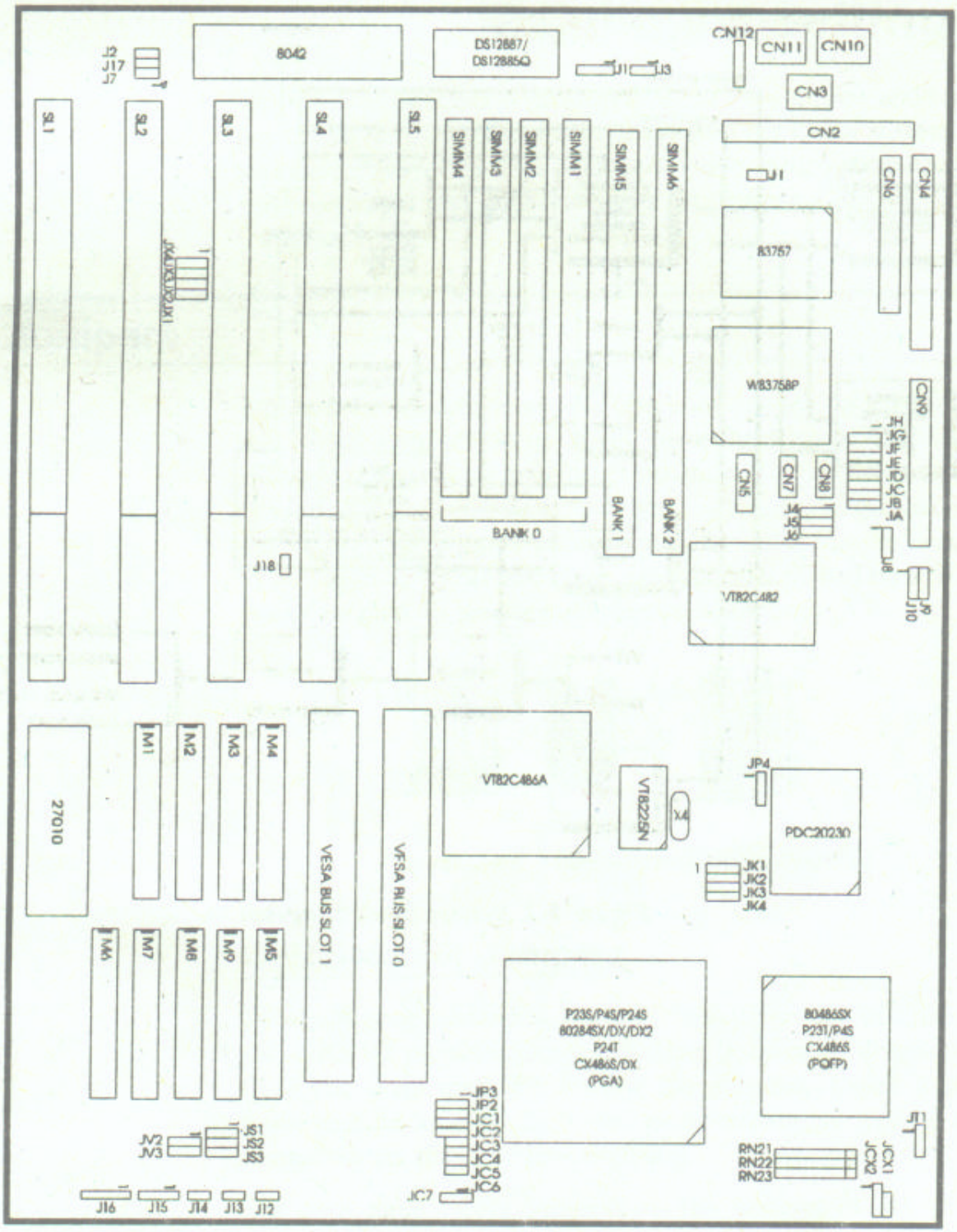


Figure 1-1. Mainboard Layout

Mainboard Settings

The 486-GIO-VT has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

Figure 2 - 1 Jumper with Pins Shorted

CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GIO-VT provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next three tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/P23S (PGA)	P24S/P4S/ 486DX/DX2 (PGA)	P24T (PGA)	CX486S (M6) (PGA)	CX486DX (M7) CX486S+ CX487S (M6+C6) (PGA)
JC1	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC2	2-3 shorted	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted
JC3	open	shorted	open	shorted	shorted
JC4	open	open	shorted	open	open
JC5	shorted	shorted	open	open	open
JC7	1-2 shorted	1-2 shorted	2-3 shorted	1-2 shorted	1-2 shorted

JUMPER (RP 0ohm 10p5R)	P23S/P4S/P24S (PGA)	486DX/DX2/SX (PGA)	CX486S CX486S+CX487S CX486DX (M6, M6+C6, M7) (PGA)	P23S/P4S/CX486S (PQFP)
RN21	empty	empty	empty	inserted
RN22	inserted	empty	empty	empty
RN23	empty	empty	inserted	empty

JUMPER	PIN DEFINITION	
JCX1	Short Open	Cyrix CX486S/DX Intel S-series CPU, others (default)
JCX2	1-2 2-3	Intel S-series CPU, others (default) Cyrix CX486S/DX
JX2, JP2	1-2 * 2-3	IRQ15 (Regular CPUs -- default) -- SMI (Cyrix or Intel S-series CPUs)
JP3	1-2	(factory default)

* IRQ15 is no longer available for the other devices when SMI is selected.

Table 2 - 1 Jumper Settings for CPU Selector

→ **NOTE : Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.**

JUMPER	PIN DEFINITION
J2	Display Type Select Open Mono/EGA/VGA (default) Short Color
J3	External, Internal Battery Select 1-2 External battery 2-3 Internal battery (default)
J4	Local IDE Select 1-2 Enable 2-3 Disable
JP4	Local IDE 1-2 Default 2-3 For VESA Local VGA Card installed at VESA slot 0 only
J5, J6	HDD Speed Select (PDC 20230 Only) IDE Type J5 J6 Speed 0 2-3 2-3 Speed 1 1-2 2-3 (default) Speed 2 1-2 1-2
J7	Password Clear (Award/AMI BIOS Select) Short Clear password Open (default)
J9	HDD_BALE Short Enable Open Disable (default)
J10	HDD_IOCHRDY Short Enable Open Disable (default)
J18	Short Adaptec ISA Master 1542B/C SCSI card only (Transfer rate ≥ 5.7MB/s) Open Default (Transfer rate < 5.7MB/s)
JC6	80486SX/P23S/P4S/CX486S PQFP Select Short Disable Open Enable
JT1	P24T Write-back/Write-through Select 1-2 Write-back 2-3 Write-through
JX1	CPU Clock Select 1-2 1 X (default) 2-3 2 X
JX3, JX4	JX3 JX4 1-2 2-3 Reserved 1-2 1-2 External KBC (default)

Table 2-2. Jumper Definitions

On-board I/O Jumper

JUMPER	FUNCTION	SETTINGS		DESCRIPTION
JA, JB	RS-232-I	JA	JB	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	3E8
		2-3 Short	1-2 Short	3F8 (default)
		2-3 Short	2-3 Short	2E8
JC, JD	RS-232-II	JC	JD	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	2E8
		2-3 Short	1-2 Short	2F8 (default)
		2-3 Short	2-3 Short	3E8
JE, JF	LPT1	JE	JF	
		1-2 Short	1-2 Short	Disable
		1-2 Short	2-3 Short	378 (default)
		2-3 Short	1-2 Short	278
		2-3 Short	2-3 Short	3BC
JG	IDE	2-3 Short		Enable (default)
		1-2 Short		Disable
JH	FDC	2-3 Short		Enable (default)
		1-2 Short		Disable
JI	LPT OE	Short		O/P Port (default)
		Open		Bi-directional

Table 2-3. On-board I/O Jumper Definition

CPU Clock Jumper JK1-JK4 (VT8225N)

CLK 2	JK1	JK2	JK3	JK4
100 MHz	1-2	2-3	1-2	2-3
80 MHz	1-2	1-2	2-3	2-3
66.6 MHz	2-3	2-3	1-2	2-3
50 MHz	2-3	1-2	2-3	2-3
40 MHz	1-2	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
25 MHz	2-3	1-2	2-3	1-2

Table 2-4. CPU Clock Jumper Selection JK1-JK4 (VT8225N)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
J1 External Battery Connector	1 2, 3 4	Anode+ NC Cathode –
J8 HDD_LED Connector	1 2	VCC LED
CN2 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V –12V Ground –5V
CN3 Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data NC Ground +5V
CN4 FDD Connector	2 4, 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33	Density selection NC Index detection Select motor A Select drive A Select drive B Select motor B Direction control Step pulse Write data Write enable Track 0 Write protect Read data Head select Disk change Ground
CN5 Game Port Connector	1, 8, 9, 15 2 3 4, 5, 12 6 7 10 11 13 14 16	VCC D4 D0 Ground D1 D5 D6 D2 D3 D7 Not used

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
CN6 Parallel Port Connector	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18-25	LPT strobe Data bit 0 Data bit 1 Data bit 2 Data bit 3 Data bit 4 Data bit 5 Data bit 6 Data bit 7 LPT acknowledge LPT busy Paper end Selected status Auto line feed LPT error Initiate printer Select printer Ground
CN7, CN8 Serial Port 1, 2 Connector	1 2 3 4 5 6 7 8 9	Data carrier detect Receive data Transmit data Data transmit ready Signal ground Ready to receive data Request to send data Clear to send Ring indicator
CN10 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground +5V Keyboard clock
CN11 PS/2 Mouse Connector	1 2, 6 3 4 5	Mouse data NC Ground +5V Mouse clock
CN12 Mouse Connector	1 2 3 4 5	Mouse data NC Ground +5V Mouse clock
J12 Turbo Switch	1 2	Turbo Signal Ground
J13 Turbo LED	1 2	VCC LED
J14 Hardware Reset	1 2	Ground Reset signal

Table 2-5. Connector Pin Definitions (Continued)

CONNECTOR	PIN OUTS	SIGNAL NAME
J15 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J16 Keylock and Power LED Connector	1 2 3, 5 4	Power signal Spare Ground Keylock
J17 * Green Power Supply Connector	1 2	Enable/Disable power supply outlet Ground
CN9 HDD IDE Connector	1 2, 19, 22, 24, 26, 30, 40 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 20, 21, 29, 34 23 25 27 28 31 32 33 35 36 37 38 39	Reset hard disk Ground HDD7 HDD8 HDD6 HDD9 HDD5 HDD10 HDD4 HDD11 HDD3 HDD12 HDD2 HDD13 HDD1 HDD14 HDD0 HDD15 NC HDD I/O write HDD I/O read IOCHRDY HDD address latch IRQ14 IOCS16 HDD A1 HDD A0 HDD A2 HDD chip select 0 HDD chip select 1 HDD active

* Insert two pin connector wire from Green Power Supply into Connector J17.

Table 2-5. Connector Pin Definitions

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL15 and SL16, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL15) or (SL16).

The following tables give the pin assignments for SL15 and SL16. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV2 and JV3 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV2	CPU Speed Select 1-2 Greater than 33 MHz 2-3 Less than or equal to 33 MHz
JV3	High Speed Write 1-2 One wait write 2-3 Zero wait write (default)

Memory Subsystem

The 486-GIO-VT is equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

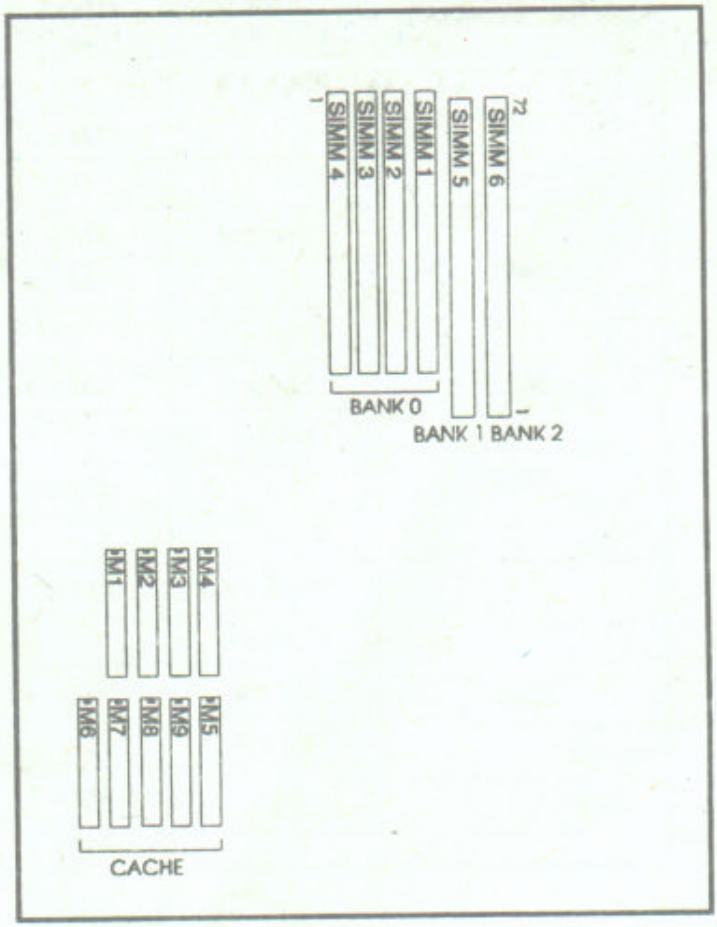


Figure 3-1. Cache and Memory Locations

Installing DRAM

SIMM Banks

The 486-GIO-VT can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256K x 4		
		1M x 1	
			1M x 1
2MB	256K x 4	1M x 1	
		1M x 1	1M x 1
	256K x 4		1M x 1
3MB	256K x 4	1M x 1	1M x 1
4MB	1M x 4		
		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table 3 - 1 DRAM Configurations

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
16MB	4M x 4		
		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
		1M x 1	16M x 1
		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
18MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4		16M x 1
	4M x 4	4M x 1	
	4M x 4		4M x 1
		4M x 1	16M x 1
		16M x 1	4M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
21MB	256K x 4	4M x 1	16M x 1
	256K x 4	16M x 1	4M x 1
	1M x 4	1M x 1	16M x 1
	1M x 4	16M x 1	1M x 1
	4M x 4	1M x 1	4M x 1
	4M x 4	4M x 1	1M x 1
24MB	1M x 4	4M x 1	16M x 1
	1M x 4	16M x 1	4M x 1
	4M x 4	4M x 1	4M x 1
32MB	4M x 4	16M x 1	
	4M x 4		16M x 1
		16M x 1	16M x 1
		32M x 1 *	
			32M x 1 *
33MB	256K x 4	16M x 1	16M x 1
	4M x 4	1M x 1	16M x 1
	4M x 4	16M x 1	1M x 1
36MB	1M x 4	16M x 1	16M x 1
	4M x 4	4M x 1	16M x 1
	4M x 4	16M x 1	4M x 1
48MB	4M x 4	16M x 1	16M x 1
64MB	16M x 4		
		32M x 1 *	32M x 1 *
65MB	16M x 4	1M x 1	
	16M x 4		1M x 1
66MB	16M x 4	1M x 1	1M x 1
68MB	16M x 4	4M x 1	
	16M x 4		4M x 1
69MB	16M x 4	1M x 1	4M x 1
	16M x 4	4M x 1	1M x 1

* Double-RAS SIMM

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
72MB	16M x 4	4M x 1	4M x 1
80MB	16M x 4	16M x 1	
	16M x 4		16M x 1
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

→ **NOTE : When using double-RAS SIMM, it is advised that Bank 2 be used instead of Bank 1. If Bank 1 contains a double-RAS SIMM, then Bank 0 (30-pin) is rendered inoperative.**

Installation Instructions

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.**

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

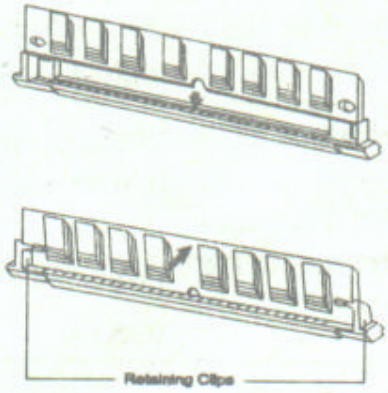


Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-GIO-VT can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**
Alter RAM type is always the same as Tag RAM.

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.

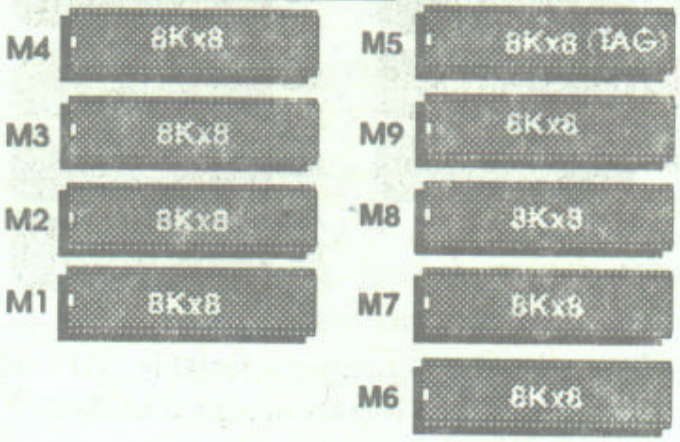
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

5. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

64K Cache SRAM



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Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

5. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

64K Cache SRAM