40P201- NV40 HIGH END BOARD

NV 40 E201_A00 - NV40 Flipchip BGA, 4 x 64MB DDR3 (8 x 8Mx32 = 256MB)
Internal TMDS (dual link) and External TMDS (dual link), Internal TVout,
TV Capture (7114 or 7108), and scalability connector

Table of Contents:

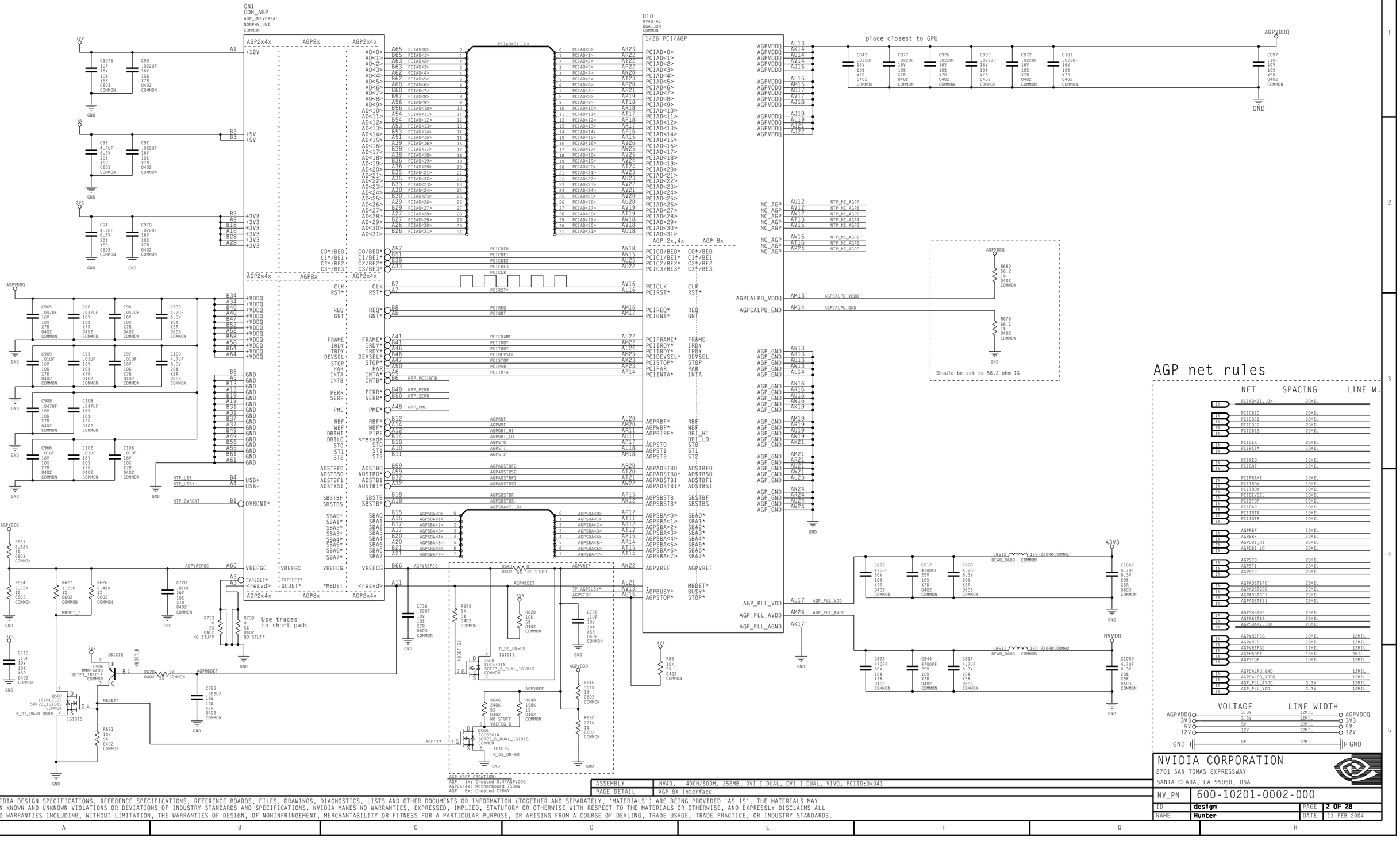
SKU	VARIANT	NVPN	ASSEMBLY
B	BASE	600-10201-base-sch	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
1	000	600-10201-0000-000	NV40-U, 500N/700M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x040
2	001	600-10201-0001-000	NV40, 400N/600M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
3	002	600-10201-0002-000	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
4	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
5	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
6	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
7	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
8	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
9	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
10	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
11	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
12	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
13	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
14	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>
15	<UNDEFINED>	<UNDEFINED>	<UNDEFINED>

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Table of Contents

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	1 OF 28
NAME	Hunter	DATE	11-FEB-2004

2. AGP 8X Interface

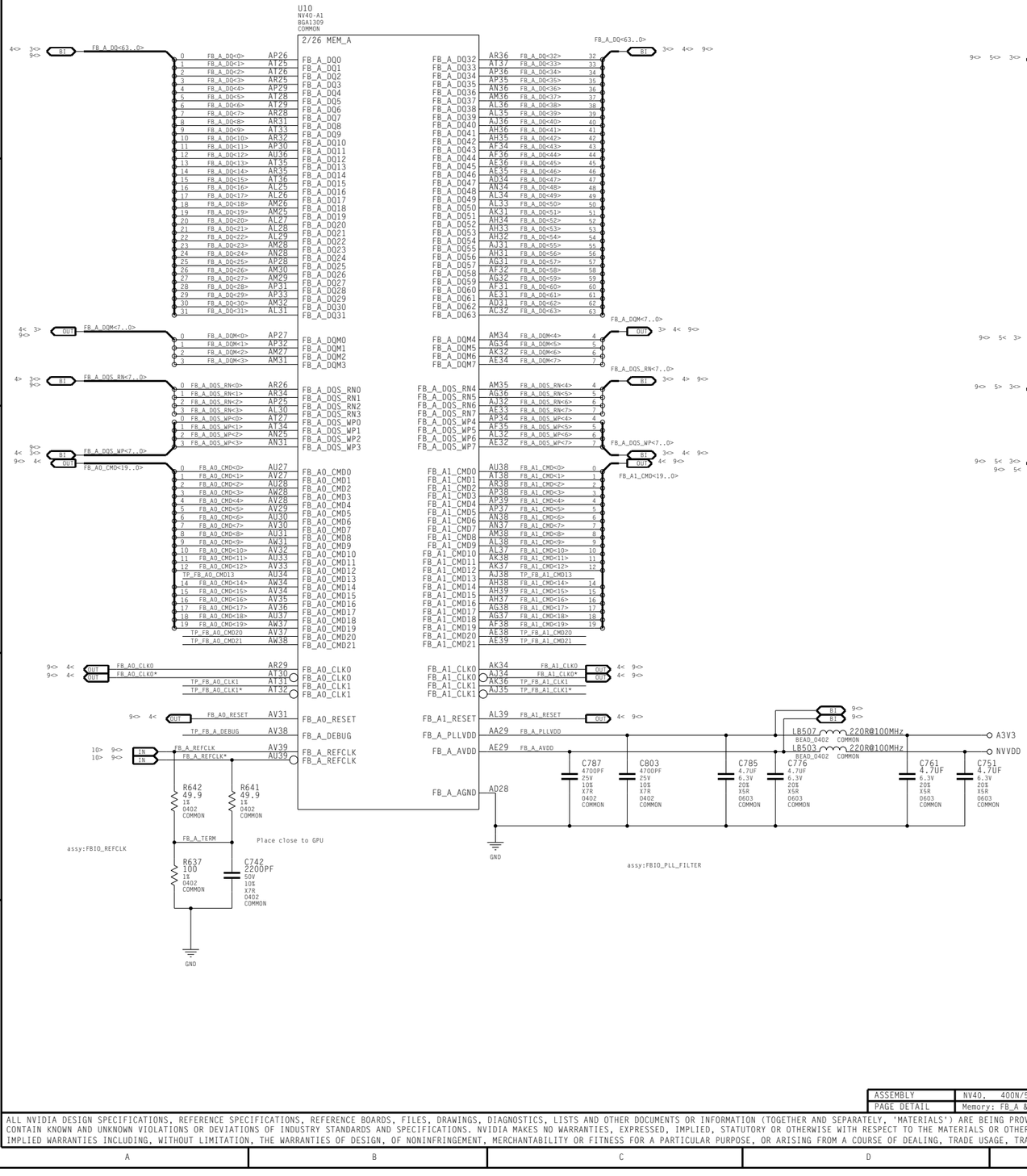


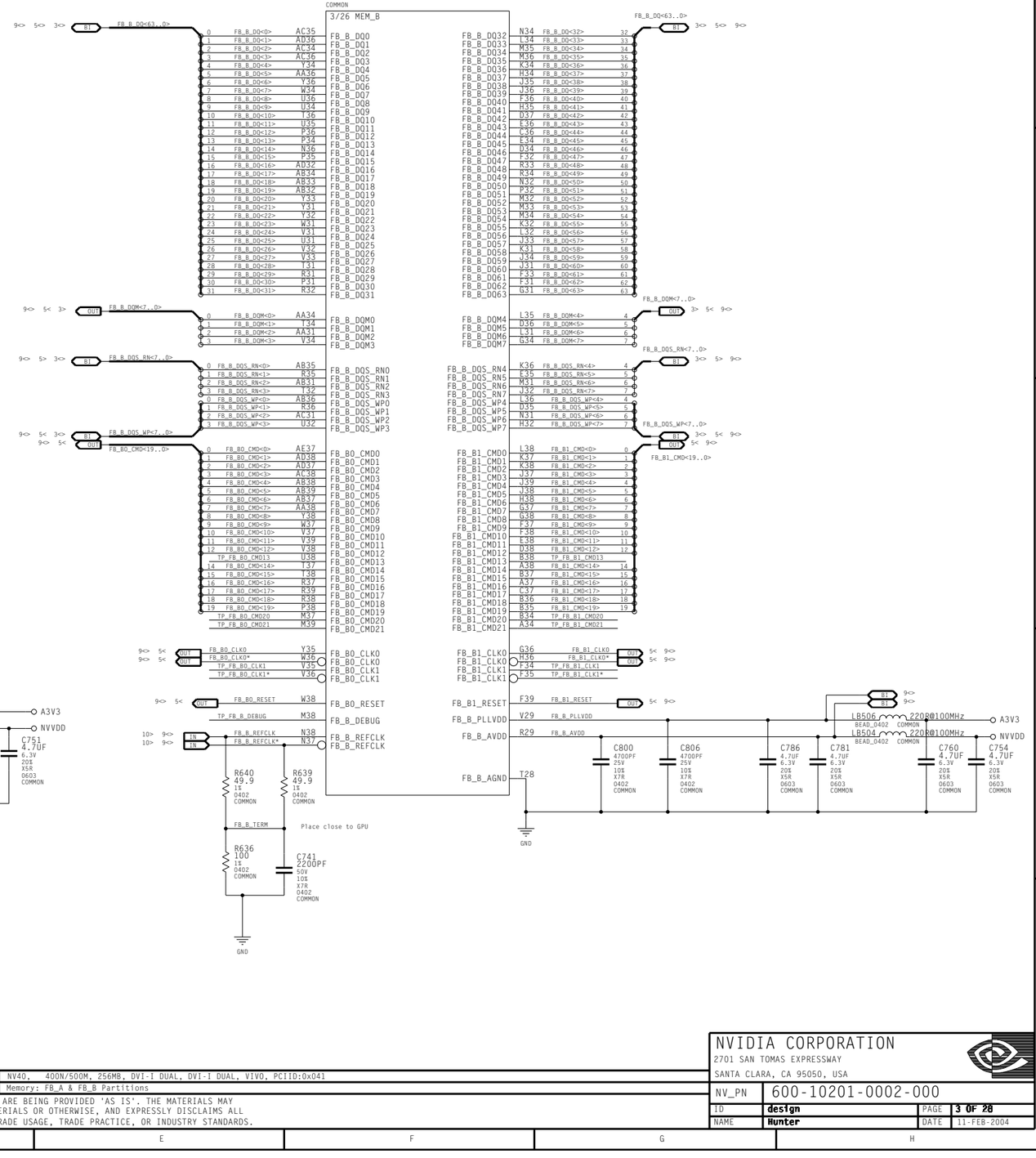
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	AGP 8X Interface

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	2 OF 28
NAME	Hunter	DATE	11-FEB-2004

3.Memory - FB_A & FB_B Partitions





ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_A & FB_B Partitions

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	des1gn	PAGE	3 OF 28
NAME	Hunter	DATE	11-FEB-2004

4. Memory Part. A

ASSY=FBIO_A

	144BGA
	TOP
	CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

termination not required for DDR2

stuff 120 for DDR2
stuff 60 for DDR3

120 for DDR2
240 for DDR3

ASSY=FBIO_VREF_CAP

DDR3 = 0.75 * VDDQ
DDR2 = 0.5 * VDDQ

H4 & H11 NC FOR DDR2

New CAPs.

Replicate to other pages!!

MEMORY BGA

placed TOP

MEMORY BGA

placed TOP

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_A

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	4 OF 28
NAME	Hunter	DATE	11-FEB-2004

5. Memory Part. B

termination not required for DDR2

ASSY=FBIO_B

	144BGA
	TOP
	CSO
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

H4 & H11 NC FOR DDR2

H4 & H11 NC FOR DDR2

New CAPs.

Replicate to other pages!!

MEMORY BGA

placed TOP

MEMORY BGA

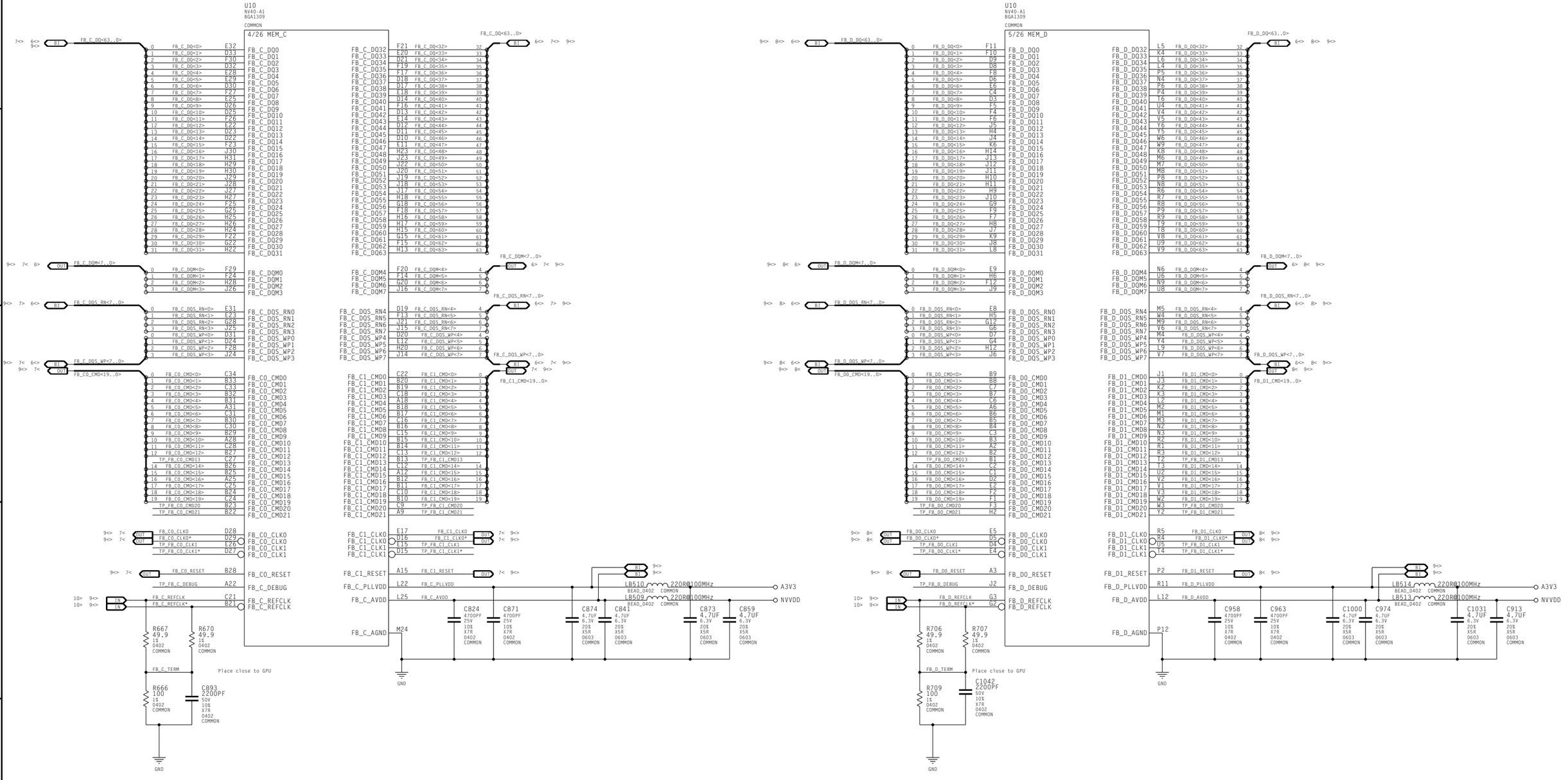
placed TOP

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_B

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	5 OF 28
NAME	Hunter	DATE	11-FEB-2004

6. Memory - FBC & FBD Partitions



ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_C & FB_D Partitions

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	6 OF 28
NAME	Hunter	DATE	11-FEB-2004

7. Memory Part. C

ASSY=FBIO_C

	144BGA
	TOP
	CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

MEMORY BGA
placed TOP

MEMORY BGA
placed TOP

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_C

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	7 OF 28
NAME	Hunter	DATE	11-FEB-2004

8. Memory Part. D

ASSY=FBIO_D

	144BGA
	TOP CS0
CMD0	A4
CMD1	A7
CMD2	A5
CMD3	A6
CMD4	A9
CMD5	A8
CMD6	CS0
CMD7	BA1
CMD8	WE*
CMD9	RAS*
CMD10	CKE
CMD11	CAS*
CMD12	BA0
CMD13	CS1
CMD14	A11
CMD15	A10
CMD16	A1
CMD17	A2
CMD18	A0
CMD19	A3
CMD20	<und>
CMD21	<und>

termination not required for DDR2

U8 / U6 DDR3BGA144 PACK_TYPE=BGA144 VERSION=BGA144 COMMON

H4 & H11 NC FOR DDR2

MEMORY BGA
placed TOP

MEMORY BGA
placed TOP

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory: FB_D

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	8 OF 28
NAME	Hunter	DATE	11-FEB-2004

9. Memory NET SPACING RULES, FB CAL & VREF

Memory FBA FBB

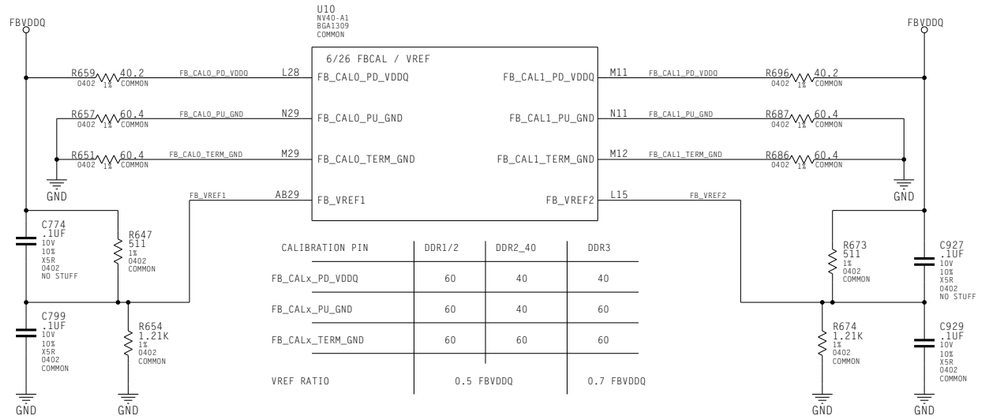
		NET Name	Diffpair	Spacing	
4<	3>	FB_A0_CLK0	FBA0CLK0	80_OHM_DIFF	
4<	3>	FB_A0_CLK0*	FBA0CLK0	80_OHM_DIFF	
4<	3>	FB_A1_CLK0	FBA1CLK0	80_OHM_DIFF	
4<	3>	FB_A1_CLK0*	FBA1CLK0	80_OHM_DIFF	
5<	3>	FB_B0_CLK0	FBB0CLK0	80_OHM_DIFF	
5<	3>	FB_B0_CLK0*	FBB0CLK0	80_OHM_DIFF	
5<	3>	FB_B1_CLK0	FBB1CLK0	80_OHM_DIFF	
5<	3>	FB_B1_CLK0*	FBB1CLK0	80_OHM_DIFF	
10>	3<	FB_A_REFCLK	FBAREFCLK		100 ohm diff
10>	3<	FB_A_REFCLK*	FBAREFCLK		
10>	3<	FB_B_REFCLK	FBBREFCLK		
10>	3<	FB_B_REFCLK*	FBBREFCLK		100 ohm diff
4<>	3<>	FB_A_DQ<63..0>		10MIL	
5<>	3<>	FB_B_DQ<63..0>		10MIL	
4<	3>	FB_A_DQM<7..0>		10MIL	
4>	3<>	FB_A_DQS_RN<7..0>		10MIL	
4<	3<>	FB_A_DQS_WP<7..0>		10MIL	
5<	3>	FB_B_DQM<7..0>		10MIL	
5>	3<>	FB_B_DQS_RN<7..0>		10MIL	
5<	3<>	FB_B_DQS_WP<7..0>		10MIL	
4<	3>	FB_A0_CMD<19..0>		15MIL	
4<	3>	FB_A1_CMD<19..0>		15MIL	
5<	3>	FB_B0_CMD<19..0>		15MIL	
5<	3>	FB_B1_CMD<19..0>		15MIL	
4<	3>	FB_A0_RESET		10MIL	
4<	3>	FB_A1_RESET		10MIL	
5<	3>	FB_B0_RESET		10MIL	
5<	3>	FB_B1_RESET		10MIL	

		NET Name	MIN_LINE_WIDTH	VOLTAGE
3<>		FB_A_AVDD	12MIL	3.3V
3<>		FB_A_PLLVDD	12MIL	3.3V
3<>		FB_B_AVDD	12MIL	3.3V
3<>		FB_B_PLLVDD	12MIL	3.3V
4<>		FB_A0_ZQ	12MIL	0.9V
4<>		FB_A1_ZQ	12MIL	0.9V
5<>		FB_B0_ZQ	12MIL	0.9V
5<>		FB_B1_ZQ	12MIL	0.9V
4<>		FB_A0_VREF1	12MIL	0.9V
4<>		FB_A0_VREF2	12MIL	0.9V
4<>		FB_A1_VREF1	12MIL	0.9V
4<>		FB_A1_VREF2	12MIL	0.9V
5<>		FB_B0_VREF1	12MIL	0.9V
5<>		FB_B0_VREF2	12MIL	0.9V
5<>		FB_B1_VREF1	12MIL	0.9V
5<>		FB_B1_VREF2	12MIL	0.9V

Memory FBC FBD

		NET Name	Diffpair	Spacing	
7<	6>	FB_C0_CLK0	FBC0CLK0	80_OHM_DIFF	
7<	6>	FB_C0_CLK0*	FBC0CLK0	80_OHM_DIFF	
7<	6>	FB_C1_CLK0	FBC1CLK0	80_OHM_DIFF	
7<	6>	FB_C1_CLK0*	FBC1CLK0	80_OHM_DIFF	
8<	6>	FB_D0_CLK0	FBD0CLK0	80_OHM_DIFF	
8<	6>	FB_D0_CLK0*	FBD0CLK0	80_OHM_DIFF	
8<	6>	FB_D1_CLK0	FBD1CLK0	80_OHM_DIFF	
8<	6>	FB_D1_CLK0*	FBD1CLK0	80_OHM_DIFF	
10>	6<	FB_C_REFCLK	FBCREFCLK		
10>	6<	FB_C_REFCLK*	FBCREFCLK		100 ohm diff
10>	6<	FB_D_REFCLK	FBDREFCLK		
10>	6<	FB_D_REFCLK*	FBDREFCLK		100 ohm diff
7<>	6<>	FB_C_DQ<63..0>		10MIL	
8<>	6<>	FB_D_DQ<63..0>		10MIL	
7<	6>	FB_C_DQM<7..0>		10MIL	
7>	6<>	FB_C_DQS_RN<7..0>		10MIL	
7<	6<>	FB_C_DQS_WP<7..0>		10MIL	
8<	6>	FB_D_DQM<7..0>		10MIL	
8>	6<>	FB_D_DQS_RN<7..0>		10MIL	
8<	6<>	FB_D_DQS_WP<7..0>		10MIL	
7<	6>	FB_C0_CMD<19..0>		15MIL	
7<	6>	FB_C1_CMD<19..0>		15MIL	
8<	6>	FB_D0_CMD<19..0>		15MIL	
8<	6>	FB_D1_CMD<19..0>		15MIL	
7<	6>	FB_C0_RESET		10MIL	
7<	6>	FB_C1_RESET		10MIL	
8<	6>	FB_D0_RESET		10MIL	
8<	6>	FB_D1_RESET		10MIL	

		NET Name	MIN_LINE_WIDTH	VOLTAGE
6<>		FB_C_AVDD	12MIL	3.3V
6<>		FB_C_PLLVDD	12MIL	3.3V
6<>		FB_D_AVDD	12MIL	3.3V
6<>		FB_D_PLLVDD	12MIL	3.3V
7<>		FB_C0_ZQ	12MIL	0.9V
7<>		FB_C1_ZQ	12MIL	0.9V
8<>		FB_D0_ZQ	12MIL	0.9V
8<>		FB_D1_ZQ	12MIL	0.9V
7<>		FB_C0_VREF1	12MIL	0.9V
7<>		FB_C0_VREF2	12MIL	0.9V
7<>		FB_C1_VREF1	12MIL	0.9V
7<>		FB_C1_VREF2	12MIL	0.9V
8<>		FB_D0_VREF1	12MIL	0.9V
8<>		FB_D0_VREF2	12MIL	0.9V
8<>		FB_D1_VREF1	12MIL	0.9V
8<>		FB_D1_VREF2	12MIL	0.9V



DEFAULT BASE SCHEMATICS ARE SETUP FOR DDR3

		NET Name	Spacing
		FB_CALO_PD_VDDQ	20MIL_G2G_30MIL
		FB_CALO_PU_GND	20MIL_G2G_30MIL
		FB_CALO_TERM_GND	20MIL_G2G_30MIL
		FB_CAL1_PD_VDDQ	20MIL_G2G_30MIL
		FB_CAL1_PU_GND	20MIL_G2G_30MIL
		FB_CAL1_TERM_GND	20MIL_G2G_30MIL

		NET Name	MIN_LINE_WIDTH	VOLTAGE
		FB_VREF1	12MIL	3.3V
		FB_VREF2	12MIL	3.3V

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Memory Signal Constraints, FB_CAL

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	9 OF 28
NAME	Hunter	DATE	11-FEB-2004

10. EXTERNAL FBIO REFCLK

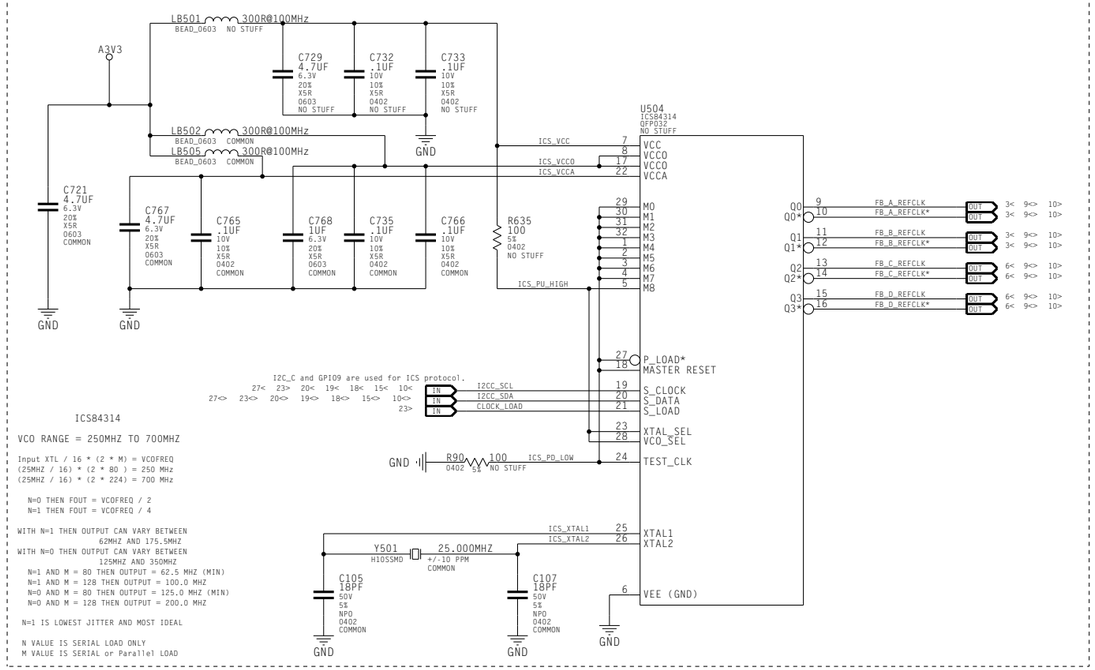
NET RULES

NET	SPACING	LINE WIDTH
ICS_XTAL1	15MIL	10MIL
ICS_XTAL2	15MIL	10MIL

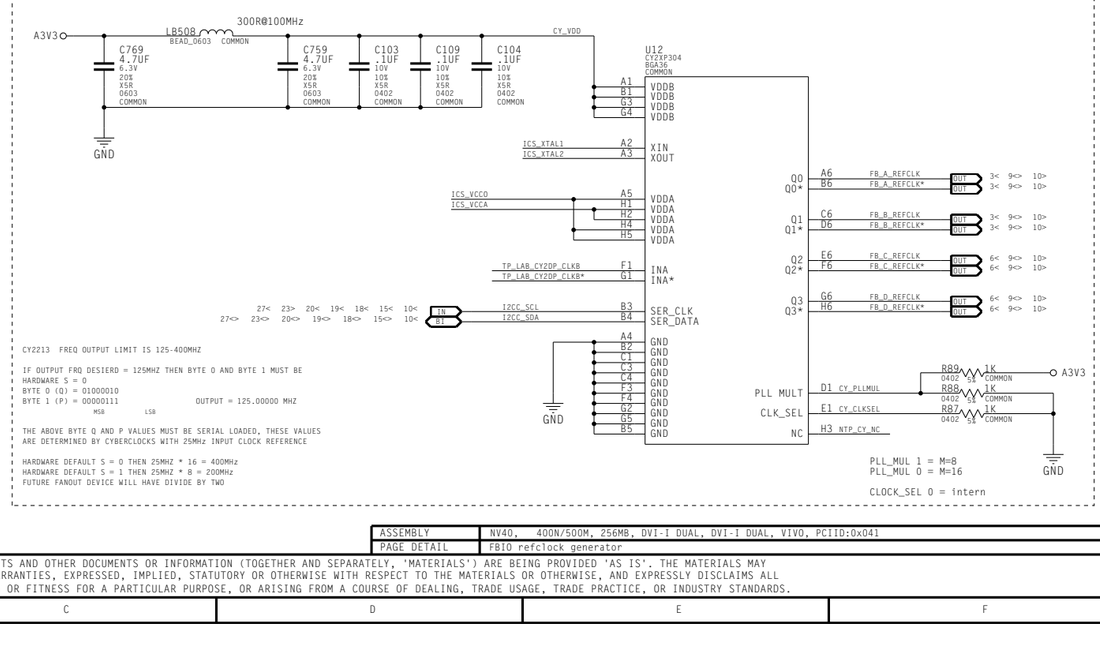
VOLTAGE

ICS_VCC	3.3	10MIL
ICS_VCCO	3.3	10MIL
ICS_VCCA	3.3	10MIL
CY_VDD	3.3	10MIL

EXTERNAL REFCLOCK GENERATOR FOR FBIO ICS SOLUTION.



EXTERNAL REFCLOCK GENERATOR FOR FBIO CYPRESS SOLUTION.



ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	FBIO refclock generator

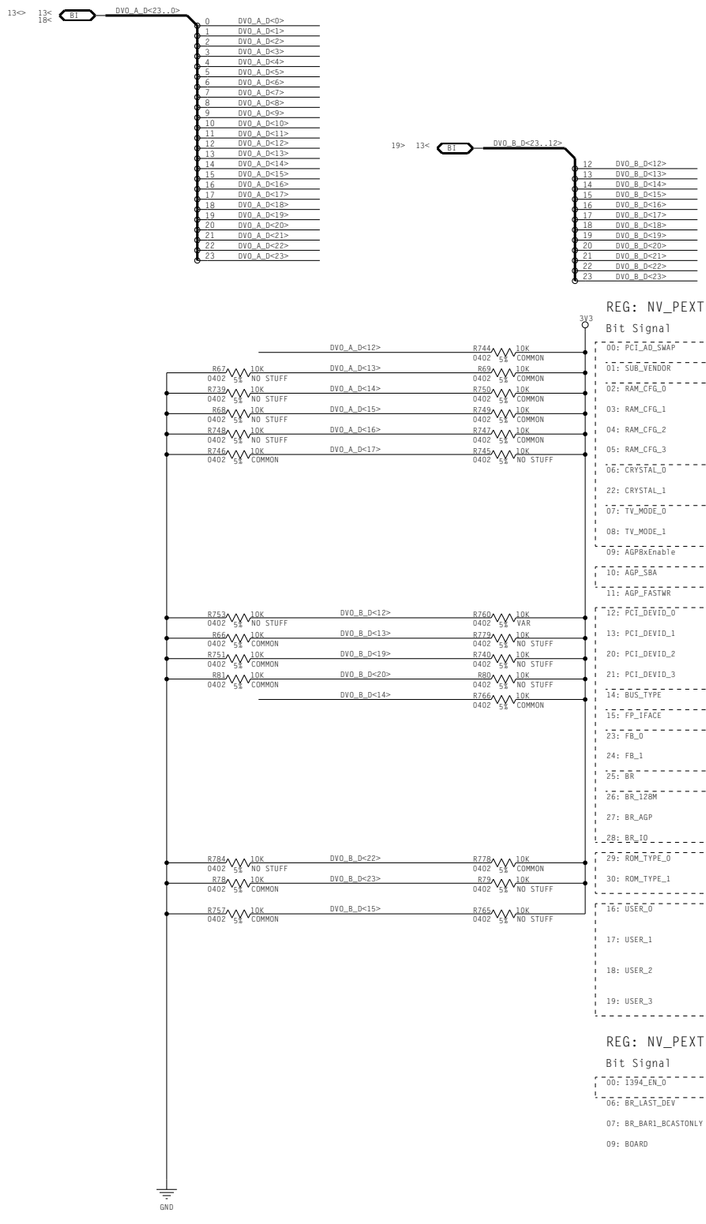
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	10 OF 28
NAME	Hunter	DATE	11-FEB-2004

11. BIOS, Straps, JTAG, PLL Filters

Straps

Assembly: BIOS



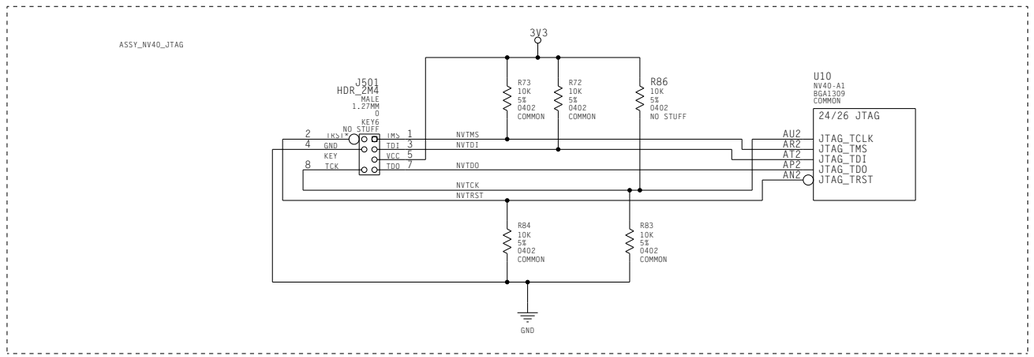
REG: NV_PEXTDEV_BOOT_0

Bit	Signal	VALUE_ID	VALUEs	
00:	PCI_AD_SWAP	PCI_AD_SWAP	0 REVERSED 1 NORMAL	
01:	SUB_VENDOR	SUB_VENDOR	0 NO_BIOS 1 read_from_BIOS	
02:	RAM_CFG_0	RAM_CFG[3:0]	0000 RFU	1000 RFU
03:	RAM_CFG_1		0001 RFU 0010 RFU	1001 RFU 1010 RFU
04:	RAM_CFG_2		0011 RFU 0100 RFU	1011 RFU 1100 RFU
05:	RAM_CFG_3		0101 RFU 0110 RFU 0111 SMX32_GDDR3	1101 RFU 1110 RFU 1111 RFU
06:	CRYSTAL_0	CRYSTAL[1:0]	00 13.500 Mhz 01 14.31818 Mhz	
22:	CRYSTAL_1		10 27.000 Mhz 11 unknown	
07:	TV_MODE_0	TV_MODE[1:0]	00 SECAM 01 NTSC	
08:	TV_MODE_1		10 PAL 11 CRT	
09:	AGPBxEnable	AGP_30_Bx	0 AGPBx enabled 1 AGPBx disabled	
10:	AGP_SBA	AGP_SBA[0]	0 SBA enabled 1 SBA disabled	
11:	AGP_FASTWR	AGP_FASTWR[0]	0 enabled 1 disabled	
12:	PCI_DEVID_0	PCI_DEVID[3:0]	0000 0x400 ... 1111 0x40F	
13:	PCI_DEVID_1		0000 (0x400) 0001 (0x401)	
20:	PCI_DEVID_2		1110 (0x40E)	
21:	PCI_DEVID_3			
14:	BUS_TYPE	BUS_TYPE[0]	0 PCI 1 AGP	
15:	FP_IFACE	FP_IFACE[0]	0 24Bit 1 12Bit	
23:	FB_0	FB[1:0]	00 64M 01 128M	
24:	FB_1		10 256M 11 512M	
25:	BR	BR[0]	0 BRIDGE disabled 1 BRIDGE enabled	
26:	BR_128M	BR bits are ignored if BRIDGE is disabled		
27:	BR_AGP			
28:	BR_IO			
29:	ROM_TYPE_0	ROM_TYPE[1:0]	00 Parallel 01 Serial_AT25F	
30:	ROM_TYPE_1		10 Serial_SST45VF 11 RFU	
16:	USER_0	STRAP_USER[3:0]	0000 (default)	
17:	USER_1			
18:	USER_2			
19:	USER_3			

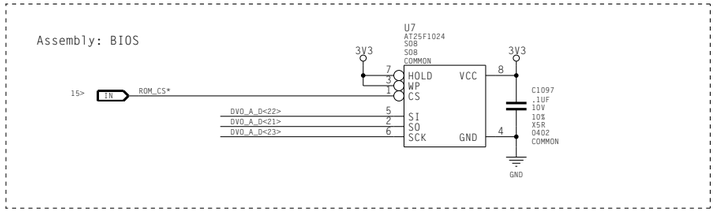
REG: NV_PEXTDEV_BOOT_3

Bit	Signal	VALUE_ID	VALUEs
00:	1394_EN_0	1394[0]	0 1394 disabled 1 1394 enabled
06:	BR_LAST_DEV		
07:	BR_BAR1_BCASTONLY		
09:	BOARD		

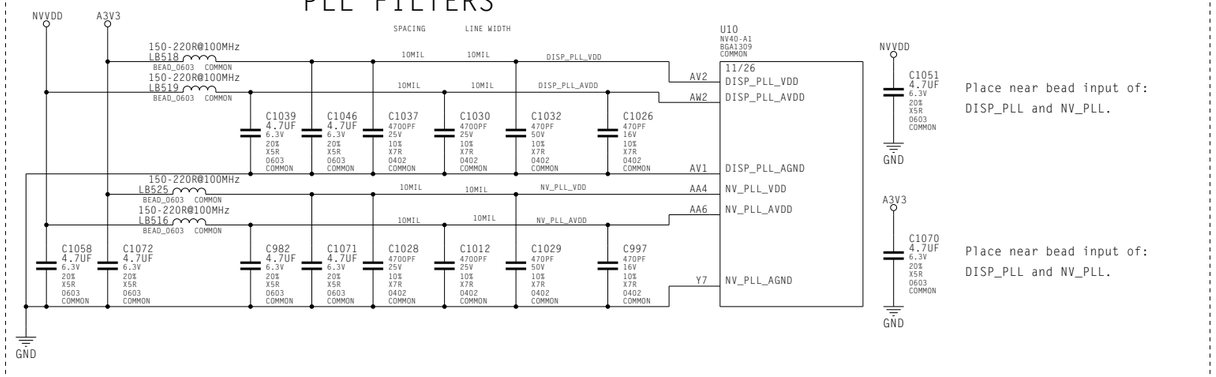
JTAG



BIOS (serial)



PLL FILTERS



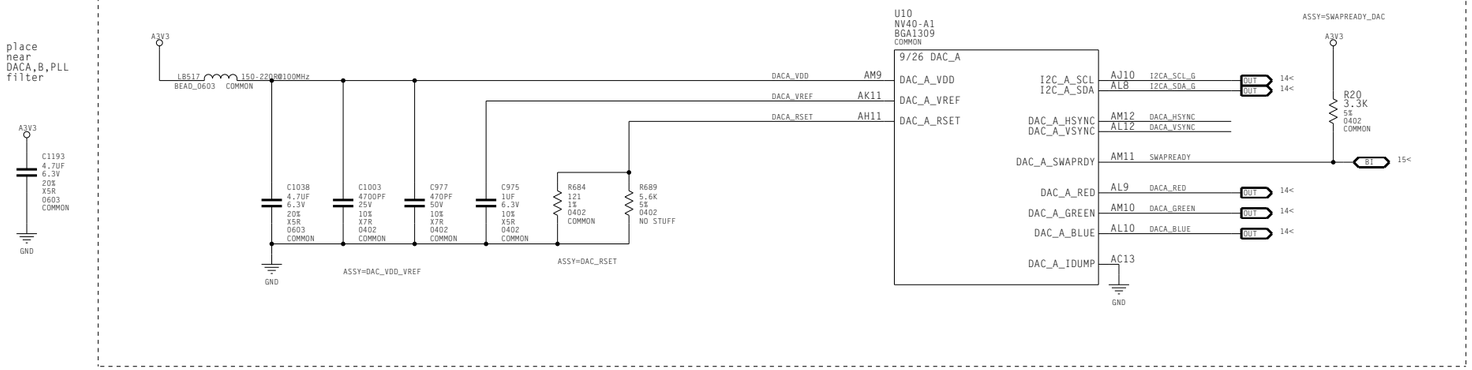
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	BIOS, Strappings, JTAG, and PLL FILTERS

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

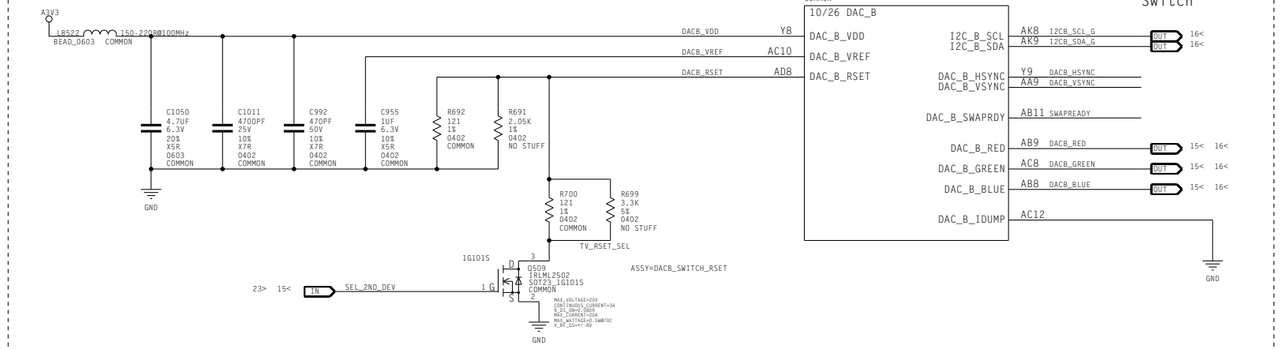
NV_PN	600-10201-0002-000		
ID	design	PAGE	11 OF 28
NAME	Hunter	DATE	11-FEB-2004

12. DAC_A, DAC_B, PLL, SyncBuffer

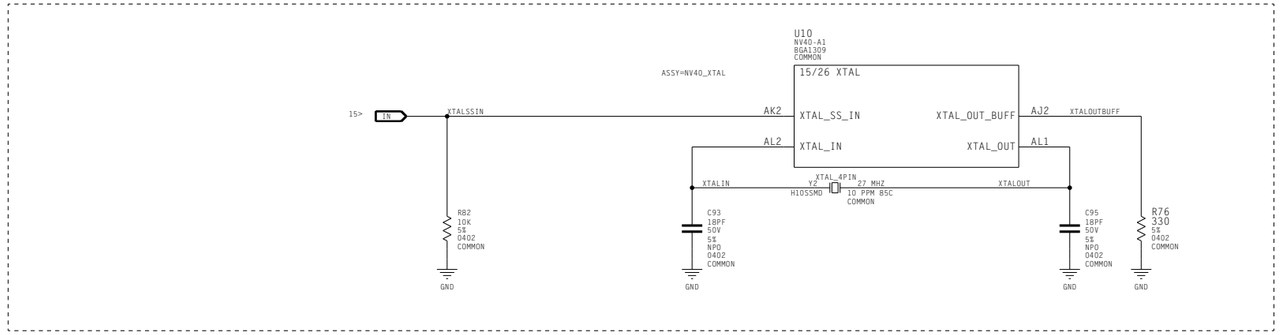
DACA



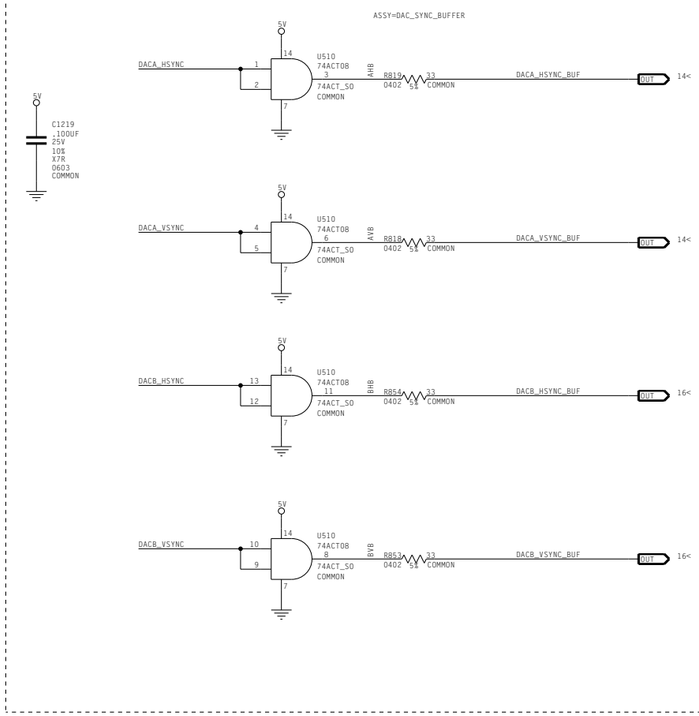
DACB



XTAL/PLLVDD



DAC Sync Buffer



NET RULES

	NET	SPACING	LINE WIDTH
IN	XTALIN	15MIL	5MIL
IN	XTALOUT	15MIL	5MIL
IN	DACB_VDD		16MIL
IN	DACB_RSET		16MIL
IN	DACB_VREF		16MIL
IN	DACA_VDD		16MIL
IN	DACA_RSET		16MIL
IN	DACA_VREF		16MIL

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DAC_A, DAC_B, PLL and SYNCbuffer

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	12 OF 28
NAME	Hunter	DATE	11-FEB-2004

13. DVO/VIP Interface

NET RULES

	NET	LINE WIDTH	SPACING
IN	DVO_A_CALPD_VDDQ	12MIL	20MIL
IN	DVO_A_CALPU_GND	12MIL	20MIL
IN	DVO_A_VDDQ	16MIL	
IN	DVO_B_CALPD_VDDQ	12MIL	20MIL
IN	DVO_B_CALPU_GND	12MIL	20MIL
IN	DVO_B_VDDQ	16MIL	
IN	DVO_A_D<23..0>		10MIL
IN	DVO_A_CLKOUT		15MIL
IN	DVO_A_CLKOUT*		15MIL
IN	DVO_B_D<23..12>		10MIL

18< 13> 11<>
18< 13>
18< 13>
19> 13< 11<>

Si1178 supports either 3.3V or 1.0V-1.8V signaling

ASSY=DVO_A_NV40

A3V3
LB515 150-220R@100MHZ COMMON BEAD_0603
C1010 4.7UF 6.3V 20% X5R 0603 COMMON
C972 .1UF 10V 10% X5R 0402 COMMON
C973 100PF 50V 5% C0G 0402 COMMON
C1006 1000PF 16V 10% X7R 0402 COMMON
GND
PLACE CLOSE TO NV40

DVO_A_VDDQ
R697 1K 1% 0402 COMMON
R701 1K 1% 0402 COMMON
C1015 .1UF 10V 10% X5R 0402 COMMON
GND
DVO_A_VREF

R695 49.9 1% 0402 COMMON
DVO_A_CALPD_VDDQ
R694 49.9 1% 0402 COMMON
DVO_A_CALPU_GND
GND

A3V3
C64 4.7UF 6.3V 20% X5R 0603 COMMON
GND

U10
NV40-A1
BGA1309
COMMON

13/26 DVO

AP10	DVO_A_VDDQ		
AR10	DVO_A_VDDQ		
AP11	DVO_A_VDDQ		
AT5	DVO_A_VREF		
AT8	DVO_A_CAL_PD_VDDQ		
AT9	DVO_A_CAL_PU_GND		
AV4	DVO_A_D0	DVO_A_D<0>	0
AU5	DVO_A_D1	DVO_A_D<1>	1
AV5	DVO_A_D2	DVO_A_D<2>	2
AU6	DVO_A_D3	DVO_A_D<3>	3
AV6	DVO_A_D4	DVO_A_D<4>	4
AW6	DVO_A_D5	DVO_A_D<5>	5
AU8	DVO_A_D6	DVO_A_D<6>	6
AV8	DVO_A_D7	DVO_A_D<7>	7
AU9	DVO_A_D8	DVO_A_D<8>	8
AV9	DVO_A_D9	DVO_A_D<9>	9
AW9	DVO_A_D10	DVO_A_D<10>	10
AT10	DVO_A_D11	DVO_A_D<11>	11
AR9	DVO_A_D12	DVO_A_D<12>	12
AR8	DVO_A_D13	DVO_A_D<13>	13
AP9	DVO_A_D14	DVO_A_D<14>	14
AR6	DVO_A_D15	DVO_A_D<15>	15
AT6	DVO_A_D16	DVO_A_D<16>	16
AU3	DVO_A_D17	DVO_A_D<17>	17
AR5	DVO_A_D18	DVO_A_D<18>	18
AP8	DVO_A_D19	DVO_A_D<19>	19
AP5	DVO_A_D20	DVO_A_D<20>	20
AM8	DVO_A_D21	DVO_A_D<21>	21
AN9	DVO_A_D22	DVO_A_D<22>	22
AN4	DVO_A_D23	DVO_A_D<23>	23
AV10	DVO_A_DE_CLKIN	DVO_A_DE	OUT 18<
AT7	DVO_A_CLKOUT	DVO_A_CLKOUT	OUT 13< 18<
AV7	DVO_A_CLKOUT	DVO_A_CLKOUT*	OUT 13< 18<
AW3	DVO_A_HSYNC	DVO_A_HSYNC	OUT 18<
AV3	DVO_A_VSYNC	DVO_A_VSYNC	OUT 18<
AV11	DVO_A_CTL3	DVO_A_CTL3	OUT 18<

DUAL TMDS
DVO_A_D<23..0> → #1 11<> 13< 18<

ASSY=DVO_B_NV40

A3V3
LB521 150-220R@100MHZ COMMON BEAD_0603
C1061 4.7UF 6.3V 20% X5R 0603 COMMON
C1018 .1UF 10V 10% X5R 0402 COMMON
C980 100PF 50V 5% C0G 0402 COMMON
C1004 1000PF 16V 10% X7R 0402 COMMON
GND
PLACE CLOSE TO NV40

DVO_B_VDDQ
R681 1K 1% 0402 COMMON
R677 1K 1% 0402 COMMON
C937 .1UF 10V 10% X5R 0402 COMMON
GND
DVO_B_VREF

R679 49.9 1% 0402 COMMON
DVO_B_CALPD_VDDQ
R675 49.9 1% 0402 COMMON
DVO_B_CALPU_GND
GND

U10
NV40-A1
BGA1309
COMMON

14/26 DVO

AE6	DVO_B_VDDQ		
AE7	DVO_B_VDDQ		
AE8	DVO_B_VDDQ		
AG14	DVO_B_VREF		
AD13	DVO_B_CAL_PD_VDDQ		
AF13	DVO_B_CAL_PU_GND		
AB2	DVO_B_D0	NTP_DVO_B_D0	
AB3	DVO_B_D1	NTP_DVO_B_D1	
AC2	DVO_B_D2	NTP_DVO_B_D2	
AC3	DVO_B_D3	NTP_DVO_B_D3	
AD2	DVO_B_D4	NTP_DVO_B_D4	
AD4	DVO_B_D5	NTP_DVO_B_D5	
AE3	DVO_B_D6	NTP_DVO_B_D6	
AF2	DVO_B_D7	NTP_DVO_B_D7	
AF3	DVO_B_D8	NTP_DVO_B_D8	
AG2	DVO_B_D9	NTP_DVO_B_D9	
AG4	DVO_B_D10	NTP_DVO_B_D10	
AH1	DVO_B_D11	NTP_DVO_B_D11	
AF4	DVO_B_D12	DVO_B_D<12>	12
AE4	DVO_B_D13	DVO_B_D<13>	13
AE5	DVO_B_D14	DVO_B_D<14>	14
AF6	DVO_B_D15	DVO_B_D<15>	15
AD6	DVO_B_D16	DVO_B_D<16>	16
AC5	DVO_B_D17	DVO_B_D<17>	17
AC6	DVO_B_D18	DVO_B_D<18>	18
AB6	DVO_B_D19	DVO_B_D<19>	19
AC4	DVO_B_D20	DVO_B_D<20>	20
AB4	DVO_B_D21	NTP_DVO_B_D21	
AB5	DVO_B_D22	DVO_B_D<22>	22
AB7	DVO_B_D23	DVO_B_D<23>	23
AH2	DVO_B_DE_CLKIN	DVO_B_CLKIN	IN 15>
AE1	DVO_B_CLKOUT	NTP_DVO_B_CLKOUT	
AE2	DVO_B_CLKOUT	NTP_DVO_B_CLOCKOUT*	
AB1	DVO_B_HSYNC	NTP_DVO_B_HSYNC	
AA2	DVO_B_VSYNC	NTP_DVO_B_VSYNC	
AJ3	DVO_B_CTL3	NTP_DVO8_CTL3	

VIP
VIP CLOCK
DVO_B_D<23..12> → IN 11<> 13< 19>

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DVO/VIP Interface
NV_PN	600-10201-0002-000
ID	design
PAGE	13 OF 28
NAME	Hunter
DATE	11-FEB-2004

14. DACA RGB filters, VGA connector Output (south)

NET RULES

	NET	LINE W.	IMPEDANCE	SPACING
14< 12> IN	DACA_RED		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
14< 12> IN	DACA_GREEN		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
14< 12> IN	DACA_BLUE		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
IN	DACA_R_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
IN	DACA_G_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
IN	DACA_B_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17< 14> IN	DACA_RED_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17< 14> IN	DACA_GREEN_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17< 14> IN	DACA_BLUE_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL

DACA RGB-FILTER

12> IN I2CA_SDA_G — RB809 33 0402 5% COMMON — I2CA_SDA — LB533 150-220R@100MHZ BEAD_0603 COMMON — I2CA_SDA_C — BI 17<

12> IN I2CA_SCL_G — RB808 33 0402 5% COMMON — I2CA_SCL — LB534 150-220R@100MHZ BEAD_0603 COMMON — I2CA_SCL_C — OUT 17<

ASSY=DACA

12> IN DACA_VSYNC_BUF — L3 68nH 0603 COMMON — DACA_VSYNC_C — OUT 17<

12> IN DACA_HSYNC_BUF — L4 68nH 0603 COMMON — DACA_HSYNC_C — OUT 17<

Place 0ohm Resistor Incident with Common Mode Choke

14< 12> IN DACA_RED — L503 27nH 0603 COMMON — DACA_R_F — R841 0 0402 5% NO STUFF — L512 cmf1tr4_2012 360R@100mhz COMMON WIRE_WOUND — DACA_RED_C — OUT 14< 17<

14< 12> IN DACA_GREEN — L502 27nH 0603 COMMON — DACA_G_F — R837 0 0402 5% NO STUFF — L511 cmf1tr4_2012 360R@100mhz COMMON WIRE_WOUND — DACA_GREEN_C — OUT 14< 17<

14< 12> IN DACA_BLUE — L506 27nH 0603 COMMON — DACA_B_F — R843 0 0402 5% NO STUFF — L515 cmf1tr4_2012 360R@100mhz COMMON WIRE_WOUND — DACA_BLUE_C — OUT 14< 17<

DACA_RGB_GND — BI 17<

ASSY=DACA_FILTER

DACA VGA connector

ASSY=DACA_DB15

J2 CON_DSUB15HD VGA_SLIM_DVIMTG VGA_SLIM_DVIMTG NO STUFF

6 GND-R		
1 R		IDO 11 NTP_A_MON_IDO
7 GND-G		
2 G		SDA 12
8 GND_B		
3 B		HSYNC 13
DDC_5V — NTP_A_MONID2	9 5V	VSYNC 14
4 ID2		
10 GND		
5 GND		SCL 15

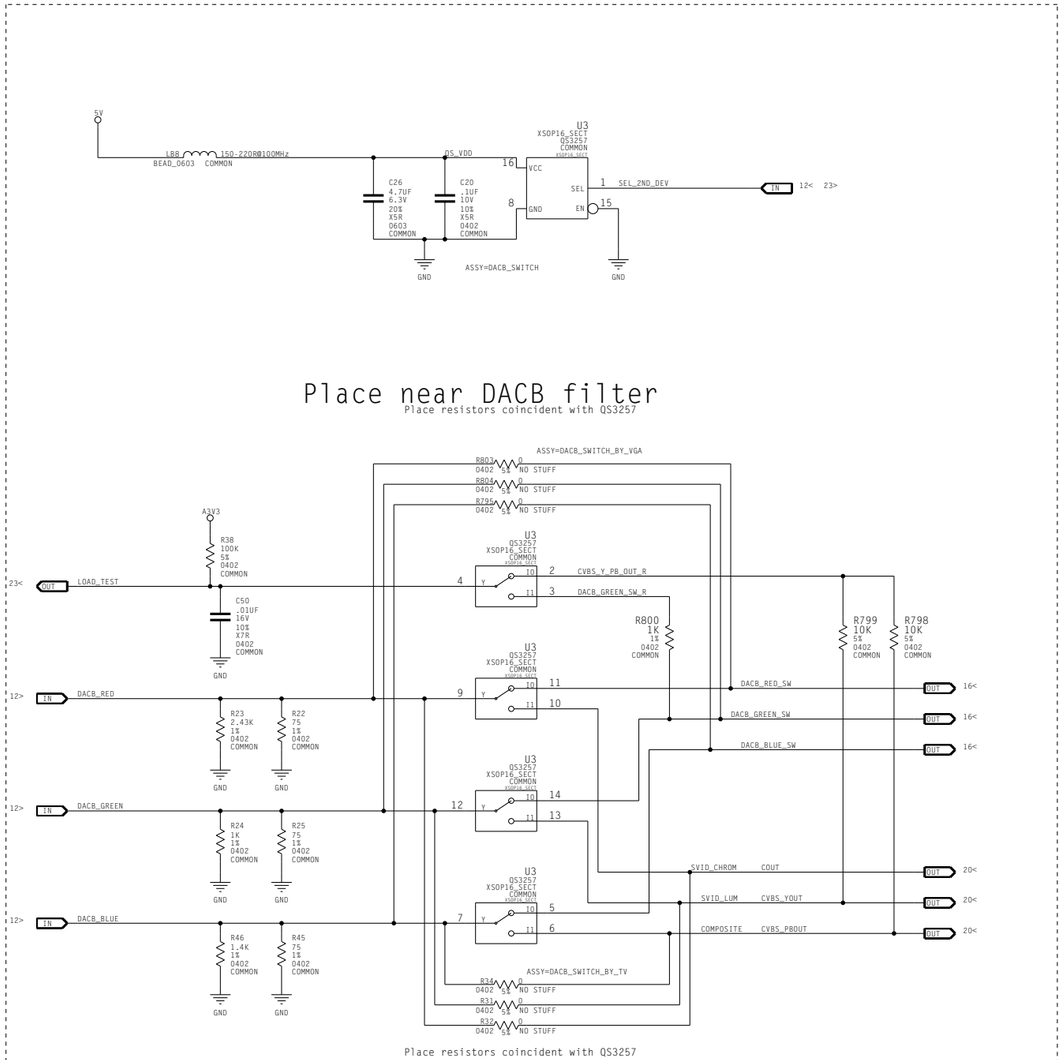
Place in output filter section!

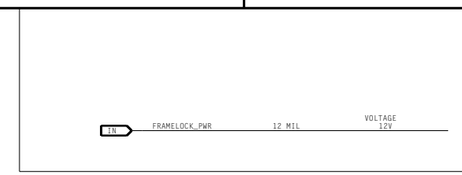
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

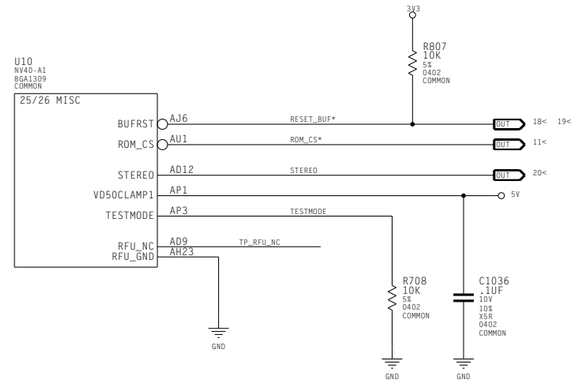
NV_PN	600-10201-0002-000		
ID	design	PAGE	14 OF 28
NAME	Hunter	DATE	11-FEB-2004

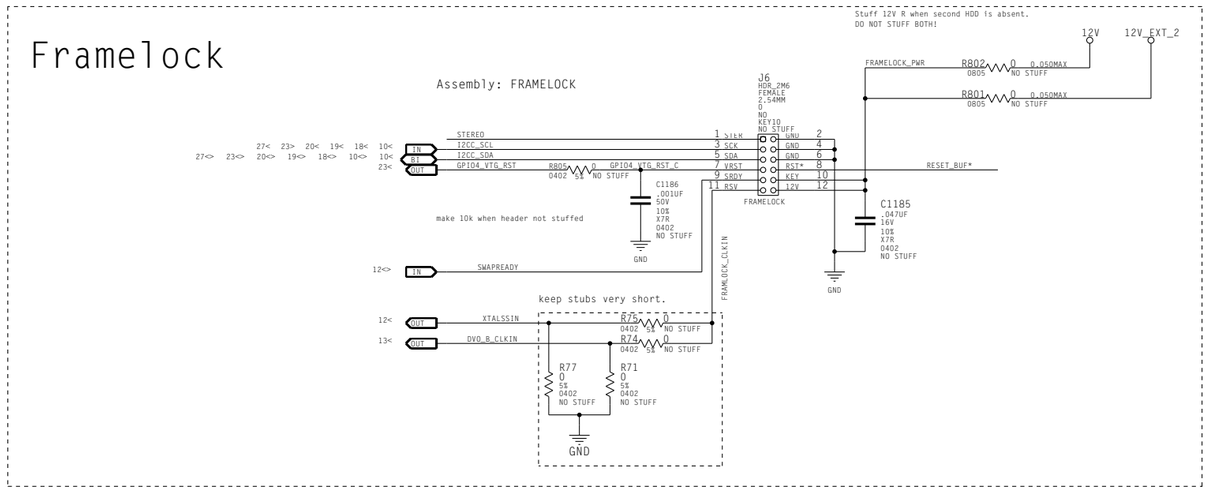
15. DACB VGA/TV Switch, miscellaneous GPU connections

Quickswitch for DACB









ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DACB VGA/TV Switch, Framelock, MISC GPU signals

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	15 OF 28
NAME	Hunter	DATE	11-FEB-2004

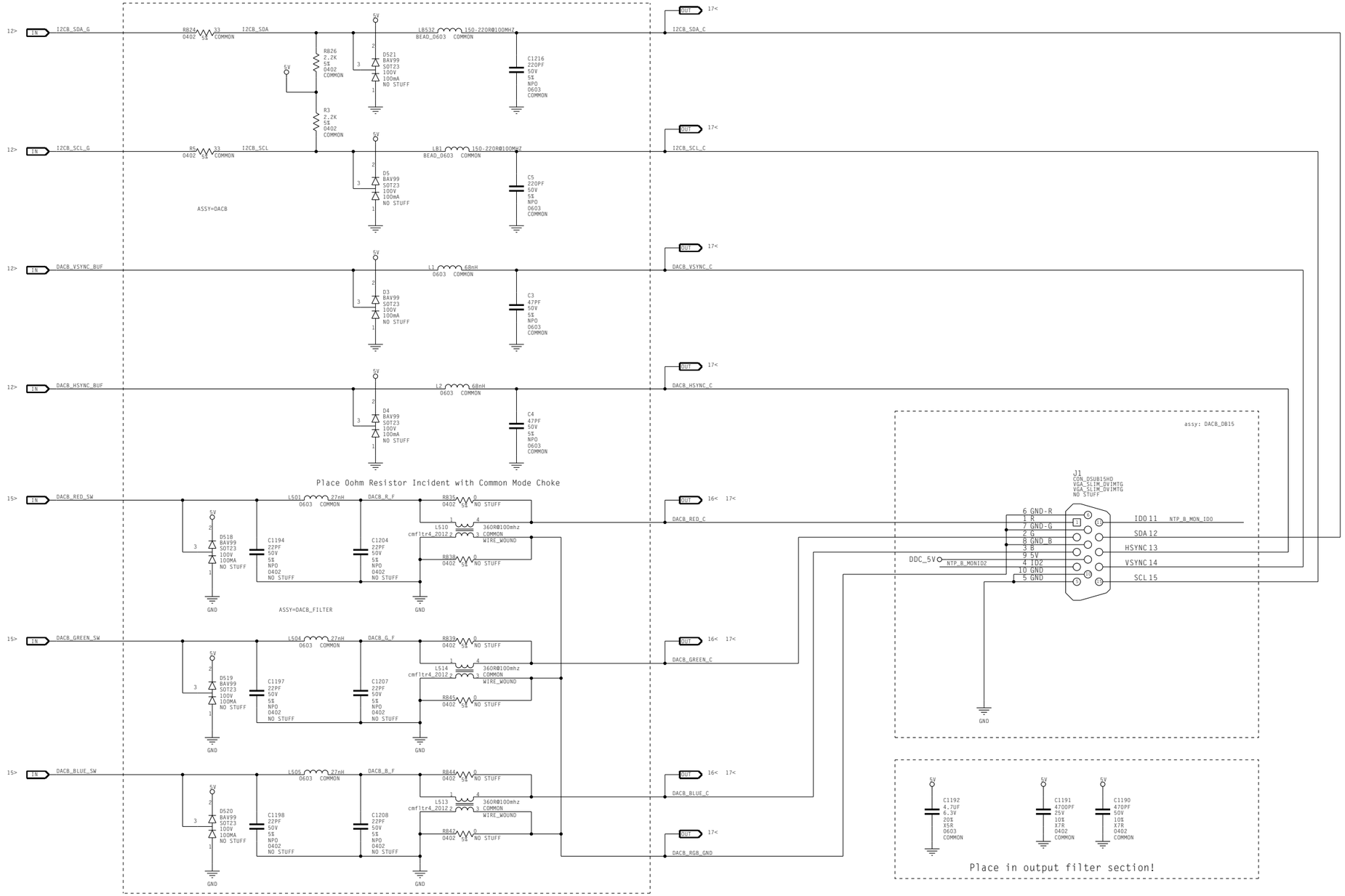
16. DACB RGB filters, VGA connector (north)

NET RULES

		NET	LINE W.	IMPEDANCE	SPACING
15<	12>	DACB_RED		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
15<	12>	DACB_GREEN		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
15<	12>	DACB_BLUE		ALL:ALL:37.5 OHM:2 %	20MIL_G2G_30MIL
16<	15>	DACB_RED_SW	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
16<	15>	DACB_GREEN_SW	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
16<	15>	DACB_BLUE_SW	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
		DACB_R_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
		DACB_G_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
		DACB_B_F	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17<	16>	DACB_RED_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17<	16>	DACB_GREEN_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL
17<	16>	DACB_BLUE_C	4MIL	ALL:ALL:75 OHM:50 %	20MIL_G2G_30MIL

DACB RGB-FILTER

DACB VGA connector



ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DACB Filter and VGA connector

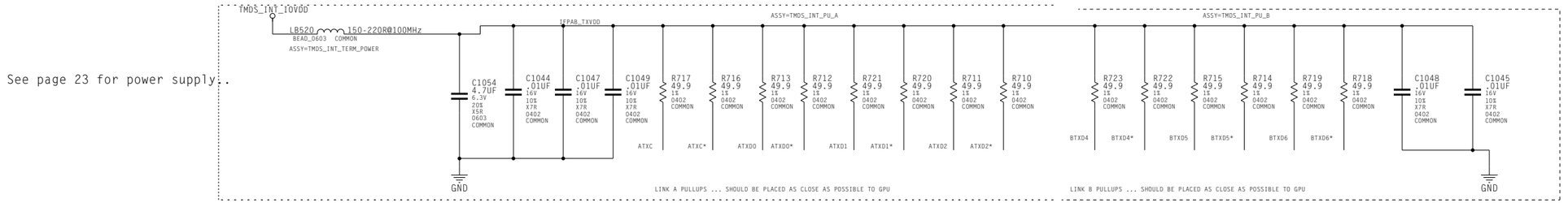
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

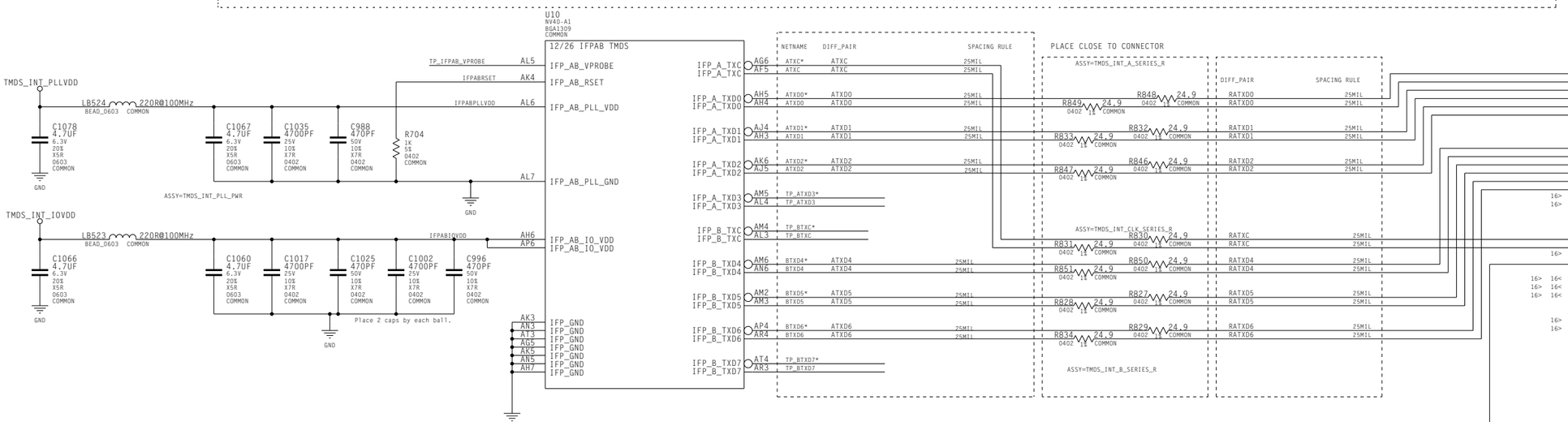
NV_PN	600-10201-0002-000		
ID	design	PAGE	16 OF 28
NAME	Hunter	DATE	11-FEB-2004

17. Internal and External TMDS (dual link X2)

See page 23 for power supply.

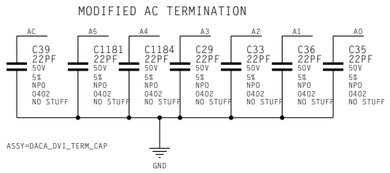
DVI B (mid) DAC B INTERNAL DUAL TMDS

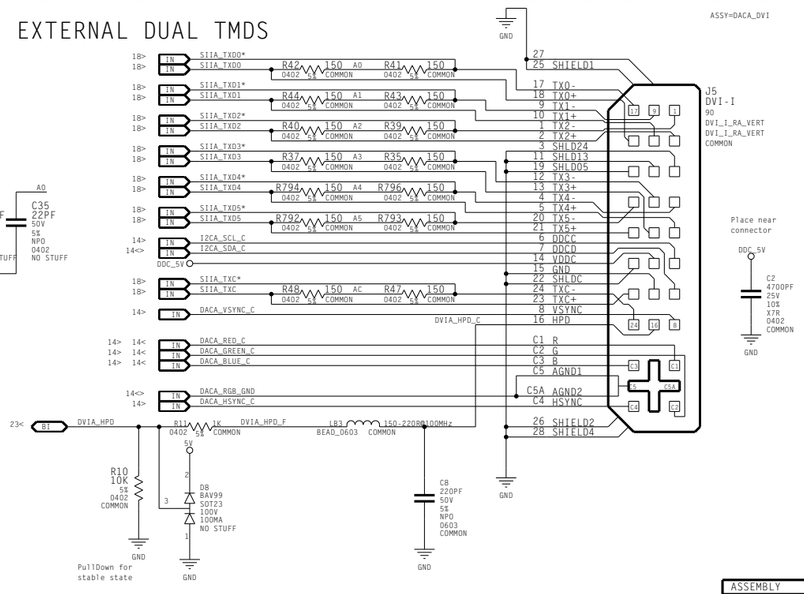




DVI A (south) DAC A, EXTERNAL DUAL TMDS

Place termination close to Silicon Image Chip





NET	LINE WIDTH	VOLTAGE
IFPABVREF	12 MIL	3.3V
IFPABPLLVDD	12 MIL	3.3V
IFPAIOVDD	12 MIL	3.3V
IFPBIOVDD	12 MIL	3.3V
TMDS_INT_PLLVDD	12 MIL	3.3V
TMDS_INT_IOVDD	12 MIL	3.3V
TMDS_BACK	12 MIL	3.3V
TMDS_BACK_1	12 MIL	3.3V
TMDS_BACK_2	12 MIL	3.3V
TMDS_BACK_3	12 MIL	3.3V
TMDS_BACK_4	12 MIL	3.3V

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DUAL LINK Internal TMDS, DVI Connectors

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	17 OF 28
NAME	Hunter	DATE	11-FEB-2004

18. External Dual-Link TMDS Transmitter

NET RULES (OTHER)

LINE WIDTH

SIIA_VCC	12 MIL	SIIA_VCC
SIIA_AVCC	12 MIL	SIIA_AVCC
SIIA_PVCC1	12 MIL	SIIA_PVCC1
SIIA_PVCC2	12 MIL	SIIA_PVCC2

ASSY: TMDS_EXT_SD stuff for single/dual link
ASSY: TMDS_EXT_D stuff for dual link
ASSY: TMDS_EXT_S stuff for single link

I2C=0x72 (Slave)

U507 SII178 78_TQFP64 COMMON — SLAVE BOTTOM

SII1xx (combi_sym)

NV40 Dual Link:
Even (D11..0) pixel via master, odd (D23..12) via slave.

NET	DIFFPAIR	SPACING	PHYSICAL
SIIA_TXD3	SIIA_TXD3	20MIL	4MIL_TRACE
SIIA_TXD3*	SIIA_TXD3	20MIL	4MIL_TRACE
SIIA_TXD4	SIIA_TXD4	20MIL	4MIL_TRACE
SIIA_TXD4*	SIIA_TXD4	20MIL	4MIL_TRACE
SIIA_TXD5	SIIA_TXD5	20MIL	4MIL_TRACE
SIIA_TXD5*	SIIA_TXD5	20MIL	4MIL_TRACE
NTP_SIIA_TXC			
NTP_SIIA_TXC*			

DVO_A_D<23..0> → D<23>..D<12>; D<14>/SYNCOUT; D<13>/MAST; D<12>/DUAL; D<11>..D<0>

HSYNC/SYNCIN, VSYNC, DE, IDCLK, IDCLK

CTL1/A1/DK1/MCL, CTL2/A2/DK2/MDA, CTL3/A3/DK3/ .

BSEL/SCL, DSEL/SDA, ISEL/RST#, MSEN, EDG/HPD, DKEN/GND

EXT_SWING, AVCC, PVCC1, PVCC2, VCC, VREF, PD, RESVD(GND), AGND, PGND1, PGND2, GND

Note a:
STUFFING OPTION:
Rdual for Dual-Link
Rsing for Single-Link

Note a:
Rdual R58 0 5% 0402 COMMON
Rsing R57 0 5% 0402 NO STUFF

Note a:
Rdual R769 1.5K 5% 0402 COMMON
Rsing R768 1.5K 5% 0402 NO STUFF

I2C=0x70 (Master)

U5 SII178 78_TQFP64 COMMON — MASTER TOP

NET	DIFFPAIR	SPACING	PHYSICAL
SIIA_TXD0	SIIA_TXD0	20MIL	4MIL_TRACE
SIIA_TXD0*	SIIA_TXD0	20MIL	4MIL_TRACE
SIIA_TXD1	SIIA_TXD1	20MIL	4MIL_TRACE
SIIA_TXD1*	SIIA_TXD1	20MIL	4MIL_TRACE
SIIA_TXD2	SIIA_TXD2	20MIL	4MIL_TRACE
SIIA_TXD2*	SIIA_TXD2	20MIL	4MIL_TRACE
SIIA_TXC	SIIA_TXC	20MIL	4MIL_TRACE
SIIA_TXC*	SIIA_TXC	20MIL	4MIL_TRACE

DUAL_SYNC, DUAL_SELECT

STUFF OPTION
Rx for SII164/166
Ry for SII178

For Single Link SIL164/168 is used

CTL3 → R70 0 5% 0402 COMMON → DVO_A_CTL3 (ASSY=TMDS_EXT_CTL3); R64 0 5% 0402 NO STUFF

Sil178 Dual-Link TMDS

ISEL/RST - I2C Interface Select.
HIGH - active (config programmed by I2C)

When ISEL/RST = HIGH
BSEL/SCL - I2C CLK
DSEL/SDA - I2C DATA

MASTER
I2C Address is 70h and is based on MAST and DUAL pins.

SLAVE
I2C Address is 72h

Notes:

Make sure Software knows and programs this correctly.
1. Detect Dual-Link Capable
2. Detect Master and Slave
3. Both Master and Slave transmitters must set bit 2 (BSEL) at register addr 0x08 to 0 for 12-biot mode
4. For frequencies less than or equal to 165Mhz, bit 0 (PD) at register addr 0x08 of Slave must be set to 0. For frequencies greater than 165Mhz, bit 0 (PD) at register addr 0x08 of Slave must be set to 1.
5. Skew between Master and Slave can be controlled by DCTL[2:0] register
6. Both Single-Link and Dual-Link mode will be configured via I2CC

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	DUAL LINK TMDS External with SiIicon Image

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	18 OF 28
NAME	Hunter	DATE	11-FEB-2004

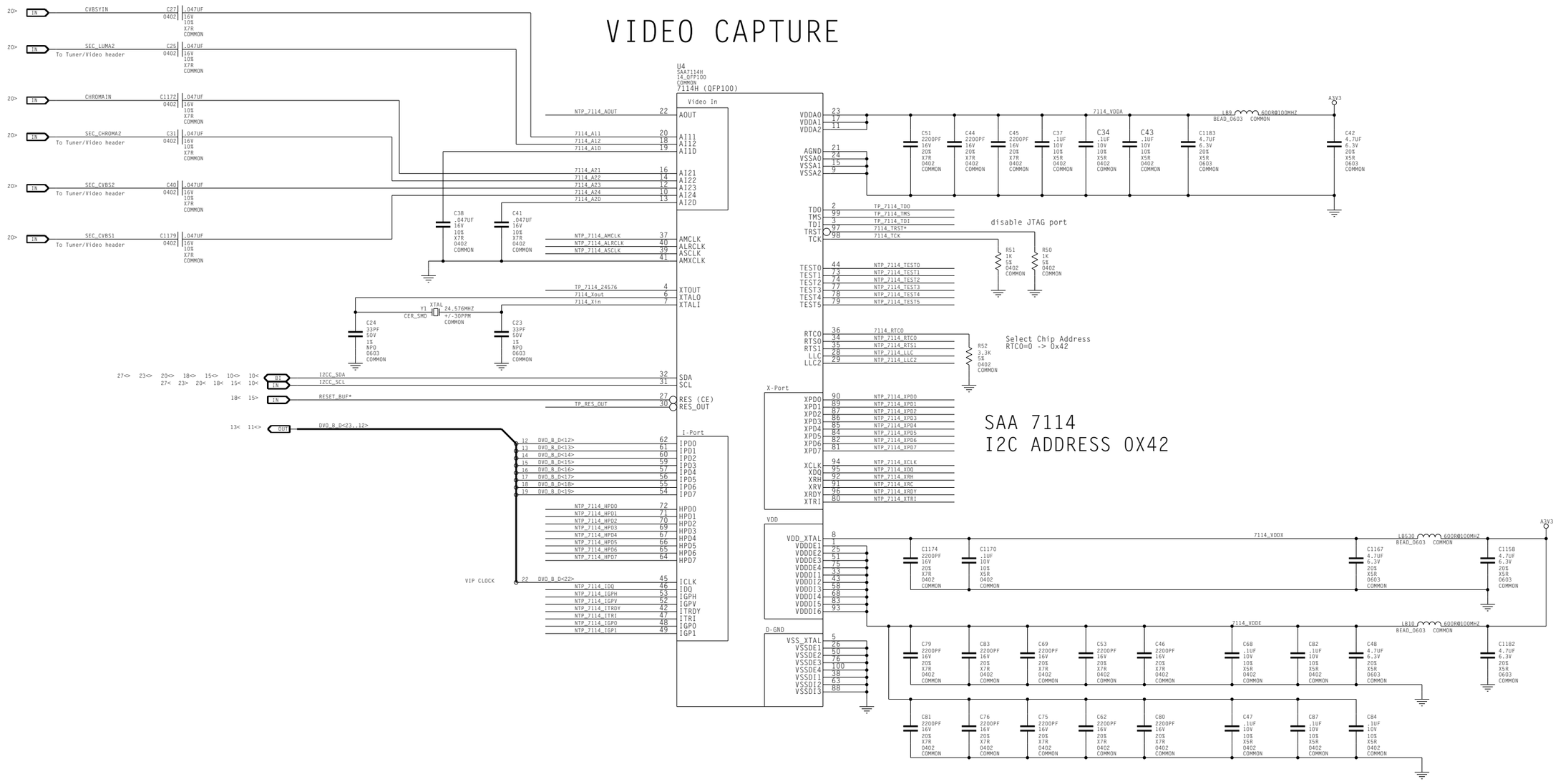
19. Video Capture

NET RULES

	NET	SPACING	LINE WIDTH	VOLTAGE
IN	7114_VDDA		12 MIL	3.3V
IN	7114_VDDE		12 MIL	3.3V
IN	7114_VDDX		12 MIL	3.3V
IN	7114_Xout	20MIL		
IN	7114_Xin	20MIL		

ASSY: 7114_COMMON

VIDEO CAPTURE



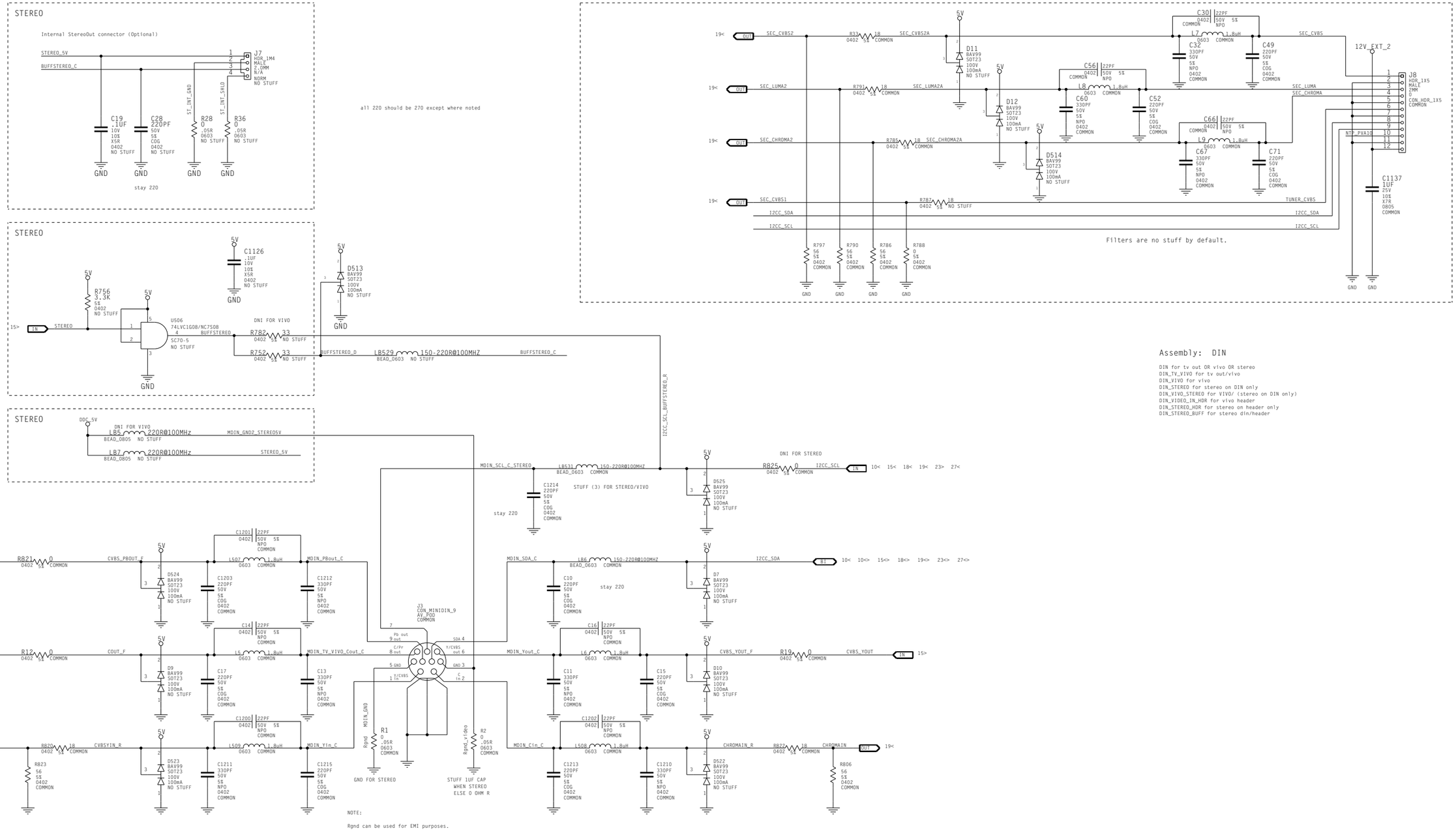
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Video Capture (SAA7114)

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	19 OF 28
NAME	Hunter	DATE	11-FEB-2004

20. S-Video Out, CVBS Out, CVBS/S-Video in, MINIDIN

PCI TUNER / INTERNAL VIDEO NOTES:
1X5 header can be used if only internal video is required.
1X12 header will be populated for both PCI tuner and internal video.



Assembly: DIN

DIN for tv out OR vivo OR stereo
DIN_TV_VIVO for tv out/vivo
DIN_VIVO for vivo
DIN_STEREO for stereo on DIN only
DIN_VIVO_STEREO for VIVO/ (stereo on DIN only)
DIN_VIDEO_IN_HDR for vivo header
DIN_STEREO_HDR for stereo on header only
DIN_STEREO_BUFF for stereo din/header

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Video In/Out Connector External/Internal (MiniDin), STEREO header

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	20 OF 28
NAME	Hunter	DATE	11-FEB-2004

21. FBVTT AND FBVDDQ DECOUPLING, AND Misc...

U10
NV40-A1
BGA1309
COMMON

8/26

FB_VTT	P13
FB_VTT	R13
FB_VTT	T13
FB_VTT	V13
FB_VTT	W13
FB_VTT	N14
FB_VTT	N15
FB_VTT	N16
FB_VTT	N18
FB_VTT	N22
FB_VTT	N24
FB_VTT	N25
FB_VTT	N26
FB_VTT	AG26
FB_VTT	AH26
FB_VTT	P27
FB_VTT	R27
FB_VTT	T27
FB_VTT	AC27
FB_VTT	AE27
FB_VTT	AF27
FB_VTT	AC28

FBVTT

U10
NV40-A1
BGA1309
COMMON

7/26

FBVDDQ

V11	FB_VDDQ
W11	FB_VDDQ
N12	FB_VDDQ
R12	FB_VDDQ
T12	FB_VDDQ
U12	FB_VDDQ
V12	FB_VDDQ
W12	FB_VDDQ
L13	FB_VDDQ
M13	FB_VDDQ
N13	FB_VDDQ
M14	FB_VDDQ
M15	FB_VDDQ
M17	FB_VDDQ
L18	FB_VDDQ
M18	FB_VDDQ
M22	FB_VDDQ
M23	FB_VDDQ
M25	FB_VDDQ
AJ25	FB_VDDQ
M26	FB_VDDQ
L27	FB_VDDQ
M27	FB_VDDQ
N27	FB_VDDQ
W27	FB_VDDQ
AA27	FB_VDDQ
AG27	FB_VDDQ
AH27	FB_VDDQ
AJ27	FB_VDDQ
N28	FB_VDDQ
P28	FB_VDDQ
R28	FB_VDDQ
U28	FB_VDDQ
V28	FB_VDDQ
AB28	FB_VDDQ
AE28	FB_VDDQ
AF28	FB_VDDQ
AG28	FB_VDDQ
AJ28	FB_VDDQ
AG29	FB_VDDQ
AH29	FB_VDDQ

FBVDDQ

Place near BGA

C954	C795	C773	C770	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C952	C846	C757	C801	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C822	C847	C900	C791	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C772	C790	C777	C764	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C756	C775	C752	C910	
1UF	1UF	1UF	10UF	
10V	10V	10V	6.3V	
10%	10%	10%	20%	
X7R	X7R	X7R	X5R	
0603	0603	0603	0805	
COMMON	COMMON	COMMON	COMMON	
C864	C1040		C748	
10UF	10UF		10UF	
6.3V	6.3V		6.3V	
20%	20%		20%	
X5R	X5R		X5R	
0805	0805		0805	
COMMON	COMMON		COMMON	
C744	C793	C746		
10UF	10UF	10UF		
6.3V	6.3V	6.3V		
20%	20%	20%		
X5R	X5R	X5R		
0805	0805	0805		
COMMON	COMMON	COMMON		

GND

FBVTT

Place near BGA

C938	C821	C818	C863	C904
470OPF	.022UF	.1UF	.1UF	.1UF
25V	16V	10V	10V	10V
10%	10%	10%	10%	10%
X7R	X7R	X5R	X5R	X5R
0402	0402	0402	0402	0402
NO STUFF	NO STUFF	NO STUFF	NO STUFF	NO STUFF

GND

C794	C903	C948	C922
.01UF	.01UF	.01UF	.01UF
25V	25V	25V	25V
10%	10%	10%	10%
X7R	X7R	X7R	X7R
0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON
C816	C941	C881	C940
.01UF	.01UF	.01UF	.01UF
25V	25V	25V	25V
10%	10%	10%	10%
X7R	X7R	X7R	X7R
0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON
C813	C959	C835	C947
.01UF	.01UF	.01UF	.01UF
25V	25V	25V	25V
10%	10%	10%	10%
X7R	X7R	X7R	X7R
0402	0402	0402	0402
COMMON	COMMON	COMMON	COMMON

GND

C753	C956	C826	C953	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C994	C840	C812	C763	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C993	C1014	C815	C792	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C762	C979	C866	C962	
1UF	1UF	1UF	10UF	
10V	10V	10V	6.3V	
10%	10%	10%	20%	
X7R	X7R	X7R	X5R	
0603	0603	0603	0805	
COMMON	COMMON	COMMON	COMMON	

GND

C862	C921	C951	C848	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C845	C834	C810	C901	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C672	C995	C817	C1023	
470OPF	.022UF	.1UF	.1UF	
25V	16V	10V	10V	
10%	10%	10%	10%	
X7R	X7R	X5R	X5R	
0402	0402	0402	0402	
COMMON	COMMON	COMMON	COMMON	
C898	C999	C837	C1019	
1UF	1UF	1UF	10UF	
10V	10V	10V	6.3V	
10%	10%	10%	20%	
X7R	X7R	X7R	X5R	
0603	0603	0603	0805	
COMMON	COMMON	COMMON	COMMON	

GND

U10
NV40-A1
BGA1309
COMMON

21/26 GND

K23	GND	GND	D1
N23	GND	GND	G1
AG23	GND	GND	K1
A24	GND	GND	N1
E24	GND	GND	T1
G24	GND	GND	W1
C26	GND	GND	AA1
K26	GND	GND	AD1
AK26	GND	GND	AG1
AU26	GND	GND	AK1
A27	GND	GND	AN1
E27	GND	GND	A11
G27	GND	GND	E3
U27	GND	GND	H3
AD27	GND	GND	L3
AN27	GND	GND	P3
AR27	GND	GND	U3
AW27	GND	GND	Y3
M28	GND	GND	AA3
Y28	GND	GND	AD3
AH28	GND	GND	AG3
C29	GND	GND	A4
K29	GND	GND	AU4
AK29	GND	GND	AW4
AU29	GND	GND	C5
A30	GND	GND	G5
E30	GND	GND	K5
G30	GND	GND	N5
L30	GND	GND	T5
P30	GND	GND	W5
U30	GND	GND	AA5
W30	GND	GND	AD5
AA30	GND	GND	A7
AC30	GND	GND	E7
AF30	GND	GND	G7
AJ30	GND	GND	K7
AN30	GND	GND	N7
AR30	GND	GND	T7
AW30	GND	GND	AD7
C32	GND	GND	AG7
W32	GND	GND	AK7
AA32	GND	GND	AN7
AU32	GND	GND	AP7
A33	GND	GND	AR7
E33	GND	GND	AU7
G33	GND	GND	AW7
K33	GND	GND	C8
N33	GND	GND	W8
T33	GND	GND	AA8
AD33	GND	GND	AC9
AG33	GND	GND	AF9
AK33	GND	GND	AJ9
AN33	GND	GND	A10
AR33	GND	GND	E10
AW33	GND	GND	G10
C35	GND	GND	L10
G35	GND	GND	P10
K35	GND	GND	U10
N35	GND	GND	W10
T35	GND	GND	AA10
W35	GND	GND	AN10
AA35	GND	GND	AU10
AD35	GND	GND	AW10
AG35	GND	GND	C11
AK35	GND	GND	K11
AN35	GND	GND	AL11
AU35	GND	GND	AA12
A36	GND	GND	AE12
AW36	GND	GND	AH12
E37	GND	GND	AJ12
H37	GND	GND	A13
L37	GND	GND	E13
P37	GND	GND	G13
U37	GND	GND	U13
Y37	GND	GND	AE13
AA37	GND	GND	C14
AC37	GND	GND	K14
AF37	GND	GND	AH14
AJ37	GND	GND	A16
AM37	GND	GND	E16
AR37	GND	GND	G16
C38	GND	GND	M16
D39	GND	GND	C17
G39	GND	GND	K17
K39	GND	GND	N17
N39	GND	GND	AG17
T39	GND	GND	AH17
W39	GND	GND	A19
AA39	GND	GND	C19
AD39	GND	GND	E19
AG39	GND	GND	H19
AK39	GND	GND	K19
AN39	GND	GND	C20
A139	GND	GND	M20
		GND	AH20
		GND	A21
		GND	E21
		GND	H21
		GND	K21
		GND	C23

GND

GND

U10
NV40-A1
BGA1309
COMMON

26/26

NC	AA11	NTP_NC_0
NC	AG13	NTP_NC_1
NC	W29	NTP_NC_2

U10
NV40-A1
BGA1309
COMMON

22/26 TGND

AC20	T_GND	T_GND	U15
AD20	T_GND	T_GND	Y15
AE20	T_GND	T_GND	AC15
U21	T_GND	T_GND	U16
V21	T_GND	T_GND	Y16
W21	T_GND	T_GND	AC16
AA21	T_GND	T_GND	R17
AB21	T_GND	T_GND	T17
AC21	T_GND	T_GND	U17
U22	T_GND	T_GND	V17
V22	T_GND	T_GND	W17
W22	T_GND	T_GND	Y17
Y22	T_GND	T_GND	AA17
AA22	T_GND	T_GND	AB17
AB22	T_GND	T_GND	AC17
AC22	T_GND	T_GND	AD17
R23	T_GND	T_GND	AE17
T23	T_GND	T_GND	U18
U23	T_GND	T_GND	V18
V23	T_GND	T_GND	W18
W23	T_GND	T_GND	Y18
Y23	T_GND	T_GND	AA18
AA23	T_GND	T_GND	AB18
AB23	T_GND	T_GND	AC18
AC23	T_GND	T_GND	U19
AD23	T_GND	T_GND	V19
AE23	T_GND	T_GND	W19
U24	T_GND	T_GND	AA19
Y24	T_GND	T_GND	AB19
AC24	T_GND	T_GND	AC19
U25	T_GND	T_GND	R20
Y25	T_GND	T_GND	T20
AC25	T_GND	T_GND	U20
		T_GND	V20
		T_GND	AB20

GND

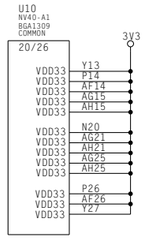
GND

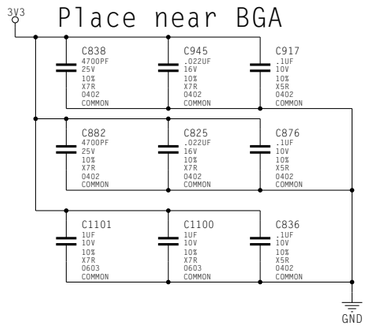
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	FBVDDQ, FBVTT DECOUP

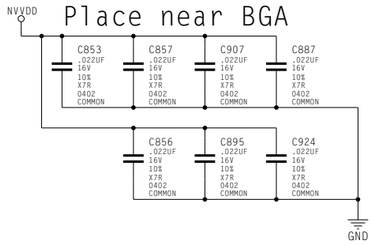
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

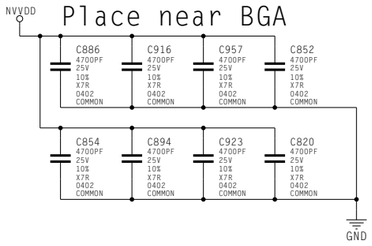
NV_PN	600-10201-0002-000		
ID	design	PAGE	21 OF 28
NAME	Hunter	DATE	11-FEB-2004

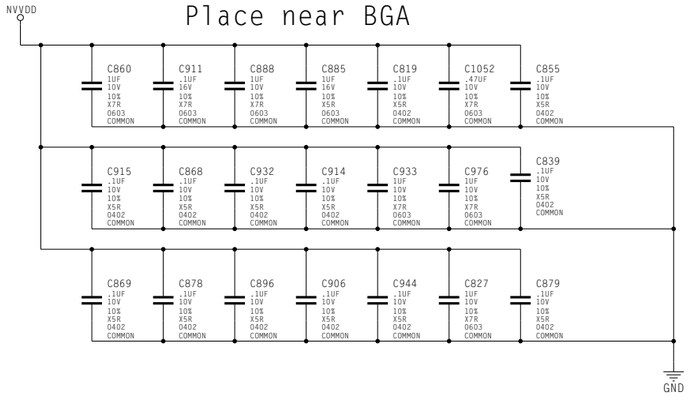
22. VDD AND NVVDD DECOUPLING

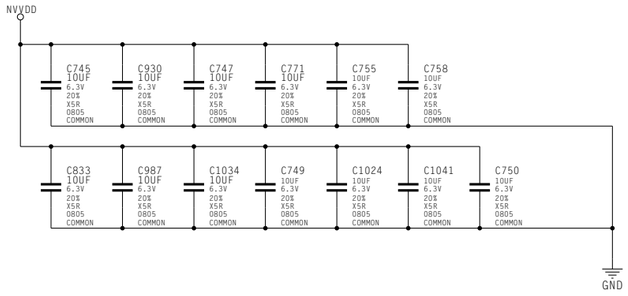


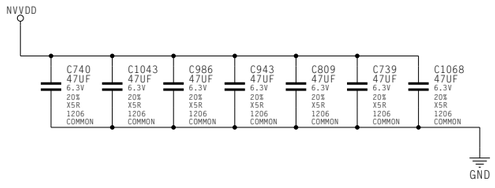


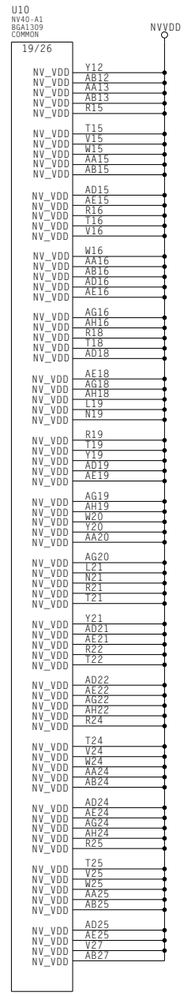












ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	3V3, NVVDD DECOUP

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

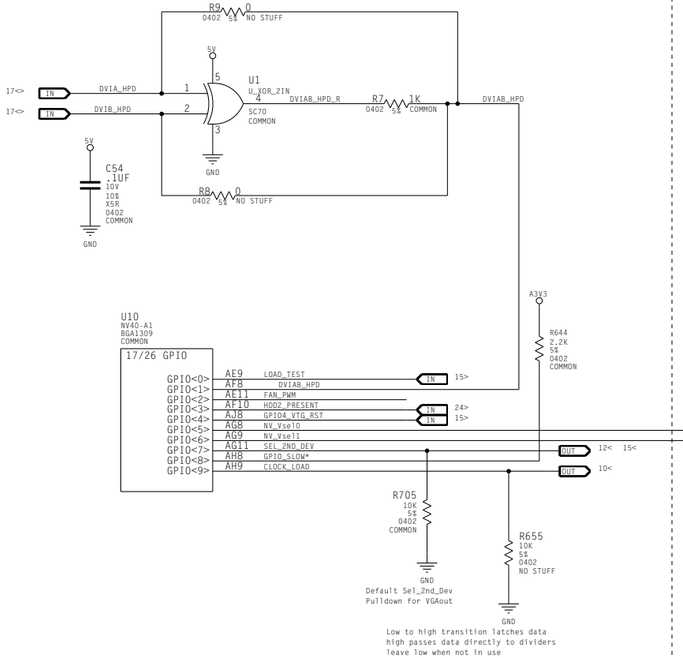
NV_PN	600-10201-0002-000		
ID	design	PAGE	22 OF 28
NAME	Hunter	DATE	11-FEB-2004

23. GPIO's, NVVDD Control, Fan & Thermal Control

NET RULES

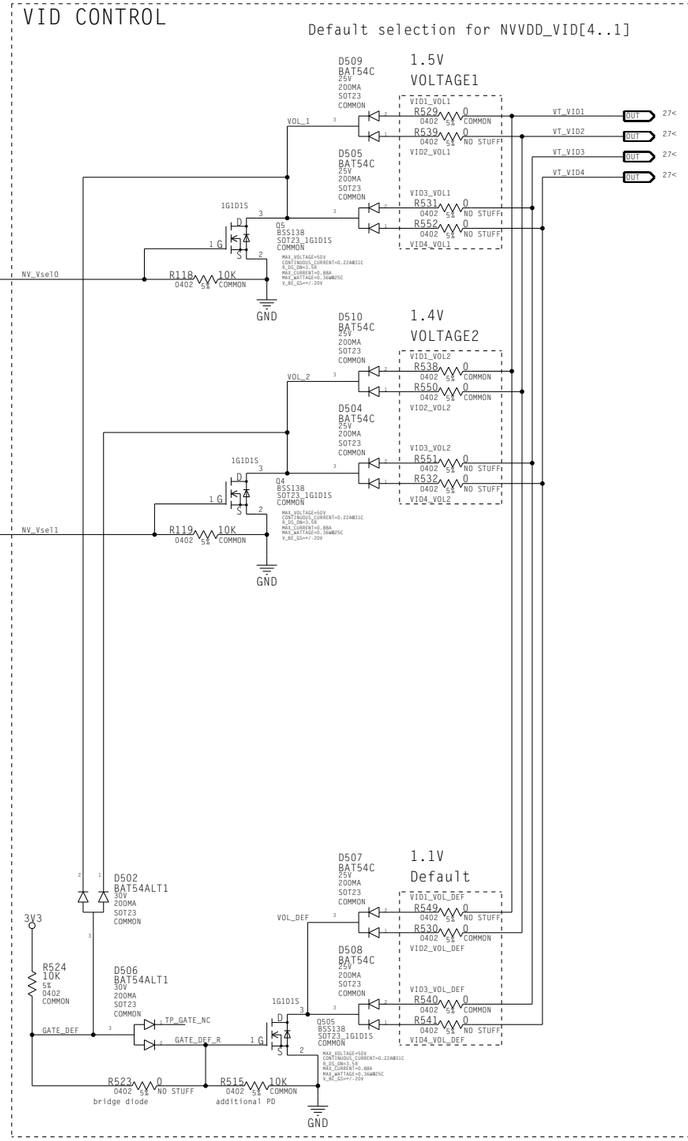
	NET	SPACING	LINE WIDTH
R1	THERMDA	10MIL	10MIL
R1	THERMDC	10MIL	10MIL
R1	FAN_PWM	20MIL	
R1	FAN_PWM_B	20MIL	12MIL
R1	FAN_PWM_C	20MIL	12MIL

GPIO CONTROL



VID CONTROL

Default selection for NVVDD_VID[4..1]



NVVDD Voltage Select

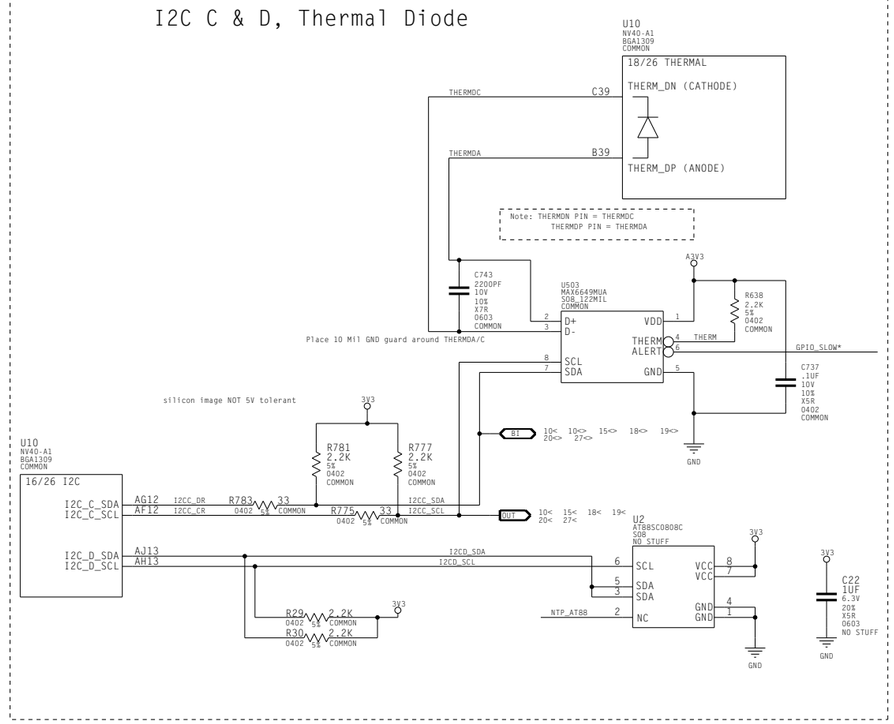
NVVDD = 0.8V-1.55V (60A)

Regulator: VT1103

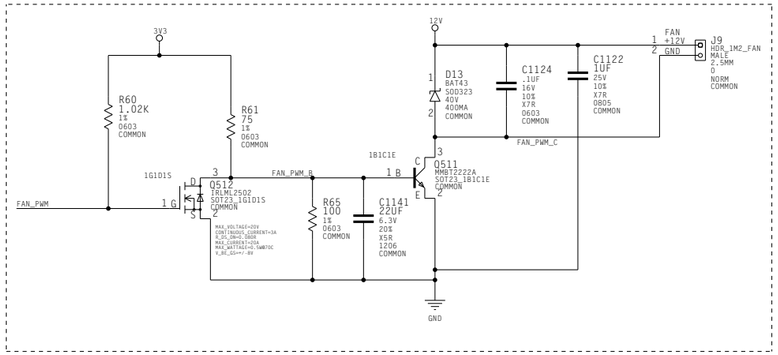
Control via NV_GPIOs NV_VSEL[2..0] :

VID 4 3 2 1	NVVDD Vout
1 1 1 1	0.80V
1 1 1 0	0.85V
1 1 0 1	0.90V
1 1 0 0	0.95V
1 0 1 1	1.00V
1 0 1 0	1.05V
1 0 0 1	1.10V
1 0 0 0	1.15V
0 1 1 1	0.20V
0 1 1 0	1.25V
0 1 0 1	1.30V
0 1 0 0	1.35V
0 0 1 1	1.40V
0 0 1 0	1.45V
0 0 0 1	1.50V
0 0 0 0	1.55V

I2C C & D, Thermal Diode



FAN CONTROL



ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	GPIOs, NVVDD VID, TEMP and FAN Control

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

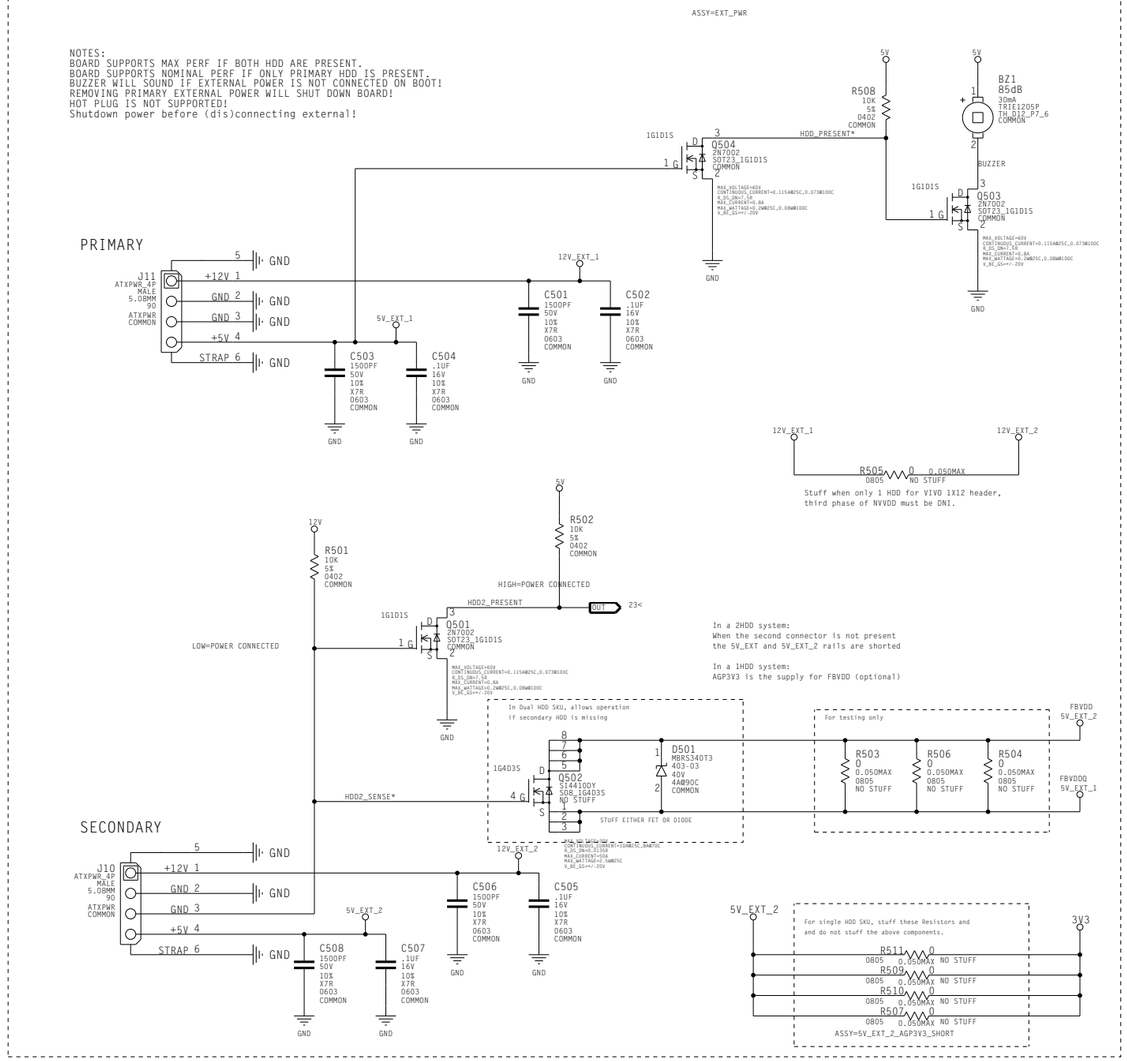
NV_PN	600-10201-0002-000		
ID	design	PAGE	23 OF 28
NAME	Hunter	DATE	11-FEB-2004

24. EXT POWER CONNECTION AND DETECTION

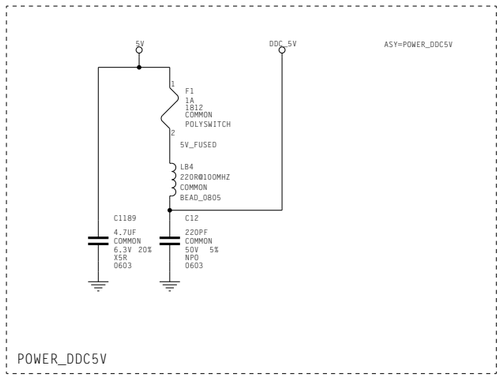
NET RULES

NET	LINE WIDTH	VOLTAGE
DDC_5V	12 MIL	5V
5V_FUSED	12 MIL	5V
BUZZER	5 MIL	5V

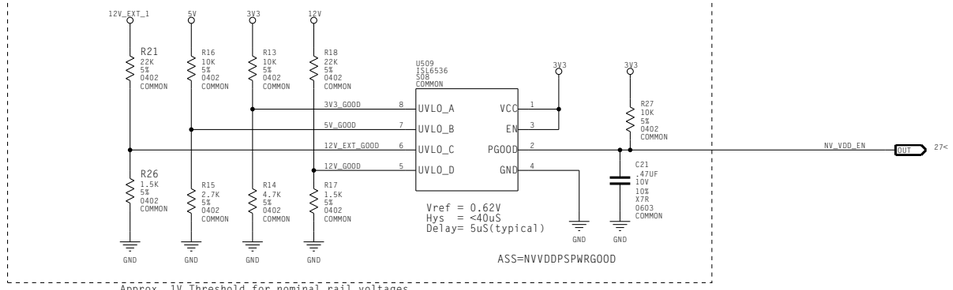
EXTERNAL POWER CONNECTORS, AUDIO ALERT



DDC 5V



Power Good



Approx. 1V Threshold for nominal rail voltages
Approx. ~.8V Threshold for NV_12V

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	EXTERNAL POWER CONNECTION AND DETECTION

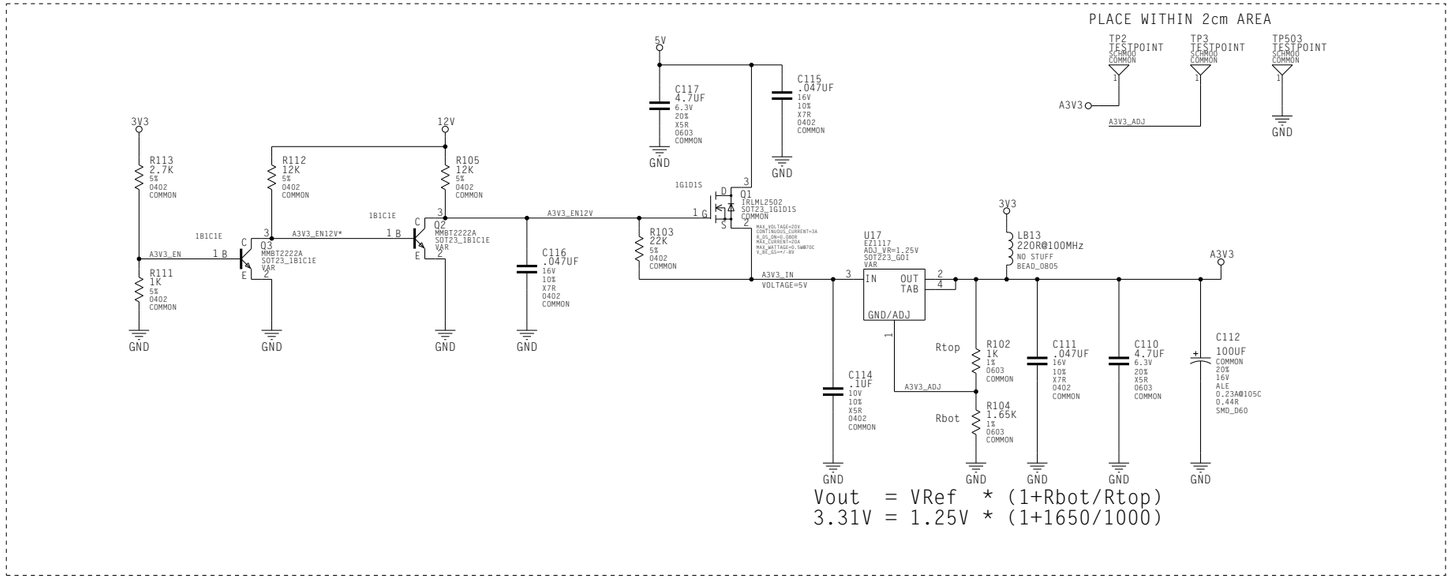
NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	24 OF 28
NAME	Hunter	DATE	11-FEB-2004

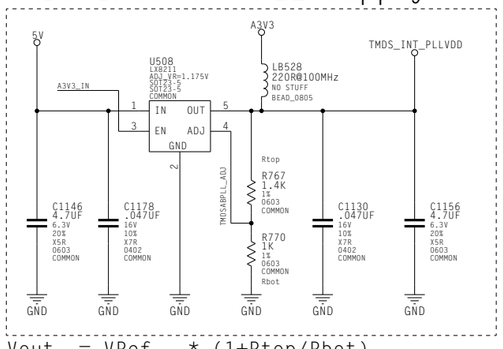
25. Power Supply I: Analog 3V3

NET	MIN_LINE_WIDTH	VOLTAGE	
A3V3	12MIL	3.3V	A3V3
TMDS_INT_IOVDD	12MIL	3.3V	TMDS_INT_IOVDD
TMDS_INT_PLLVDD	12MIL	3.3V	TMDS_INT_PLLVDD
A3V3_IN	12MIL	5V	
A3V3_ADJ	10MIL		
A3V3_EN12V	10MIL		
A3V3_EN12V*	10MIL		
A3V3_EN	10MIL		
TMDSOI_IN	12MIL	5V	

Analog Power Supply

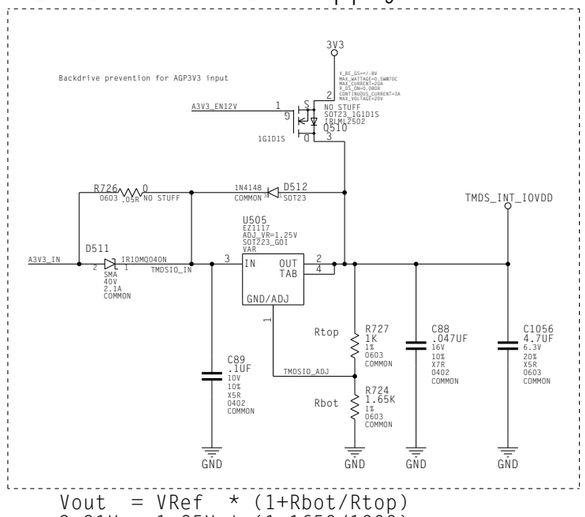


TMDS Internal PLL Supply



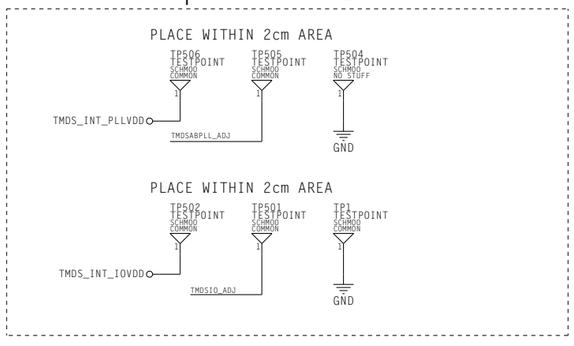
Vout = VRef * (1+Rtop/Rbot)
2.8V = 1.175V * (1+1400/1000)

TMDS Internal IO Supply



Vout = VRef * (1+Rbot/Rtop)
3.31V = 1.25V * (1+1650/1000)

SHMOO Testpoints TMDS



TMDS power sequencing done by using A3V3_IN.

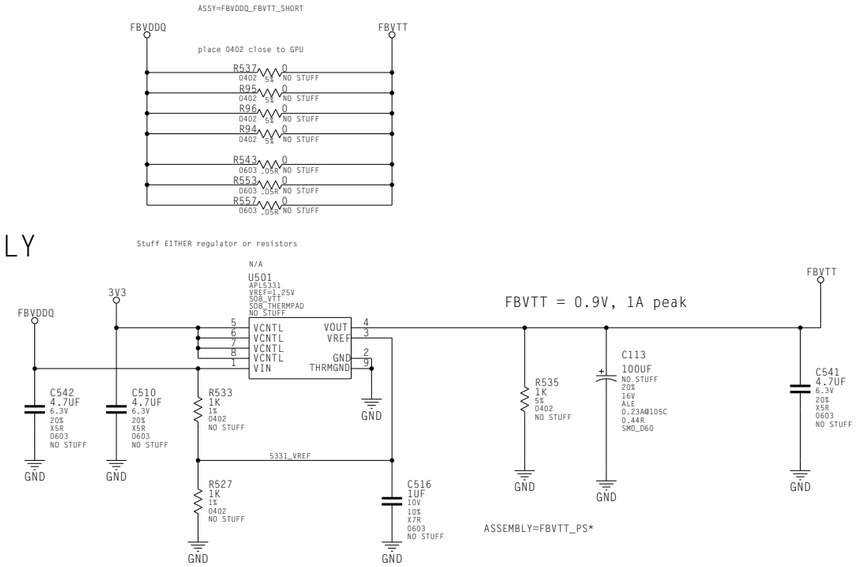
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	A3V3, TMDS IO POWER SUPPLIES

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

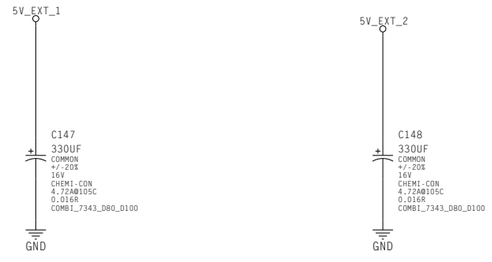
NV_PN	600-10201-0002-000		
ID	design	PAGE	25 OF 28
NAME	Hunter	DATE	11-FEB-2004

26. Power Supply III: FBVDDQ/FBVTT

FBVTT SUPPLY



INPUT FILTERS



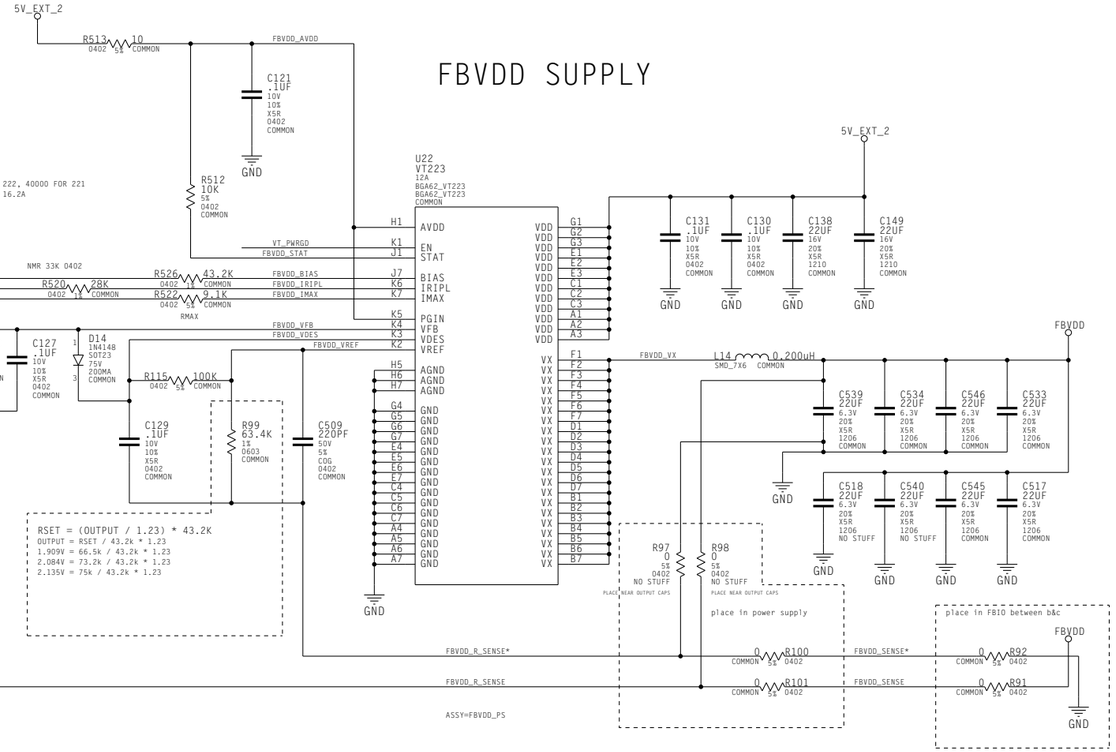
NET RULES

	NET	LINE WIDTH	VOLTAGE
BI	FBVDDQ_VX	12 MIL	3.3V
BI	FBVDD_VX	12 MIL	3.3V

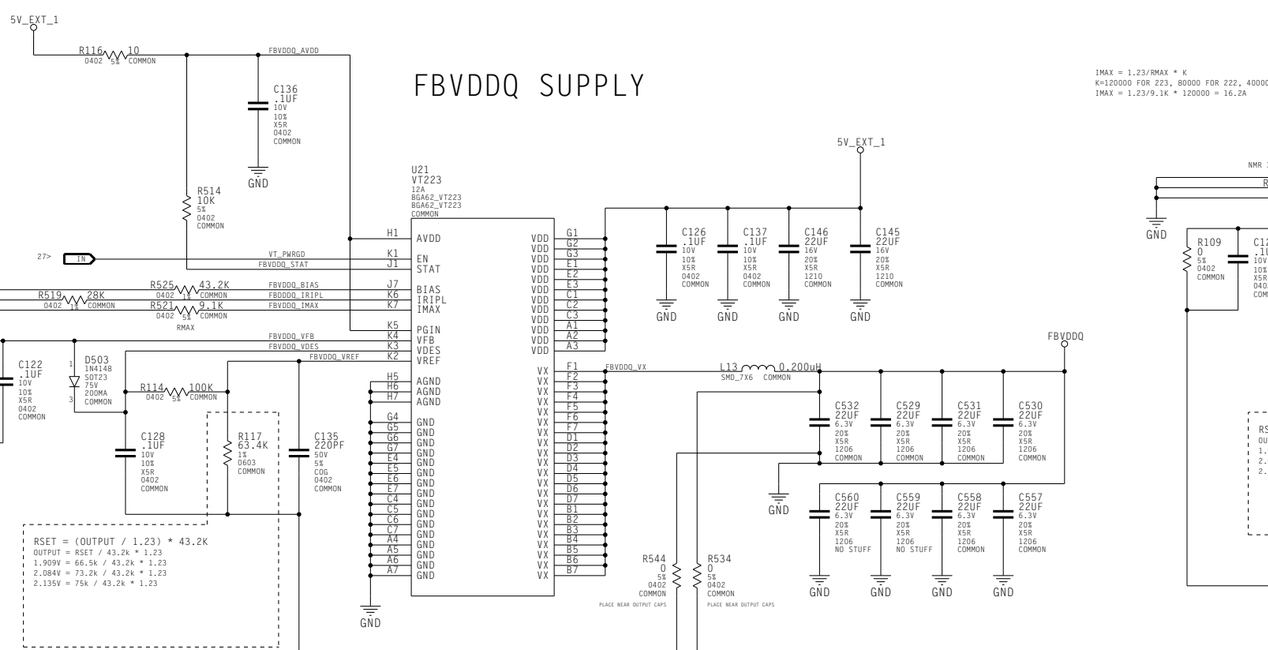
FBVDD	12 MIL	1.8V	FBVDD
FBVDDQ	12 MIL	1.8V	FBVDDQ
FBVTT	10 MIL	0.9V	FBVTT
5V_EXT_1	12 MIL	5V	5V_EXT_1
5V_EXT_2	12 MIL	5V	5V_EXT_2

	NET	DIFFPAIR	SPACING	LINE WIDTH
BI	FBVDD_SENSE		10MIL	10MIL_TRACE
BI	FBVDD_SENSE*	FBVDD_SENSE	10MIL	10MIL_TRACE

FBVDD SUPPLY



FBVDDQ SUPPLY



ASSEMBLY	ASSEMBLY=NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	FBVDD, FBVDDQ, FBVTT POWER SUPPLIES

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	26 OF 28
NAME	Hunter	DATE	11-FEB-2004

27. Power Supply IV: NVVDD

NVVDD = 0.8V..1.5V (60A)

NOTES:
For each 11035, the ground pins H6, H7, and Iref should be connected with traces to the input cap ground on J7 and there the via is located to tie to regular GND.

The analog ground amongst different 11035 should not be connected together.

4AMP SPEC Iripple each 22UF input CAP AT 100MF

0.005 OHM ESR AT 1MHZ, 100MF MLCC

NET RULES

NET	LINE WIDTH	VOLTAGE
5V	12 MIL	5V
NVVDD	24 MIL	1.4V
12V_EXT_1	12 MIL	12V
12V_EXT_2	12 MIL	12V
VT_VX0	12 MIL	1.4V
VT_VX1	12 MIL	1.4V
VT_VX2	12 MIL	1.4V

NET	DIFFPAIR	SPACING	LINE WIDTH
NVVDD_SENSE	NVVDD_SENSE	10MIL	10MIL_TRACE
NVVDD_SENSE*	NVVDD_SENSE	10MIL	10MIL_TRACE
FBVDDQ_SENSE	FBVDDQ_SENSE	10MIL	10MIL_TRACE
FBVDDQ_SENSE*	FBVDDQ_SENSE	10MIL	10MIL_TRACE

NVVDD Voltage Select

Regulator: VT1103

Control via NV_GPIOs NV_VSEL[2..0] :

NV_VSEL VID (2 1 0 4 3 2 1 0)	NVVDD (Vofs=0V) Vout	
1 1 1 0 0 0 1 0	1.50V	
1 1 0 0 0 1 1 0	1.40V	
1 0 1 0 0 1 0 1 0	1.30V	
1 0 0 0 0 1 1 1 0	1.20V	
0 1 1 1 0 0 1 0	1.10V	(default)
0 1 0 1 0 0 1 0	1.00V	
0 0 1 1 1 0 1 0	0.90V	
0 0 0 1 1 1 1 0	0.80V	

* GPIO's are inverted

Defaults are defined on Page 23

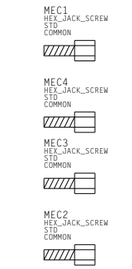
Rofs = OR

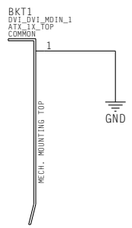
ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	NVVDD POWER SUPPLY

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	27 OF 28
NAME	Hunter	DATE	11-FEB-2004

28. MECHANICAL





bkt - dual slot DVI-DVI-MDIN = 151-10001-0007-000

cooler - ???

ASSEMBLY	NV40, 400N/500M, 256MB, DVI-I DUAL, DVI-I DUAL, VIVO, PCIID:0x041
PAGE DETAIL	Mechanical

NVIDIA CORPORATION
2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-10201-0002-000		
ID	design	PAGE	28 OF 28
NAME	Hunter	DATE	11-FEB-2004