Integrated Circuit Systems, Inc.

ICS950405

AMD - K8™ System Clock Chip

Recommended Application:
AMD K8 System Clock with AMD, VIA or ALI Chipset

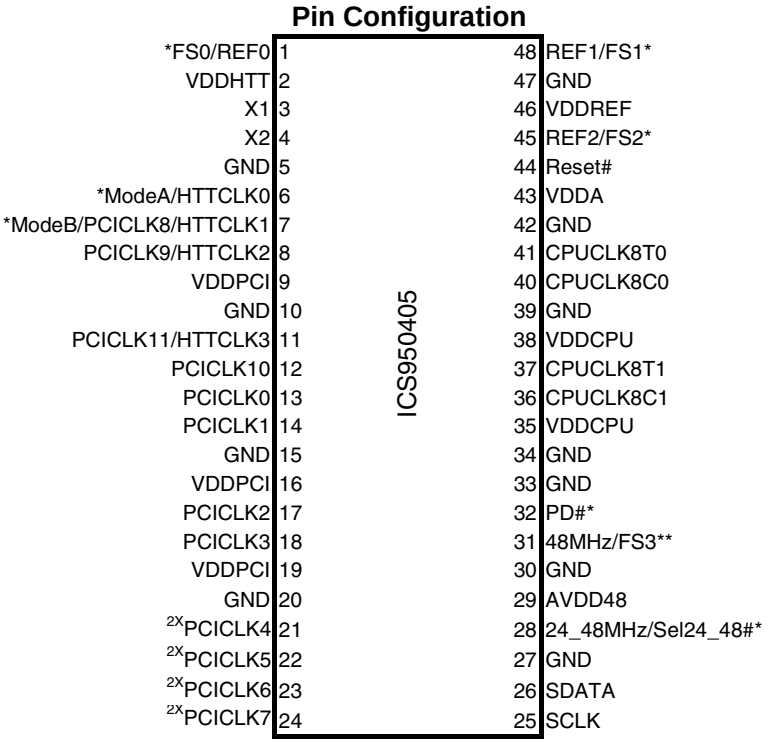
Output Features:
- 2 - Differential pair push-pull CPU clocks @ 3.3V
- 9 - PCICLK (Including 1 free running) @ 3.3V
- 3 - Selectable PCICLK/HTTCLK @ 3.3V
- 1 - HTTCLK @ 3.3V
- 1 - 48MHz @ 3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 3 - REF @ 3.3V, 14.318MHz.

Features:
- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Watchdog timer technology and RESET# output to reset system
  if system malfunctions.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz crystal.
- Supports Hyper Transport Technology (HTTCLK).

Functionality

FS3	FS2	FS1	FS0	CPU MHz	HTT MHz	PCI MHz
0	0	0	0	100.90	67.27	33.63
0	0	0	1	133.90	66.95	33.48
0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	66.68	33.34
0	1	1	1	200.40	66.80	33.40
1	0	0	0	150.00	60.00	30.00
1	0	0	1	180.00	60.00	30.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	30.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	33.33
1	1	1	1	300.00	75.00	37.50

Pin Configuration



48-SSOP

* Internal Pull-Up Resistor

2X This Output has 2X Default Drive and can be programmaed lower via IIC

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	VDDHTT	PWR	Supply for HTT clocks, nominal 3.3V.
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	GND	PWR	Ground pin.
6	*ModeA/HTTCLK0	I/O	Mode selection latch input pin / Hyper Transport output.
7	*ModeB/PCICLK8/HTTCLK1	I/O	Mode selection latch input pin / PCI clock output / Hyper Transport output.
8	PCICLK9/HTTCLK2	OUT	PCI clock output / Hyper Transport output.
9	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
10	GND	PWR	Ground pin.
11	PCICLK11/HTTCLK3	I/O	PCI clock output / Hyper Transport output.
12	PCICLK10	OUT	PCI clock output.
13	PCICLK0	OUT	PCI clock output.
14	PCICLK1	OUT	PCI clock output.
15	GND	PWR	Ground pin.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	PCICLK2	OUT	PCI clock output.
18	PCICLK3	OUT	PCI clock output.
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	GND	PWR	Ground pin.
21	2XPCICLK4	OUT	PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC.
22	2XPCICLK5	OUT	PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC.
23	2XPCICLK6	OUT	PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC.
24	2XPCICLK7	OUT	PCI clock output. This output is default @ 2X drive and can be programmed to lower drive via IIC.
25	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
26	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
27	GND	PWR	Ground pin.
28	24_48MHz/Sel24_48#*	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
29	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
30	GND	PWR	Ground pin.
31	48MHz/FS3**	I/O	Fixed 48MHz clock output. 3.3V / 'Frequency select latch input pin
32	PD#*	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped.
33	GND	PWR	Ground pin.
34	GND	PWR	Ground pin.
35	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
36	CPUCLK8C1	OUT	Complimentary clock of differential 3.3V push-pull K8 pair.
37	CPUCLK8T1	OUT	True clock of differential 3.3V push-pull K8 pair.
38	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
39	GND	PWR	Ground pin.
40	CPUCLK8C0	OUT	Complimentary clock of differential 3.3V push-pull K8 pair.
41	CPUCLK8T0	OUT	True clock of differential 3.3V push-pull K8 pair.
42	GND	PWR	Ground pin.
43	VDDA	PWR	3.3V power for the PLL core.
44	Reset#	OUT	Real time system reset signal for frequency gear ratio change or watchdog timer timeout. This signal is active low.
45	REF2/FS2*	I/O	14.318 MHz reference clock / Frequency select latch input pin.
46	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
47	GND	PWR	Ground pin.
48	REF1/FS1*	I/O	14.318 MHz reference clock / Frequency select latch input pin.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ 1.5X Drive Strength

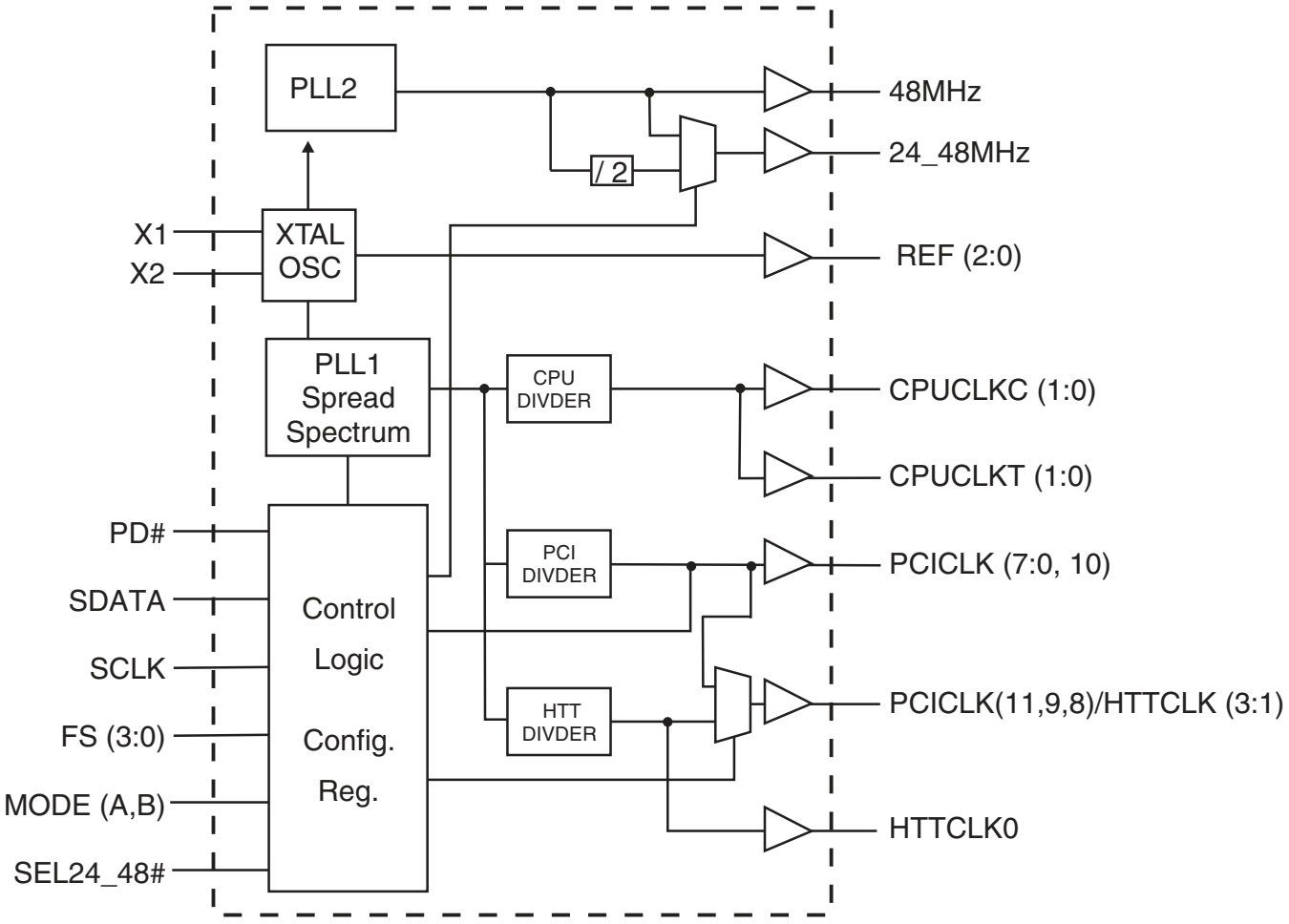
0802F—04/22/05

General Description

The **ICS950405** is a main system clock solution for desktop designs using the AMD K8 CPU. It provides all necessary clock signals for Clawhammer and Sledgehammer with AMD, VIA or ALI systems.

The **ICS950405** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
2	5	Xtal, POR
9	10	PCICLK, HTTCLK O/p
16,19	15,20	PCICLK Outputs
29	27,30,33	48 MHz, Fix Analog
35,38	34,39	CPU Outputs
43	42	Analog, CPU PLL, MCLK
46	47	REF, Digital Core

Mode Functionality Tables

ModeA	ModeB	Pin7	Pin8	Pin11
0	0	HTTCLK1	HTTCLK2	PCICLK11
0	1	HTTCLK1	HTTCLK2	HTTCLK3
1	0	PCICLK8	PCICLK9	PCICLK11
1	1	HTTCLK1	PCICLK9	PCICLK11

Table1: Frequency Selection Table

Bit3	Bit2	Bit1	Bit0	CPU	HTT	PCI
FS3	FS2	FS1	FS0	MHz	MHz	MHz
0	0	0	0	100.90	67.27	33.63
0	0	0	1	133.90	66.95	33.48
0	0	1	0	168.00	67.20	33.60
0	0	1	1	202.00	67.33	33.67
0	1	0	0	100.20	66.80	33.40
0	1	0	1	133.50	66.75	33.38
0	1	1	0	166.70	66.68	33.34
0	1	1	1	200.40	66.80	33.40
1	0	0	0	150.00	60.00	30.00
1	0	0	1	180.00	60.00	30.00
1	0	1	0	210.00	70.00	35.00
1	0	1	1	240.00	60.00	30.00
1	1	0	0	270.00	67.50	33.75
1	1	0	1	233.33	66.67	33.33
1	1	1	0	266.67	66.67	33.33
1	1	1	1	300.00	75.00	37.50

General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
	X Byte		Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS_EN	Spread Enable	RW	OFF	ON	1
Bit 6	-	SEL24_48MHz	Output Select	RW	48MHz	24MHz	Latch
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 3	-	FS3	Freq Select Bit 3	RW	See Table1: Frequency Selection Table		Latch
Bit 2	-	FS2	Freq Select Bit 2	RW			Latch
Bit 1	-	FS1	Freq Select Bit 1	RW			Latch
Bit 0	-	FS0	Freq Select Bit 0	RW			Latch

I²C Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	1	REF0	Output Control	RW	Disable	Enable	1
Bit 6	6	HTTCLK0	Output Control	RW	Disable	Enable	1
Bit 5	7	PCICLK8/HTTCLK1	Output Control	RW	Disable	Enable	1
Bit 4	8	PCICLK9/HTTCLK2	Output Control	RW	Disable	Enable	1
Bit 3	11	PCICLK11/HTTCLK3	Output Control	RW	Disable	Enable	1
Bit 2	12	PCICLK10	Output Control	RW	Disable	Enable	1
Bit 1	13	PCICLK0	Output Control	RW	Disable	Enable	1
Bit 0	14	PCICLK1	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	17	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 6	18	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 5	21	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 4	22	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 3	23	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 2	24	PCICLK7	Output Control	RW	Disable	Enable	1
Bit 1	28	24_48MHz	Output Control	RW	Disable	Enable	1
Bit 0	31	48MHz	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	37,36	CPUCLK8T/C_1	Output Control	RW	Disable	Enable	1
Bit 6	41,40	CPUCLK8T/C_0	Output Control	RW	Disable	Enable	1
Bit 5	45	REF2	Output Control	RW	Disable	Enable	1
Bit 4	48	REF1	Output Control	RW	Disable	Enable	1
Bit 3	-	PCI_Str1	PCI9,8 Strength Control only	RW	00: 0.5X Drive	10: 1.5X Drive	0
Bit 2	-	PCI_Str0		RW	01: 1.0X Drive	11: 2.0X Drive	1
Bit 1	-	PCI_Str1	PCI11 Strength Control only	RW	00: 0.5X Drive	10: 1.5X Drive	0
Bit 0	-	PCI_Str0		RW	01: 1.0X Drive	11: 2.0X Drive	1

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIStr1	All other PCICLK Strength Control	RW	00: 0.5X Drive	10: 1.5X Drive	0
Bit 6	-	PCIStr0		RW	01: 1.0X Drive	11: 2.0X Drive	1
Bit 5	-	PCIStr1	PCICLK (7:6) Strength Control	RW	00: 0.5X Drive	10: 1.5X Drive	1
Bit 4	-	PCIStr0		RW	01: 1.0X Drive	11: 2.0X Drive	1
Bit 3	-	PCIStr1	PCICLK (5) Strength Control	RW	00: 0.5X Drive	10: 1.5X Drive	1
Bit 2	-	PCIStr0		RW	01: 1.0X Drive	11: 2.0X Drive	1
Bit 1	-	PCIStr1	PCICLK (4) Strength Control	RW	00: 0.5X Drive	10: 1.5X Drive	1
Bit 0	-	PCIStr0		RW	01: 1.0X Drive	11: 2.0X Drive	1

I²C Table: Reserved Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 6	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 5	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 4	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 3	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 2	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 1	-	Reserved	Reserved	RW	Reserved	Reserved	X
Bit 0	-	Reserved	Reserved	RW	Reserved	Reserved	X

I²C Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Byte Count Programming b(7:0)	RW	Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes.		0
Bit 6	-	BC6		RW			0
Bit 5	-	BC5		RW			0
Bit 4	-	BC4		RW			0
Bit 3	-	BC3		RW			0
Bit 2	-	BC2		RW			1
Bit 1	-	BC1		RW			1
Bit 0	-	BC0		RW			0

I²C Table: Byte Count and Vendor ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	REV_ID3	Revision ID	RW	-	-	0
Bit 6	-	REV_ID2		RW	-	-	0
Bit 5	-	REV_ID1		RW	-	-	0
Bit 4	-	REV_ID0		RW	-	-	0
Bit 3	-	Vendor_ID3	Vendor ID	RW	-	-	0
Bit 2	-	Vendor_ID2		RW	-	-	0
Bit 1	-	Vendor_ID1		RW	-	-	0
Bit 0	-	Vendor_ID0		RW	-	-	1

I²C Table: Skew Control Register

Byte 8	Pin #	Name	Control Function	Type	0		1		PWD
Bit 7	-	PCI/HTTSkw3	CPU-PCI/HTT 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 6	-	PCI/HTTSkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 5	-	PCI/HTTSkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 4	-	PCI/HTTSkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0
Bit 3	-	PCISkw3	CPU-PCI 7 Step Skew Control (ps)	RW	0000:0	0100:150	1000:300	1100:450	1
Bit 2	-	PCISkw2		RW	0001:N/A	0101:N/A	1001:N/A	1101:600	1
Bit 1	-	PCISkw1		RW	0010:N/A	0110:N/A	1010:N/A	1110:750	0
Bit 0	-	PCISkw0		RW	0011:N/A	0111:N/A	1011:N/A	1111:900	0

I²C Table: WD Time Control & Async Frequency Selection Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	ASEL	Async Frequency Select	RW	66MHz	75.4MHz	0
Bit 6	-	AEN	AGP/PCI/ Freq Source Select	RW	FIX PLL	CPU PLL	1
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	Reserved	Reserved	RW	-	-	X
Bit 3	-	WDTCtrl	Watch Dog Time base Control	RW	290ms Base	1160ms Base	0
Bit 2	-	WD2	WD Timer Bit 2	RW	These bits represent X*290ms (or 1.16S) the watchdog timer waits before it goes to alarm mode. Default is 7 X 290ms = 2s.		1
Bit 1	-	WD1	WD Timer Bit 1	RW			1
Bit 0	-	WD0	WD Timer Bit 0	RW			1

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WDEN	Watchdog Enable	RW	Disable	Enable	0
Bit 5	-	WDStatus	WD Alarm Status	R	Normal	Alarm	0
Bit 4	-	WD SF4	Watch Dog Safe Freq Programming bits	RW	Writing to these bit will configure the safe frequency as Byte0 bit (4:0).		0
Bit 3	-	WD SF3		RW			0
Bit 2	-	WD SF2		RW			0
Bit 1	-	WD SF1		RW			0
Bit 0	-	WD SF0		RW			0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of N Divider in Byte 11 and 12		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits (5:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming bit (7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 14.318 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

Absolute Maximum Ratings

Supply Voltage 3.8V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +3.8 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

ESD Protection . . . . . Input ESD protection usung human body model > 1KV

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD(op)}$	C_L = 0 pF; Select @ 100MHz			180	mA
Power Down Supply Current	I_{DDPD}	C_L = 0 pF; With input address to Vdd or GND			40	mA
Input frequency	F_i	V_{DD} = 3.3 V;	11		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V	1.5		4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - K8 Push Pull Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =AMD64 Processor Test Load

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Rate	$\delta V/\delta t$	Measured at the AMD64 processor's test load. 0 V +/- 400 mV (differential	2		10	V/ns	1
Falling Edge Rate	$\delta V/\delta t$		2		10	V/ns	1
Differential Voltage	V_{DIFF}	Measured at the AMD64 processor's test load. (single-ended measurement)	0.4		2.3	V	1
Change in V_{DIFF_DC} Magnitude	ΔV_{DIFF}		-150		150	mV	1
Common Mode Voltage	V_{CM}		1.05		1.45	V	1
Change in Common Mode Voltage	ΔV_{CM}		-200		200	mV	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom. Maximum difference of cycle time between 2 adjacent cycles.	0		200	ps	1
Jitter, Accumulated	t_{ja}	Measured using the JIT2 software package with a Tek 7404 scope. TIE (Time Interval Error) measurement technique: Sample resolution = 50 ps, Sample Duration = 10 µs	-1000		1000		1,2,3
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45		53	%	1
Output Impedance	R_{ON}	Average value during switching transition. Used for determining series termination value.	15		55	Ω	1
Group Skew	$t_{src-skew}$	Measurement from differential wavefrom			250	ps	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All accumulated jitter specifications are guaranteed assuming that REF is at 14.31818MHz

[3] Spread Spectrum is off

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V,+/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps
	t_{jabs1}	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - ZCLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

Electrical Characteristics - AGPCLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5		2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5		2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45		55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66			250	ps

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V			1000	ps
	t_{jabs5}	V_T = 1.5 V			800	ps

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS950405 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

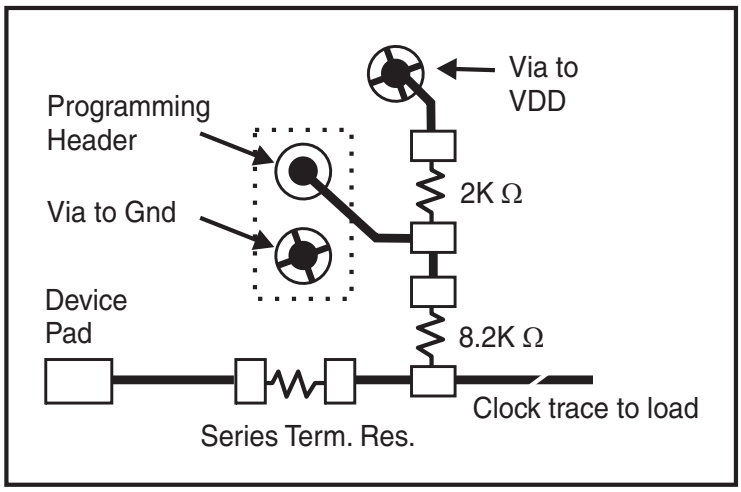
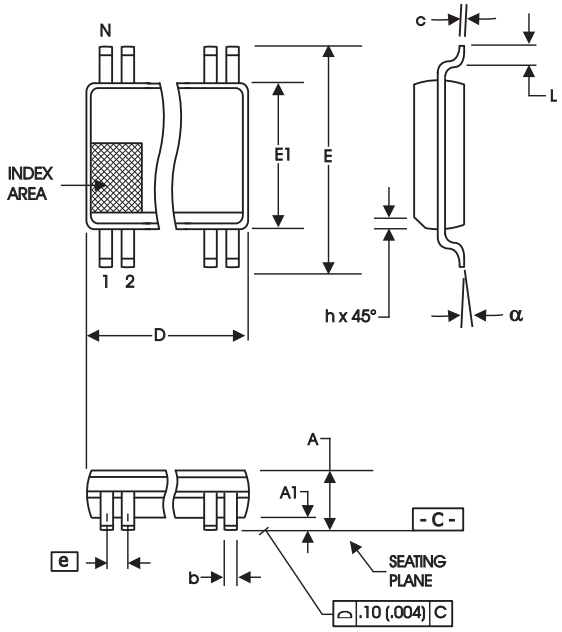


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950405yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0802F—04/22/05

Revision History

Rev.	Issue Date	Description	Page #
0.1	4/21/2005	Updated Byte 11/12 M/N programming description	8-9