

# Am78C200

## InterWave™ LC Interactive Audio and Wavetable Solution Family

### DISTINCTIVE CHARACTERISTICS

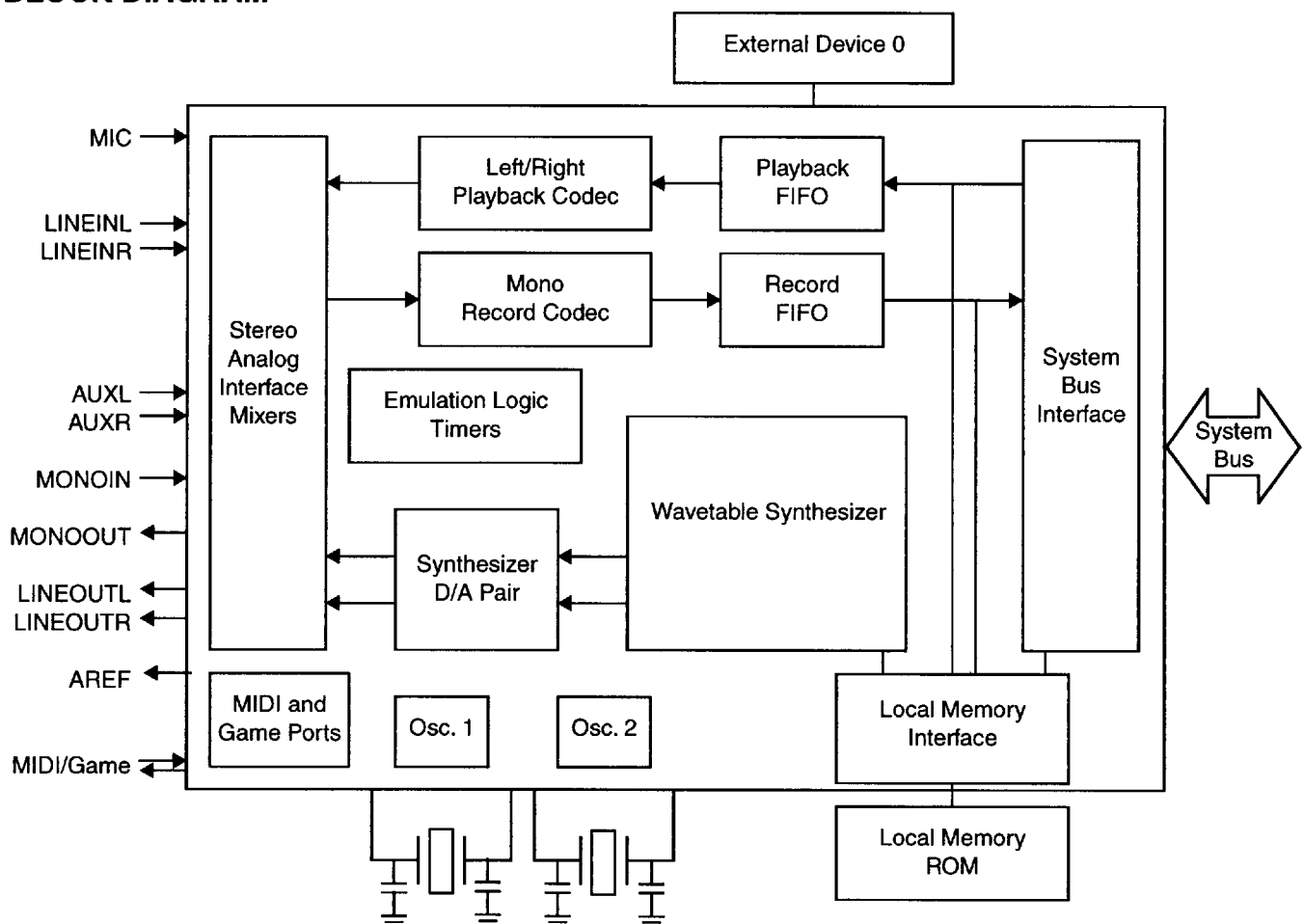
- 32-voice stereo wavetable synthesizer
- Up to 32 channels of digital mixing
- 16-bit audiophile codec with IMA ADPCM 4:1 compression/decompression
- MPC-compliant analog mixer
- ISA plug and play
- MIDI and game ports
- Power management

### Supports multiple standards:

- Compatible with Sound Blaster applications
- MPU-401
- MPC2, MPC3
- General MIDI
- Microsoft® Windows®95, DirectSound™\*
- Windows 3.x API, Win32 API\*
- Miles AIL API\*
- HMI SOS API\*
- Lucas Arts iMUSE API\*

\* Appropriate software drivers required

### BLOCK DIAGRAM



## **GENERAL DESCRIPTION**

The InterWave LC audio IC provides a complete audio subsystem that meets all major business and entertainment audio standards. The Am78C200 device integrates a 32-voice stereo wavetable synthesizer, a 16-bit stereo audiophile codec and audio mixer, both MIDI and game ports, and legacy FM sound card emulation hardware into a single 160-pin ISA Plug and Play compliant device.

### **Analog Interface, Mixers**

The Am78C200 device includes mono microphone, stereo and mono analog inputs, and, stereo auxiliary input. These signals are combined with the outputs of the left and right playback codecs to produce the outputs. The gain of each of these channels is controlled by internal registers that are loaded through the system bus interface.

### **Playback and Record Codec**

The full duplex 16-bit audiophile codec is a register compatible super-set of the CS4231 and AD1848. The codec provides independently programmable sample rates for the stereo playback and mono record paths, a variety of data types and compression schemes, on board 16-sample playback and record FIFOs.

### **Wavetable Synthesizer**

The wavetable synthesizer offers thirty-two, 16-bit stereo voices, all running at a 44.1 kHz frame rate. Each voice supports address generation, envelope generation, and enough voice processing power to support panning, volume control, and frequency shift of any combination of the thirty-two synthesizer voices which can be used to play or mix digital audio files.

The IC supports up to 16Mbytes of ROM. Wavetable patches can be 8-bit, 16-bit or 8-bit  $\mu$ -law compression.

The stereo digital output of the synthesizer is converted into analog form by two on-chip 16-bit digital-to-analog converters (DACs).

## **Bus Interface**

The bus interface of the Am78C200 device is fully compliant with the Plug and Play standard with no external logic. The Plug and Play interface can be either an 8-bit or a 16-bit ISA interface. The IC supports one (1) external device to the ISA bus through the Plug and Play interface.

## **Local Memory Interface**

The local memory control module (LMC) transfers data between local memory, the system bus interface, and the codec. Local memory can include up to four banks of ROM. The IC contains support for implementing external serial EEPROM that in turn supports the Plug and Play interface.

## **MIDI and Game Ports**

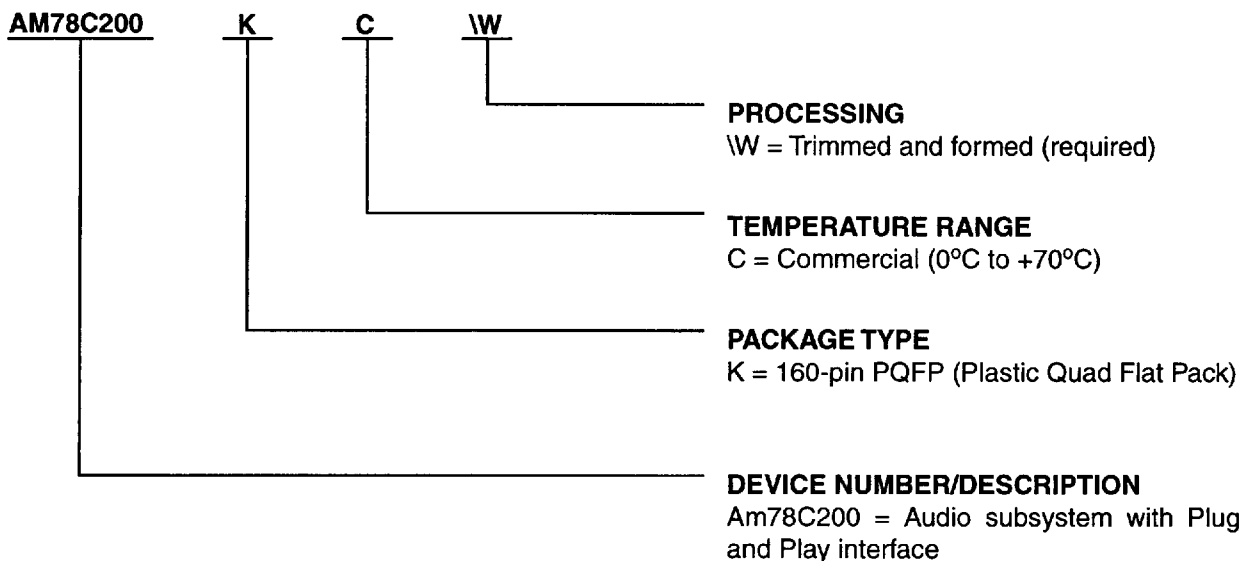
The MIDI (Musical Instrument Digital Interface) port provides data to a user-supplied external interface between the InterWave LC IC and a MIDI-compatible Local Area Network (LAN). The MIDI port is built around a UART with a 16-byte receive FIFO.

The game port of the InterWave LC IC provides the functions found in standard game ports in PCs. The Am78C200 device supports connection of up to two joysticks with a total of four buttons. Trim DACs are provided to adjust the offset voltage for calibration.

## ORDERING INFORMATION

### Standard Products

AMD® standard products are available in several operating ranges and functionality. The order numbers (Valid Combination) are formed by a combination of the elements below.



Valid Combinations	
Am78C200	KC\W

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## PIN ASSIGNMENTS AND CONNECTION DIAGRAMS

The InterWave LC audio IC is packaged in a 160-pin plastic quad flat pack (PQFP) (Am78C200). Figure 1 shows the package layout and Table 1 lists the pin assignments. AVCC and AVSS are analog power and ground pins; VCC and VSS are digital power and ground pins. The NC pins are no connects and must be left unconnected.

# CONNECTION DIAGRAM

## 160 Pin Top View

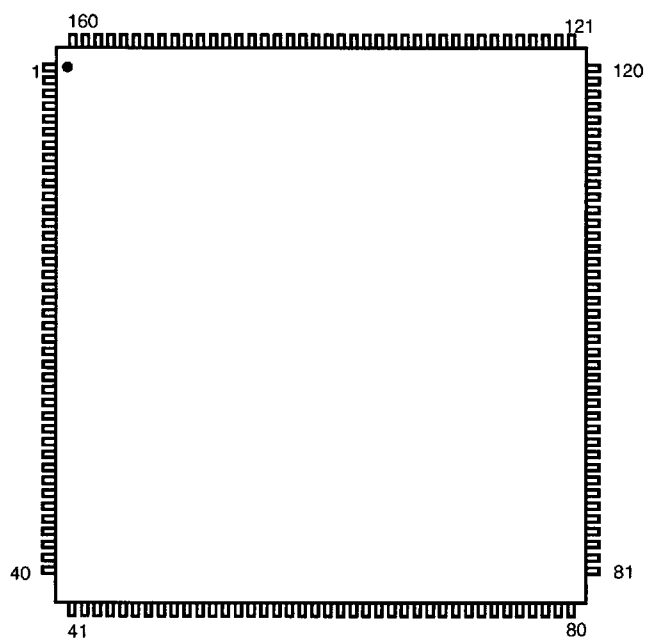


Table 1. Pin Assignments

160 Pin	Signal Name	Note	160 Pin	Signal Name	Note	160 Pin	Signal Name	Note	160 Pin	Signal Name	Note
1	SA7		41	EX_DRQ		81	MD7		121	SD11	
2	SA8		42	GAMIN3		82	VCC		122	SD10	
3	GPOUT0		43	GAMIN2		83	DRQ7		123	SD9	
4	RESET		44	GAMIN1		84	DAK7		124	SD8	
5	GPOUT1		45	GAMIN0		85	ROMCS		125	TC	
6	VCC		46	GAMIO3		86	RAHLD		126	DRQ1	
7	AVSS		47	GAMIO2		87	NC	1	127	DAK1	
8	AVSS		48	GAMIO1		88	NC	1	128	AEN	
9	IREF		49	GAMIO0		89	RA20		129	IOCHRDY	
10	CFILT		50	VSS		90	RA21		130	IRQ2/9	
11	AVSS		51	VSS		91	VCC		131	IRQ3	
12	AVCC		52	MA0		92	IRQ15		132	IOF	
13	AREF		53	MA1		93	IRQ12		133	VSS	
14	RESERVE0	2	54	EX_DAK		94	BKSEL0		134	VCC	
15	MIC		55	VCC		95	BKSEL1		135	IOW	
16	RESERVE1	4	56	MA2		96	VSS		136	IOCS16	
17	RESERVE2		57	MA3		97	BKSEL2		137	SD0	
18	RESERVE3	4	58	MA4		98	BKSEL3		138	SD1	
19	RESERVE4	2	59	MA5		99	IRQ11		139	SD2	
20	RESERVE5	3	60	EX_IRQ		100	XTAL1I		140	SD3	
21	AUXR		61	EX_CS		101	XTAL1O		141	VSS	
22	LINEINR		62	VSS		102	VSS		142	SD4	
23	AVSS		63	MA6		103	XTAL2O		143	SD5	
24	LINEINL		64	MA7		104	XTAL2I		144	SD6	
25	AUXL		65	MA8		105	VCC		145	SD7	
26	AVCC		66	MA9		106	MIDIRX		146	VCC	
27	LINEOUTR		67	MA10		107	MIDITX		147	VSS	
28	AVSS		68	DAK5		108	RESERVE6	6	148	IRQ5	
29	LINEOUTL		69	MD0		109	SUSPEND		149	IRQ7	
30	MONOOUT		70	MD1		110	VSS		150	IOCHK	
31	MONOIN		71	MD2		111	SBHE		151	SA0	
32	AVSS		72	MD3		112	DRQ0		152	SA1	
33	AVCC		73	VSS		113	DAK0		153	SA2	
34	AVSS		74	DRQ5		114	VCC		154	SA3	
35	PNPCS		75	VCC		115	VCC		155	SA4	
36	SA9		76	DAK6		116	SD15		156	SA5	
37	SA10		77	DRQ6		117	SD14		157	VSS	
38	SA11		78	MD4		118	SD13		158	DRQ3	
39	VCC		79	MD5		119	SD12		159	DAK3	
40	VSS		80	MD6		120	VSS		160	SA6	

**Notes:**

1. NC are no connects. There should be no electrical connections made to these pins.
2. RESERVE0 and RESERVE4 must have a 0.1  $\mu$ f capacitor to AVSS.
3. RESERVE5 must be connected to pin 15.
4. RESERVE1 and RESERVE3 must connect to AVSS.
5. RESERVE2 must connect to AVCC.
6. RESERVE6 must be attached to a 10 k $\Omega$  resistor to DVCC.

**PIN SUMMARY**
**Table 2. Am78C200 Pin Designations**

System Control		Codec		Local Memory		Ports, Crystals	
Pin Name	# Pins	Pin Name	# Pins	Pin Name	# Pins	Pin Name	# Pins
SD15–SD0	16	MIC	1	MA10–MA0	11	XTAL1I	1
SA11–SA0*	12	AUX[L,R]	2	MD7–MD0	8	XTAL1O	1
SCS[1,0], SA[3;0]		LINEIN[L,R]	2	BKSEL[3;0]	4	XTAL2I	1
SBHE	1	LINEOUT[L,R]	2	ROMCS	1	XTAL2O	1
DRQ[7,6,5,3,1,0]	6	MONOIN	1	RAHLD	1	MIDIRX	1
DAK[7,6,5,3,1,0]	6	MONOOUT	1	RA21–RA20	2	MIDITX	1
TC	1	IREF	1			GAMIN[3;0]	4
IRQ[15,12,11]	3	CFILT	1			GAMIO[3;0]	4
IRQ[7,5,3,2/9]	4	AREF	1				
IRQ10, IRQ4*	2→	GPOUT[1;0]					
IOCHK	1						
IOR	1						
IOW	1						
IOCS16	1						
IOCHRDY	1						
AEN	1						
EX_IRQ	1						
EX_DRQ	1						
EX_DAK	1						
EX_CS	1						
RESET	1						
					1	SUSPEND	
RESERVED[0;6]	7						
PNPCS	1						
NC	2						
Power & Ground	34						

**Notes:**

- \* These pins have multiple functions as indicated.
- This arrow identifies the common pin.

## PIN DESCRIPTIONS BY FUNCTIONAL GROUP

Table 3 through Table 8 lists pins by function and describes each pin.

Table 3. System Bus Interface Pins

Pin Name	Pin No.	Type	Description
AEN	128	I, T	<b>Address Enable</b> from the ISA bus, used to distinguish between DMA and I/O cycles. This signal must be driven Low when the bus performs an I/O access to the IC.
DAK0, DAK1, DAK3, DAK5, DAK6, DAK7	113, 127, 159, 68, 76, 84	I, T	The selectable <b>DMA Acknowledge</b> lines from the ISA bus. DAK0, DAK1, and DAK3 are used for 8-bit DMA transfers, and DAK5, DAK6, and DAK7 are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
DRQ0, DRQ1, DRQ3, DRQ5, DRQ6, DRQ7	112, 126, 158, 74, 77, 83	3S, T	The selectable <b>DMA Request</b> lines to the ISA bus. DRQ0, DRQ1, and DRQ3 are used for 8-bit DMA transfers, and DRQ5, DRQ6, and DRQ7 are used for 16-bit DMA transfers. The device can select up to three of the six supported DMA channels; the allocation of DMA channels is fully programmable using the Plug and Play registers.
IOCHRDY	129	OD, T	<b>I/O Channel Ready</b> to the ISA bus is used to extend the I/O bus cycle when deasserted. IOCHRDY High indicates that the device is ready to complete the current I/O bus cycle.
IOCS16	136	OD, T	<b>I/O Chip Select 16</b> is asserted Low by the device during an I/O Read or Write operation to indicate that a 16-bit port is supported at the current address.
IOR	132	I, T	<b>I/O Read</b> on the ISA bus is driven Low by the host to indicate that an input/output Read operation is taking place. IOR is valid only if the AEN signal is also Low.
IOW	135	I, T	<b>I/O Write</b> on the ISA bus is driven Low by the host to indicate that an input/output Write operation is taking place. IOW is valid only if the AEN signal is also Low.
IRQ2/9, IRQ3, IRQ5, IRQ7, IRQ11, IRQ12, IRQ15	130, 131, 148, 149, 99, 93, 92	3S, T	The selectable <b>Interrupt Requests</b> to the ISA bus. The device can select up to three of the nine supported interrupts; the allocation of interrupt signals is fully programmable using the Plug and Play registers. Internally, interrupt sources can be assigned to the available interrupt request signals as required by software.
IRQ4, IRQ10	3, 5	3S, C	See description for <b>Interrupt Requests</b> . These pins are multiplexed with GPOUT0 and GPOUT1. IRQ4 and IRQ10 are selected by IEIRQI[7] = 0 (EX_DAK = 0 at reset). See the <i>InterWave IC Programmer's Guide</i> .
IOCHK	150	OD, T	<b>I/O Check</b> . Channel or I/O channel check on the ISA bus. IOCHK is asserted Low by the device to generate an NMI (non-maskable interrupt).
PNPCS	35	B, T	<b>Plug and Play Serial EEPROM Chip Select</b> . Active High output used as chip select for the Plug and Play serial EEPROM. This is an input during reset; its state is latched by the trailing edge of reset to determine whether the IC is in PNP-compliant mode (Low) or in PNP-system mode (High).
RESET	4	I, T	<b>Reset</b> from the ISA bus. When RESET is asserted High on the ISA bus, the device performs an internal system reset. The RESET pin must be asserted for at least 10 ms before being deasserted. While in the reset state, the device ignores all ISA bus activity and no local memory cycles take place. On the trailing edge of RESET, the state of some I/O pins are latched to determine the configuration of certain multifunction pins.
SBHE	111	I, T	The <b>System Byte High Enable</b> signal indicates the High byte of the system data bus is to be used. When connecting to an 8-bit ISA bus, this pin must be disconnected.
SA11-SA6	38-36, 2, 1, 160	I, T I, T	<b>System Address Bus</b> . During Internal Decoding mode, these inputs are the 12 lower lines of the ISA System Address Bus which are used along with AEN to generate decodes for internal device resources.

Table 3. System Bus Interface Pins (continued)

Pin Name	Pin No.	Type	Description
SD15–SD0	116–119, 121–124, 145–142, 140–137	B, T	The ISA <b>System Data Bus</b> is used to transfer data to and from the device. The entire data bus, SD15–SD0, is active during 16-bit I/O access. During 8-bit I/O accesses, the lower data bus, SD7–SD0, is active when accessing an even byte, and the upper data bus, SD15–SD8, is active when accessing an odd byte.
TC	125	I, T	<b>Transfer Complete</b> or <b>Terminal Count</b> is driven active High by the master or slave DMAC when the word or byte transfer count for a DMA channel is complete.

**Note:**

Pin Type: A = analog signal, B = digital bidirectional, C = CMOS compatible, I = digital input, O = digital output, OD = digital open drain output, P = power or ground, T = TTL compatible, 3S = digital 3-state output

Table 4. Codec/Mixer Pins

Pin Name	Pin No.	Type	Description
AREF	13	A	The <b>Analog Reference</b> pin provides a reference voltage which can be used by external amplifier circuitry. When VCC is at +5.0 V, the value of this output pin is 0.376 times supply. See the <i>InterWave IC Programmer's Guide</i> .
AUXL, AUXR	25, 21	A	The <b>Stereo Auxiliary Inputs</b> can always be independently mixed or muted. Typically, these inputs are used for mixing analog stereo audio. The AUX input impedance is at least 20 k $\Omega$ .
CFILT	10	A	The <b>Capacitor Filter</b> input must be connected to analog ground through a 0.1 $\mu$ F capacitor and a 10 $\mu$ F capacitor.
IREF	9	A	The Current Reference input pin must be connected to analog ground through a 61.9 k $\Omega$ 1% tolerance resistor.
LINEINL, LINEINR	24, 22	A	The <b>Stereo Line Inputs</b> can always be independently mixed or muted. These inputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these inputs are used for mixing or recording analog audio from a variety of external audio sources. The LINEIN input impedance is at least 20 k $\Omega$ .
LINEOUTL, LINEOUTR	29, 27	A	The <b>Stereo Line Outputs</b> are stereo single-ended line drivers which can drive 5 k $\Omega$ loads. These outputs are the sum of the left and right mixer channels respectively. The LINEOUTs can be independently attenuated or muted and these mixer outputs can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, these outputs are used for driving powered speakers or connected to speaker or headphone drivers.
MIC	15	A	The <b>Microphone Input</b> can be independently mixed or muted. This input can also be selected for analog-to-digital conversion through the Record Multiplexer. Typically, this input is used for mixing or recording a preamplified signal from a microphone. The MIC input impedance is at least 10 k $\Omega$ .
MONOIN	31	A	The <b>Mono Input</b> can always be independently mixed or muted and feeds both the left and right mixer output paths. Typically, this input is used for mixing PC speaker audio. The MONOIN input impedance is at least 20 k $\Omega$ .
MONOOUT	30	A	The <b>Mono Output</b> is a single-ended line driver which can drive a 5 k $\Omega$ load. It provides the sum of the left and right LINEOUT signals and is independently mutable. Typically, this output is connected to a speaker driver for a PC speaker.



Table 5. Local Memory Controller Pins

Pin Name	Pin No.	Type	Description
$\overline{\text{BKSEL0}}$ , $\overline{\text{BKSEL3}}$	94, 95, 97, 98	O, C	The <b>Bank Select</b> signals are used to control the Output Enable input of each ROM bank.
MA3–MA10	57–59, 63–67	B, C	The <b>Memory Address</b> signals are time-multiplexed ROM access cycles for ROM Latched Address[10:3] outputs and ROM High Byte Data Bus[15:8] inputs. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal.
MA0–MA2	52, 53, 56	O, C	<b>Memory address.</b> RLA[2,1,19] outputs for ROM access cycles.
MD7–MD0	69–72, 78–81	B, C	The <b>Memory Data Bus</b> for ROM access cycles are time-multiplexed ROM Latched Address[18:11] outputs and ROM Low Byte Data Bus[7:0]. The ROM Latched Addresses must be latched externally using the $\overline{\text{RAHLD}}$ signal. For Plug and Play Serial EEPROM accesses, MD[2] is the Serial Data Clock (SK), MD[1] is the Serial Data Input (DI), and MD[0] is the Serial Data Output (DO).
RA20–RA21	89, 90	B, C	High <b>ROM Address</b> lines during ROM accesses. At the trailing edge of RESET, these signals become inputs that are used to determine the operation mode of certain multiplexed function pins.
$\overline{\text{RAHLD}}$	86	O, C	The <b>ROM Address Hold</b> output is used to latch the state of ROM Latched Address lines MD[7:0] (RLA[18:11]) and MA[10:3] (RLA[10:3]) in external latches during ROM accesses.
ROMCS	85	O, C	The <b>ROM Chip Select</b> output is asserted Low during ROM accesses, and is connected directly to the Chip Select/Enable input of each ROM in all of the ROM banks.

Table 6. Additional Function Pins

Pin Name	Pin No.	Type	Description
GPOUT0, GPOUT1	3, 5	3S, T	The <b>General Purpose Digital Outputs</b> are two general purpose digital outputs controlled by bits located in the External Control (CEXTI) register. These pins are multiplexed with IRQ4 and IRQ10. GPOUT0 and GPOUT1 are selected by IEIRQI[7] = 1 ( $\overline{\text{EX\_DAK}}$ = 1 at reset). See the <i>InterWave IC Programmer's Guide</i> .
EX_CS	61	B, T	The <b>External Device Chip Select</b> consisting of the decode of AEN deasserted (Low) and the address specified in the PNP CD-ROM address High/Low (PRAHI and PRALI) registers. The state of this pin on the falling edge of RESET determines if the device will decode SA[11:0] on all ports, or decode SA[9:0] on all ports (except the PNP ports).
EX_DAK	54	B, T	The <b>External Device DMA Acknowledge</b> output to the external device. The state of this pin on the falling edge of RESET configures the device to utilize the GPOUT[1:0] pins as IRQ[10,4] if held Low at RESET; or, the device can be configured to select the GPOUT[1:0] to be decode flags if held High at RESET.
EX_DRQ	41	I, T	<b>External Device DMA Request.</b>
EX_IRQ	60	O, T	<b>External Device Interrupt Request.</b>
SA5–SA0/ SCS1–SCS0, SA3–SA0	156–151	I, T I, T	During External Decoding mode, the System Address Bus is redefined as follows: SA[11:6] are not used, SA[5:4] are redefined as <b>System Chip Selects</b> (SCS[1:0]), and the lower address lines SA[3:0] are unchanged. The decoding mode is determined by the state of RA[20] at the trailing edge of the RESET signal. If RA[20] is Low at the trailing edge of RESET, Internal Decoding mode is selected; if RA[20] is High, External Decoding mode is selected.

Table 6. Additional Function Pins (continued)

Pin Name	Pin No.	Type	Description
SUSPEND	109	I, C	When the <b>Suspend</b> input is asserted Low, all chip activity becomes frozen, the oscillators are turned off, and most of the ISA bus inputs and outputs are isolated from the IC.  The operation mode of this pin is determined by the state of RA[21] at the trailing edge of the RESET signal. If RA[21] is High at the trailing edge of RESET, the SUSPEND input function is selected.
NC	87, 88		These pins are No Connects. There must be no traces attached to these pins.
RESERVED[0;6]	14,16,17, 18,19,20, 108		Please refer to Table 1 Pin Assignments.

Table 7. Game and MIDI Port Pins, Crystal Pins

Pin Name	Pin No.	Type	Description
GAMIN3– GAMIN0	42–45	I, C	The <b>Game Inputs</b> are used to monitor the state of buttons on external joystick(s). The state of these inputs can be read from the Game Control (GGCR) register. These pins are internally pulled up through a nominal 6 kΩ resistance.
GAMIO3– GAMIO0	46–49	A	The <b>Game I/O</b> pins are used to determine the state of potentiometers on an external joystick to obtain the joystick's X-Y position.
MIDITX	107	B	The <b>MIDI Transmit</b> output is used to send serial digital data from the internal Motorola MC6850-compatible UART.
MIDIRX	106	I	The <b>MIDI Receive</b> input is used to receive serial digital data into the internal Motorola MC6850-compatible UART.
XTAL1I	100		<b>Crystal 1 Input.</b> Input from the 24.576 MHz crystal. The clock used by the codec module to support select sampling rates is derived from the 24.576 MHz crystal attached to the XTAL1 pins. An external 24.576 MHz CMOS-compatible clock is not supported.
XTAL1O	101		<b>Crystal 1 Output.</b> Output from the 24.576 MHz crystal.
XTAL2I	104		<b>Crystal 2 Input.</b> Input from the 16.9344 MHz crystal. The main clocks used throughout the IC are derived from the 16.9344 MHz crystal attached to the XTAL2 pins. An external 16.9344 MHz CMOS-compatible clock is not supported.
XTAL2O	103		<b>Crystal 2 Output.</b> Output from the 16.9344 MHz crystal.

Table 8. Power Supply Pins

Pin Name	Pin (200)	Type	Description
AVCC	12, 26, 33	P	<b>Analog Power.</b> Supplies power to analog portions of the InterWave LC IC.
VCC	6, 39, 55, 75, 82, 91, 105, 114, 115, 134, 146	P	<b>Digital Power.</b> Supplies power to digital portions of the InterWave LC IC.
AVSS	7, 8, 11, 23, 28, 32, 34	P	<b>Analog Ground.</b> Supplies ground reference to analog portions of the InterWave LC IC.
VSS	40, 50, 51, 62, 73, 96, 102, 110, 120, 133, 141, 147, 157	P	<b>Digital Ground.</b> Supplies ground reference to digital portions of the InterWave LC IC.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature . . . . . -65°C to +150°C  
 Ambient Temperature Under Bias . -65°C to +125°C  
 Supply Voltage VCC to VSS . . . . . -0.5 V to +7 V  
 All digital inputs within  
 the range . . . . . -0.5 V to VCC +0.5 V  
 All analog inputs within  
 the range . . . . . -0.5 V to AVCC +0.5 V  
 Supply voltage . . . . . AVCC to AVSS -0.5 V to +7 V  
 Supply voltage . . . . . VCC to AVCC ±0.5 V  
 Supply voltage . . . . . VSS to AVSS ±0.5 V

*Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.*

**OPERATING RANGES**

Ambient Temperature . . . . . 0°C to +70°C  
 VCC . . . . . 4.75 V to 5.25 V  
 AVCC . . . . . 4.75 V to 5.25 V

**ELECTRICAL CHARACTERISTICS over COMMERCIAL operating ranges****Table 9. DC Characteristics**

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
TTL-Compatible Input Voltage (VCC = 4.75 V to 5.25 V)						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.0		VCC +0.5	V
CMOS-Compatible Input Voltage (VCC = 4.75 V to 5.25 V)						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		3.7		VCC +0.5	V
Digital Output Voltage						
VOL	Output Low Voltage				0.5	V
VOH	Output High Voltage		2.4			V
Digital Leakage Current						
IIX	Input Leakage Current		-10		10	μA
IOZL	Output Low Leakage Current		-10			μA
IOZH	Output High Leakage Current				10	μA
Crystal Input						
FCK1	Crystal 1 Frequency			24.576		MHz
FCK2	Crystal 2 Frequency			16.9344		MHz
Power Supply Current						
	Total Operating Current (Digital and Analog)	Note 2		140	TBD	mA
	Analog Operating Current	Note 1		TBD	TBD	mA
	Digital, Suspend			TBD	TBD	μA

**Notes:**

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. All applicable output pins are three-stated.

Table 10. Maximum Drive Table For VOL and VOH Specifications, VCC = 5.0 V

Signals	Load Cap. (pF)	IOL (mA)	IOH (mA)	Notes
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	240	24	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	120	12	-3	1, 2
SD[15:0], IOCHRDY, $\overline{\text{IOCS16}}$ , $\overline{\text{IOCHK}}$	60	3	-3	1, 2
DRQ[7:5,3,1:0], IRQ[15,12,11,7,5,3,2], GPOUT[1:0]	120	5	-3	2
PNPCS, EX_CS, EX_DAK, EX_IRQ, MIDITX, RAHLD,	50	3	-3	3
MA[10:0], MD[7:0], BKSEL[3:0], $\overline{\text{ROMCS}}$ , RA[21:20]	120	3	-3	

**Notes:**

1. The maximum drive capability for these signals is selectable via programmable register. See the InterWave IC Programmer's Guide.
2. There is no IOH value for the open collector outputs.

Table 11. Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
<b>A/D</b>							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range			80		dB	
THD	Total Harmonic Distortion			0.02		%	
	Signal-to-Intermodulation Distortion			85		dB	1
	Offset Error				TBD	bits	1
	Gain Error				TBD	%	
<b>Mixer Inputs</b>							
	Full Scale Input Voltage			2.9		Vp-p	
	Input Resistance		20			k $\Omega$	1
	MIC Input Resistance		10			k $\Omega$	1
	Input Capacitance				15	pF	1
	Interchannel Isolation						
	Line-Line			75		dB	
	Line-Mic			75		dB	
	Line-Aux			75		dB	
	Interchannel Gain Mismatch				0.5	dB	
	Programmable Gain Range (CLICI)			22.5		dB	3
	Programmable Gain Step Size (CLICI)			1.5		dB	3
	Programmable Gain Range (CLOAI)			46.5		dB	3
	Programmable Gain Step Size (CLOAI)			1.5		dB	3
	Programmable Gain Range (CMONOI)			45.0		dB	3
	Programmable Gain Step Size (CMONOI)			1.5		dB	3

Table 11. Electrical Characteristics (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typical	Max	Unit	Notes
Mixer Outputs							
	Full Scale Output Voltage, OFVS = 1	measured at LINEOUT		2.9		Vp-p	
	Full Scale Output Voltage, OFVS = 0	measured at LINEOUT		2.0		Vp-p	
	External Load Impedance	LINEOUT, MONOOUT		5		k $\Omega$	2
	External Load Capacitance				100	pF	
	Audible Out-of-Band Energy 0.6 Fs to 20 kHz	measured at Fs = 8 kHz		-65		dB	1
	Mute Attenuation			75		dB	
	AREF Drive		-0.25		1.0	mA	
	AREF Level			1.88 V		V	
	Programmable Gain Range (CLCI, CLDACI)			94.5		dB	3
	Programmable Gain Step Size			1.5		dB	
	Line-to-Line Interchannel Isolation	measured at LINEOUT		75		dB	
	Interchannel Gain Mismatch				$\pm 0.5$	dB	
Synthesizer D/A							
	Resolution			16		bits	1
IDR	Instantaneous Dynamic Range			80		dB	
THD	Total Harmonic Distortion			0.01		%	
	Signal-to-Intermodulation Distortion			80		dB	1
	Gain Error		-0.5		0.5	dB	1
Codec D/A							
	Resolution			16		bits	
IDR	Instantaneous Dynamic Range			80			
THD	Total Harmonic Distortion			0.01	0.02	%	
	Signal-to-Intermodulation Distortion			80		dB	1
	Gain Error		-0.5		0.5	dB	
Game Port							
	Joystick Trim DAC Threshold				TBD	V	
	Joystick Trim DAC Step Size				TBD	V	

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. Outputs AC coupled.
3. See InterWave IC Programmer's Guide.

Table 12. Digital Filter Characteristics—Playback

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		$\pm 0.1$	dB	1
	Transition Band		0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		107	dB	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

Table 13. End-To-End Frequency Characteristics—Playback (Measured at LINEOUT)

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	$\pm 0.2$	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

Table 14. Digital Filter Characteristics—Record

Parameter Symbol	Parameter Description	Min	Max	Units	Notes
	Passband		0.45 Fs	Hz	1
	Passband Ripple		0.1	dB	1
	Transition Band		0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs		Hz	1
	Stopband Attenuation		-100	dB	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

Table 15. End-To-End Frequency Characteristics—Record

Parameter Symbol	Parameter Description	Typical	Units	Notes
	Passband	0.45 Fs	Hz	1
	Passband Ripple	$\pm 0.2$	dB	1
	Transition Band	0.1 Fs	Hz	1
	Stopband Frequency	0.55 Fs	Hz	1

**Notes:**

VCC = 5.0 V; Ambient temperature = 25°C; Sample Rate = 44.1 kHz; all attenuators = 0 dB; outputs measured from 20 Hz to 20 kHz.

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.

Table 16. Switching Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit	Notes
System Control						
$t_{AS}$	Address Setup		88		ns	
$t_{AH}$	Address Hold		32		ns	
$t_{AR}$	Address Recovery		152		ns	
$t_{SW}$	Read or Write Strobe Width		TBD		ns	
$t_{DDW}$	Data Delay (Write)			61	ns	
$t_{DHW}$	Data Hold (Write)			25	ns	
$t_{DDR}$	Data Delay (Read)			103	ns	
$t_{DHR}$	Data Hold (Read)		0		ns	
$t_{RD}$	Ready Delay			76	ns	
$t_{ID}$	I/O Delay			116	ns	
$t_{IDD}$	I/O Delay (Read)			59	ns	
ROM Read						
$t_{AS1}$	Address Setup Time (bits 19, 2, 1)		24		ns	2
$t_{AS2}$	Address Setup Time (bits 10–3)		55		ns	2
$t_{AS3}$	Address Setup Time (bits 18–11)		24		ns	2
$t_{AS4}$	Address Setup Time (bits 21–20)		24		ns	2
$t_{AH1}$	Address Hold Time (bits 19, 2, 1)		237		ns	2
$t_{AH2,3}$	Address Hold Time (bits 18–3)		80		ns	2
$t_{RC}$	Read Cycle Time		102		ns	2
$t_{DF}$	Output Disable Time		29		ns	2
$t_{ACE}$	Chip Enable Access Time			239	ns	
$t_{OE}$	Output Enable Access Time			161	ns	
$t_{RDS}$	Read Data Setup Time		58		ns	
$t_{RDH}$	Read Data Hold Time			70	ns	

**Notes:**

$V_{CC} = 5.0\text{ V}$ ; Ambient temperature =  $25^{\circ}\text{C}$ .

1. This parameter is not tested in production; it is guaranteed by characterization or by correlation to other tests.
2. XTAL2 frequency = 16.9344 MHz.

## FILTER RESPONSE

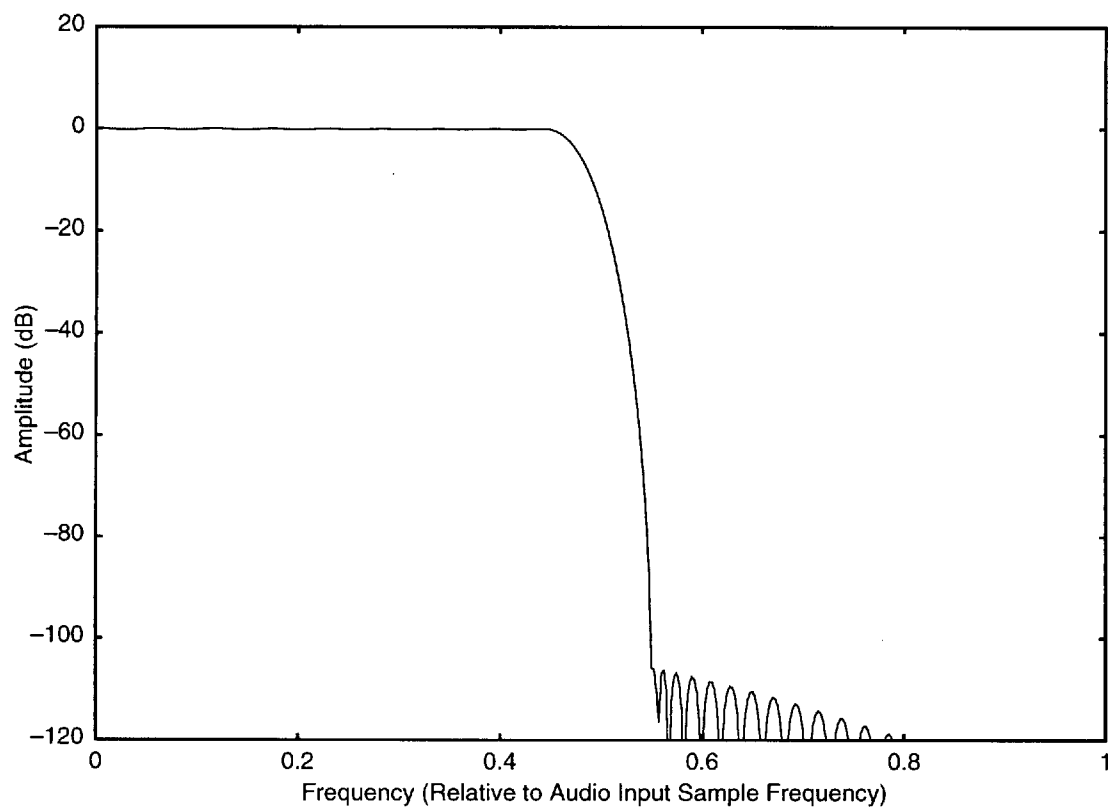


Figure 1. DAC Filter Response

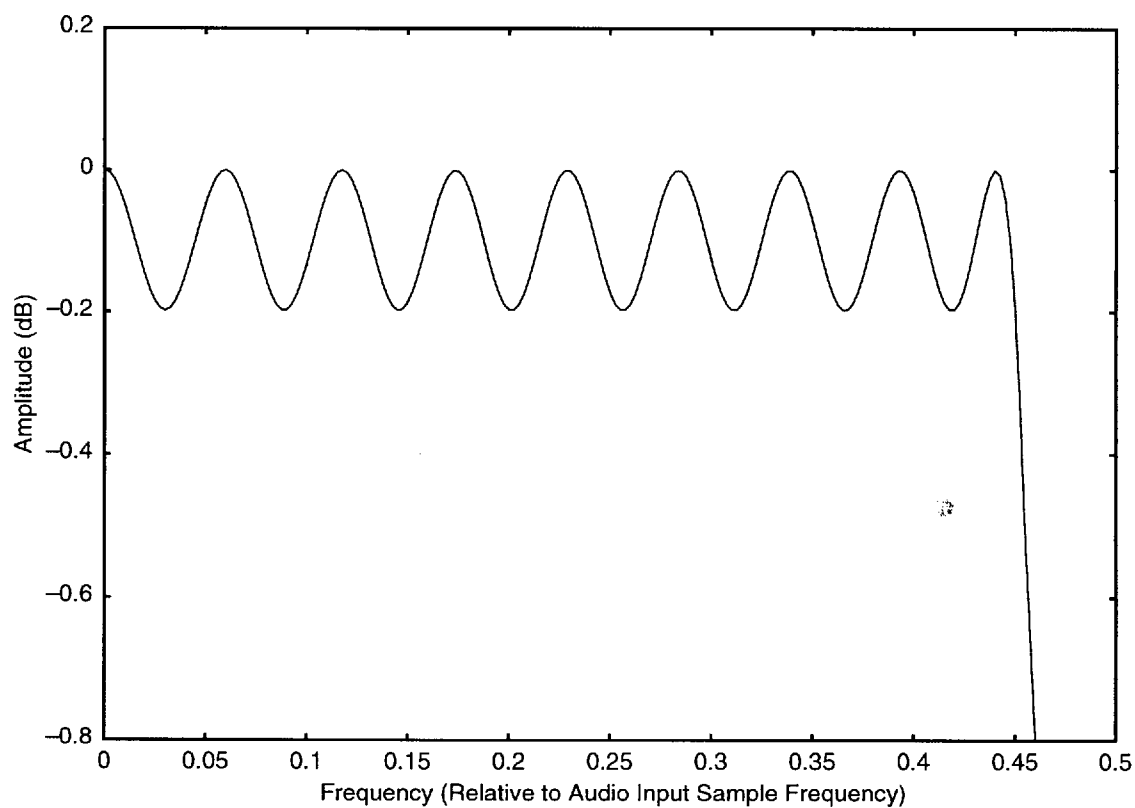
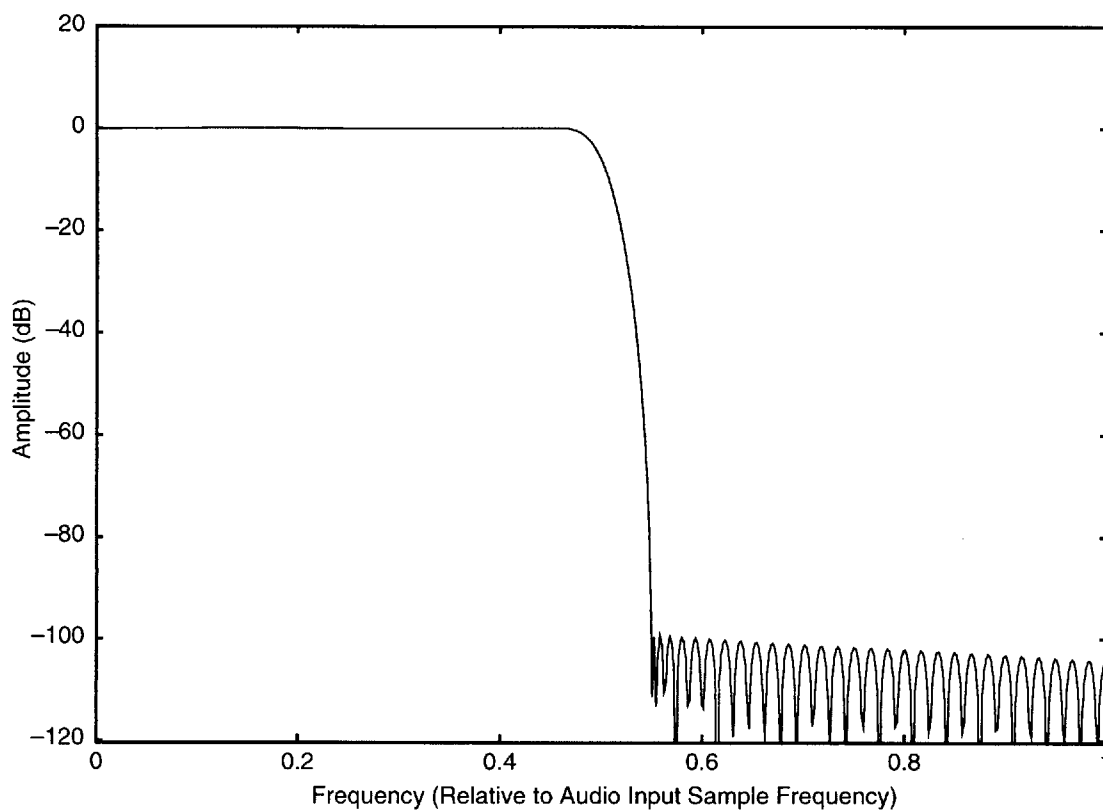
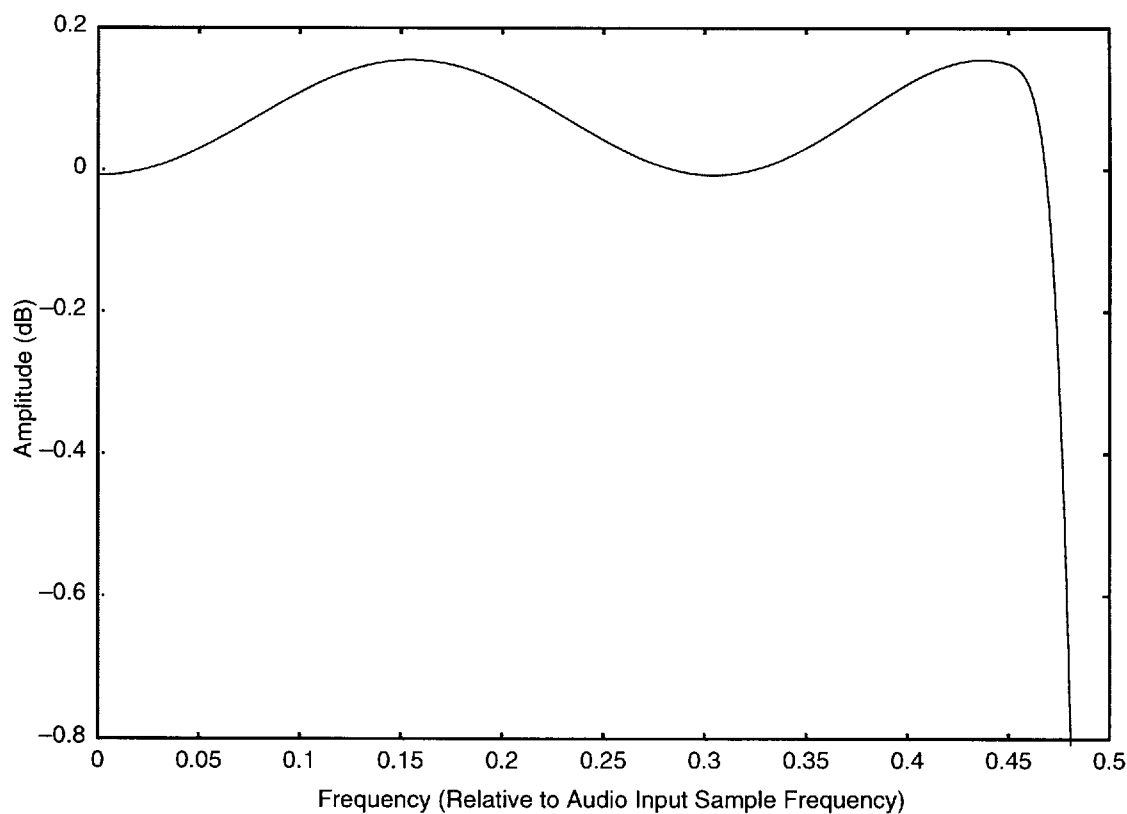
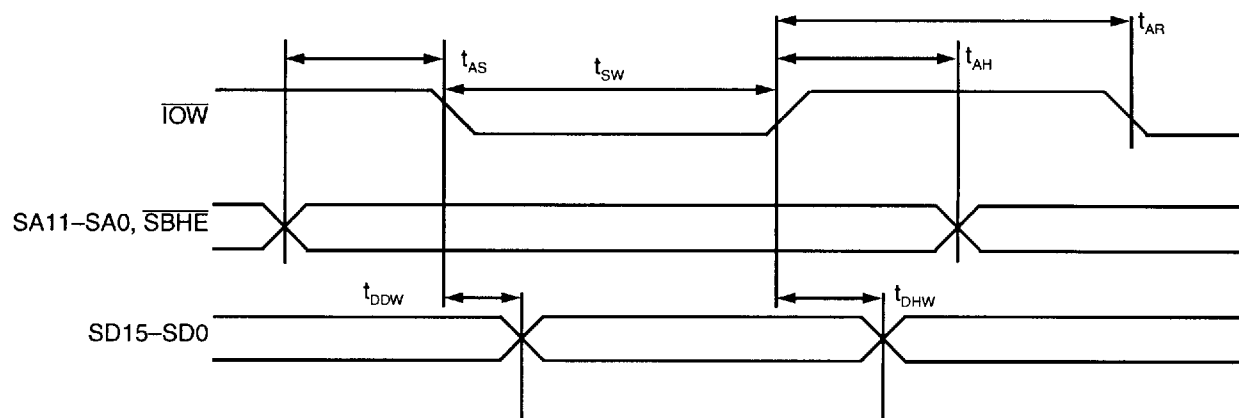


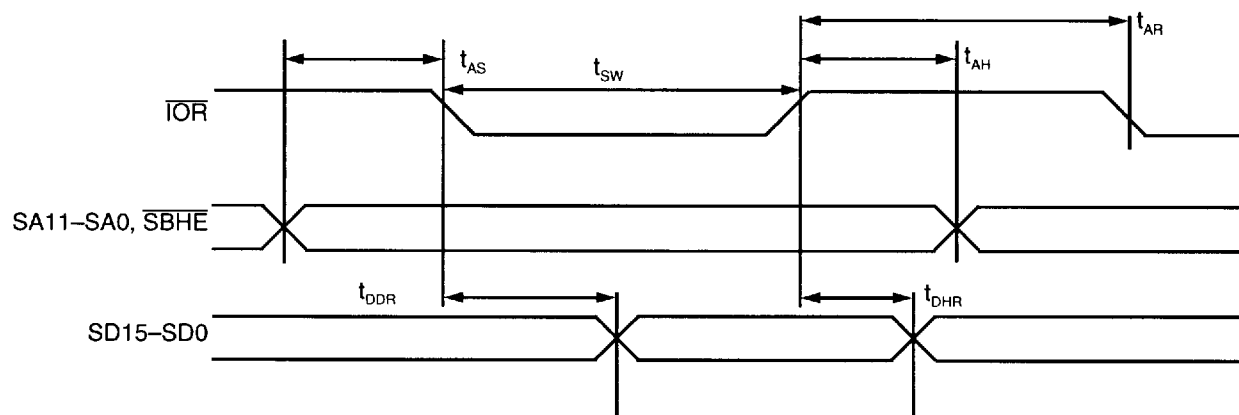
Figure 2. DAC Filter In Band Response



**Figure 3. ADC Filter Response****Figure 4. ADC Filter In Band Response**

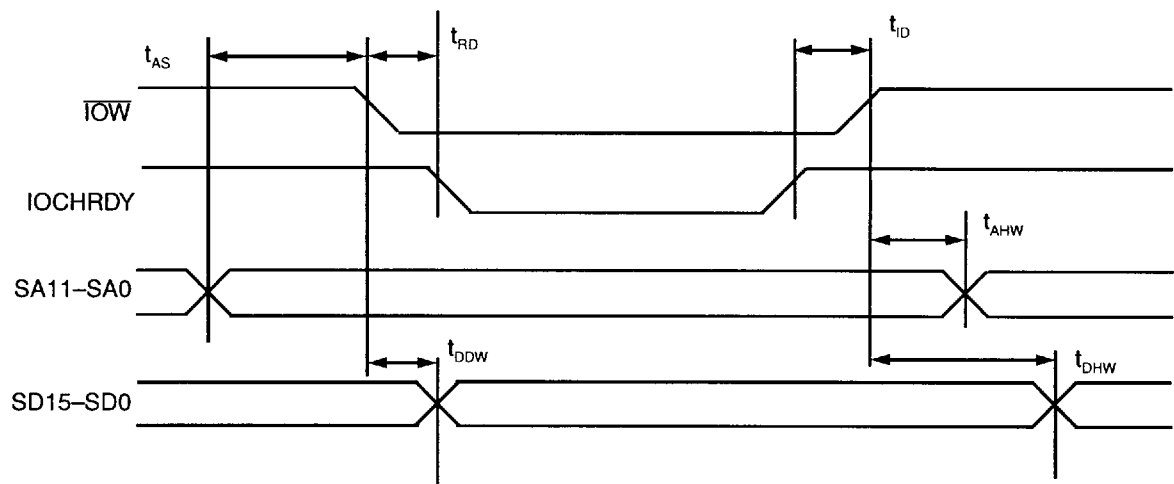


ISA Bus Write Cycle Timing

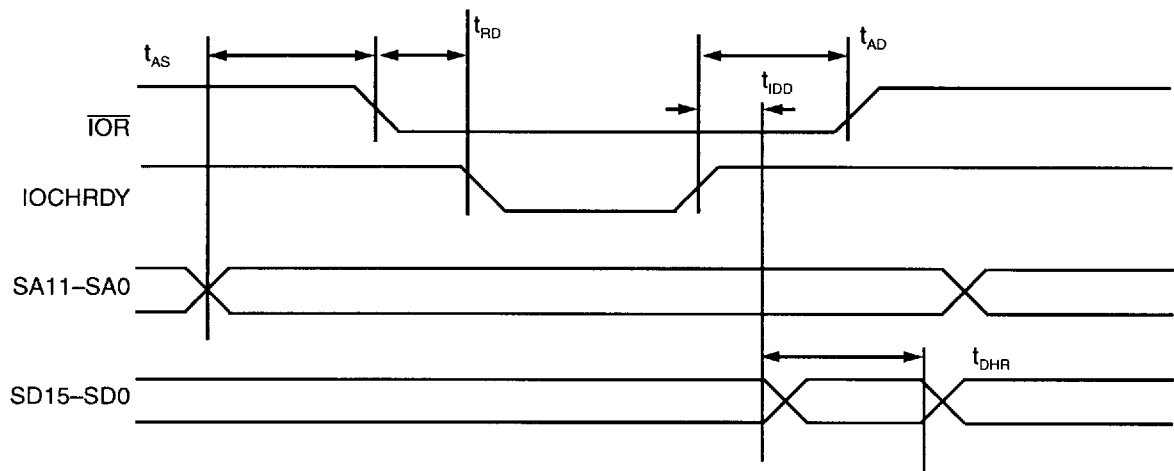


ISA Bus Read Cycle Timing

Figure 5. ISA Bus Cycle Timing



ISA Bus Extended Write Cycle Timing



ISA Bus Extended Read Cycle Timing

Figure 6. ISA Bus Extended Cycle Timing

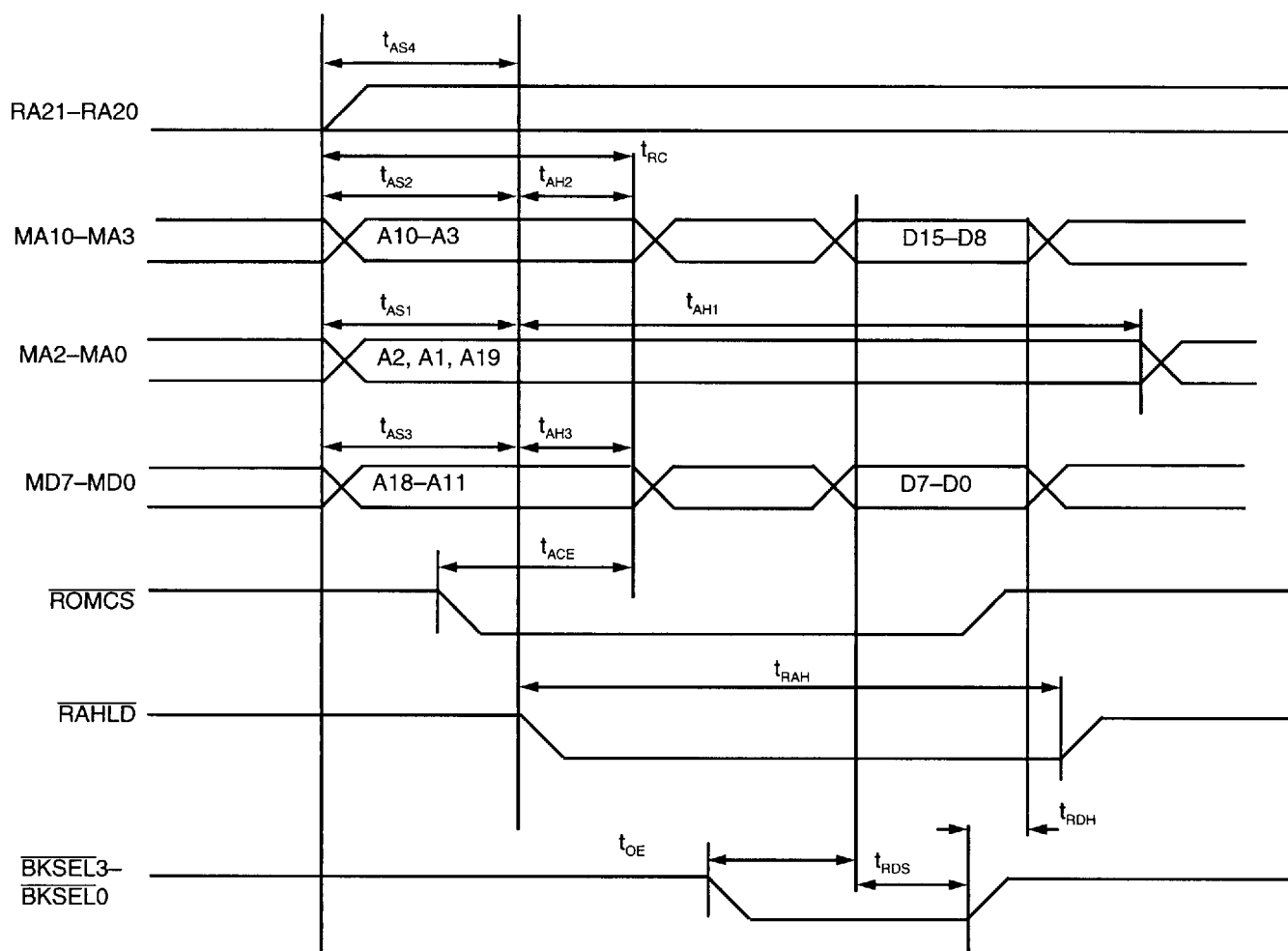
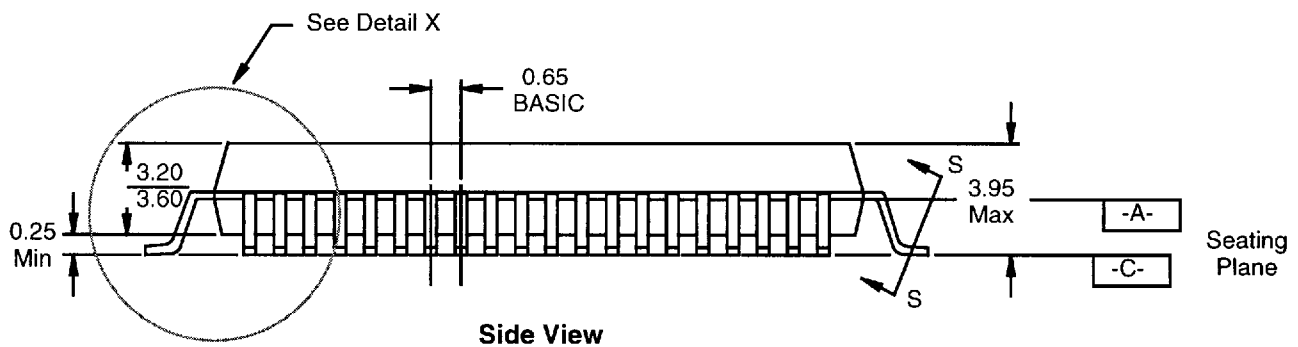
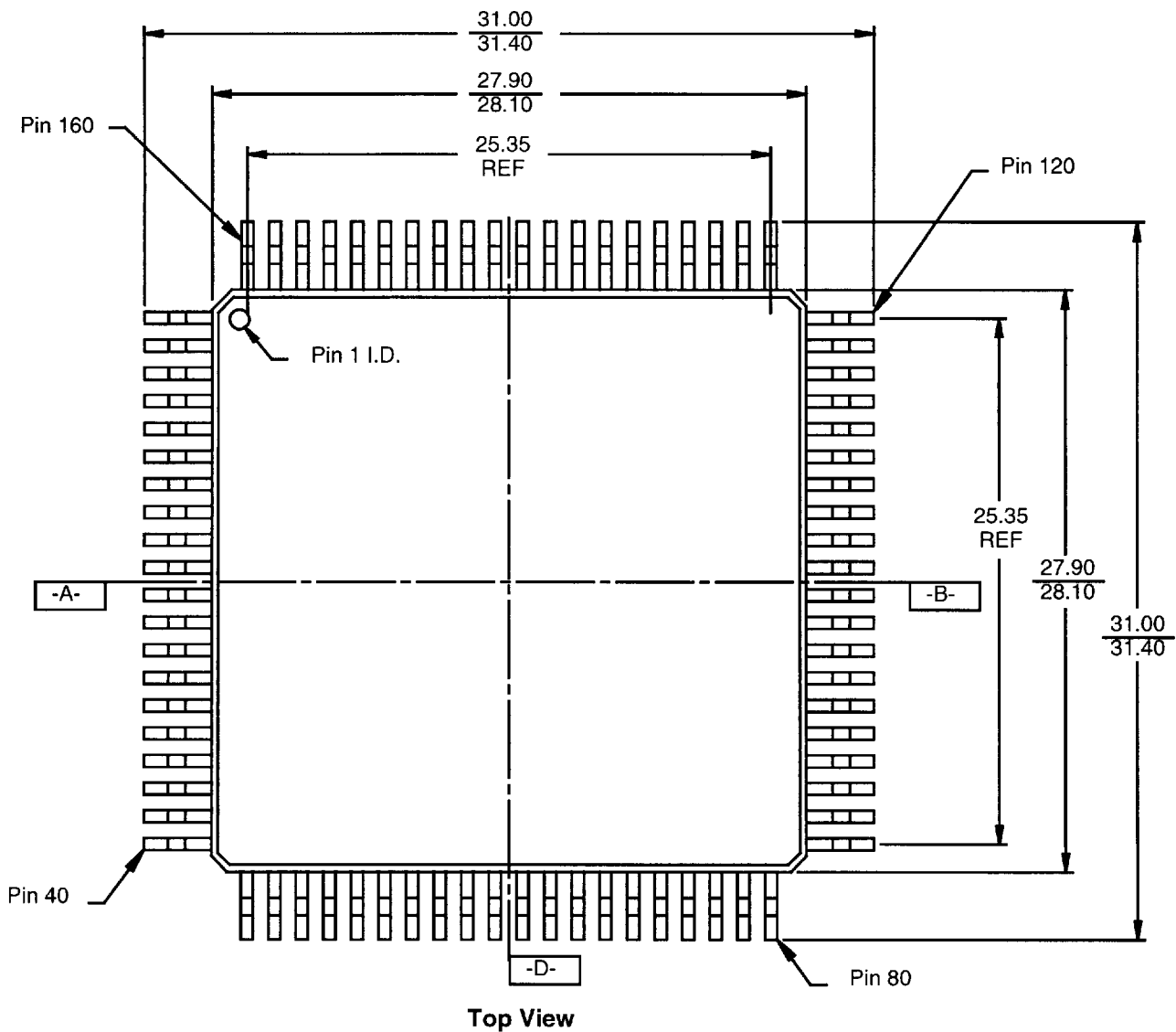


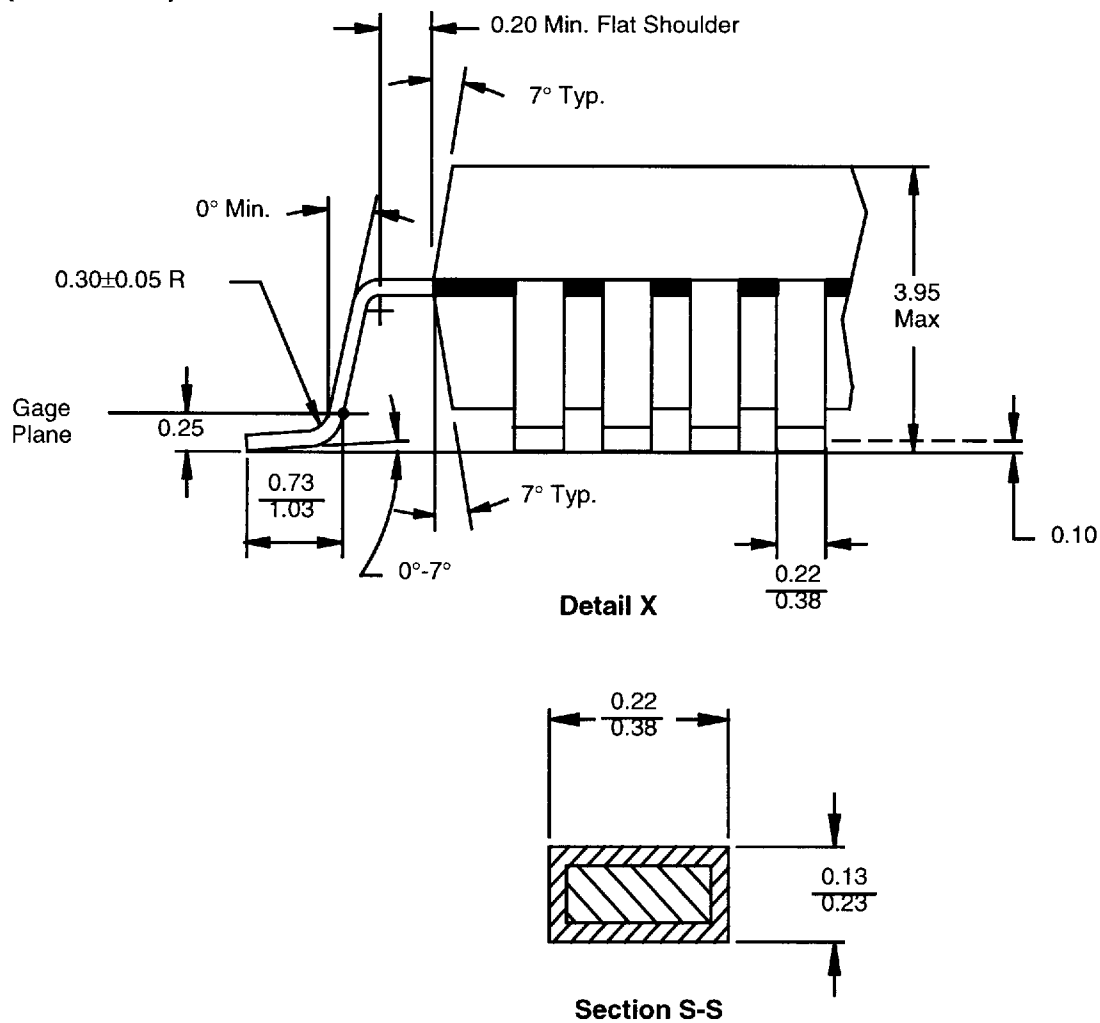
Figure 7. Local Memory: ROM Access

# PQR 160, Trimmed and Formed Plastic Quad Flat Pack



## Notes:

1. All measurements are in millimeters unless otherwise noted.
2. Not to scale; for reference only.

**PQR 160 (continued)**

**Note:**

1. Not to scale; for reference only.

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