UMC UM8881 HB4 Super Energy Star Green (reverse engineered)

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Introduction

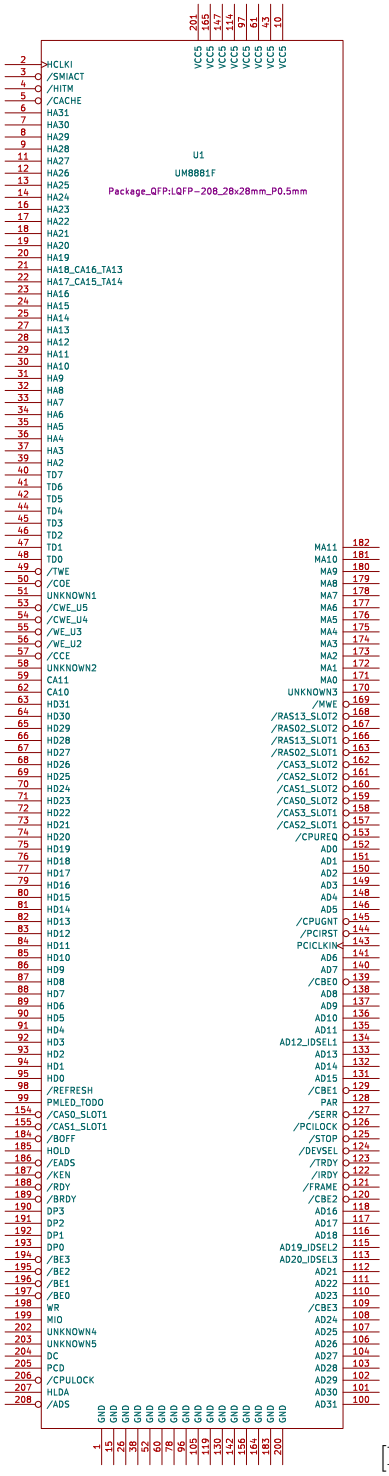
UMC didn't make "UM8881 HB4 Super Energy Star Green" technical reference public, so I made my own. Pinout obtained *pain*stakingly by measuring my ATC-1415 board. Some pin definitions may be inaccurate, incomplete or missing. The board used for experiment has UM8881F 9536-ETA chip, only 2 SIMM slots, noninterleavable cache up to 512kB. The board has been configured for Am5x86-133, which may cause some pins to be left disconnected and so unidentified. Alsop different processors have different locations for some pins. The board had also NiCd leak (but all traces seems to be fine).

Further measurements would be appreciated. Especially for boards with:

- 4 SIMM (which pins drives other slots)
- dual cache (which additional pins switch between cache banks)
- 4 PCI (which pins are used for aditional IDSEL)

Pin assignment and descripion

Schematic symbol



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Pins

Pin	Name	Description
1	GND	Ground
2	HCLKI	Host clock in, via buffer
3	/SMIACT	Jumper 27
4	/HITM	multiple jumpers
5	/CACHE	multiple jumpers
6	HA31	CPU address
7	HA30	CPU address
8	HA29	CPU address
9	HA28	CPU address
10	VCC5	Power supply +5V
11	HA27	CPU address
12	HA26	CPU address
13	HA25	CPU address
14	HA24	CPU address
15	GND	Ground
16	HA23	CPU address
17	HA22	CPU address
18	HA21	CPU address
19	HA20	CPU address
20	HA19	CPU address
21	HA18_CA16_TA13	CPU address A18, cache address A16, tag address A13 (via 512k 1-2 jumper)
22	HA17_CA15_TA14	CPU address A17, cache address A15, tag address A14 (via 256k 3-4 jumper)
23	HA16	CPU address
24	HA15	CPU address
25	HA14	CPU address
26	GND	Ground
27	HA13	CPU address
28	HA12	CPU address
29	HA11	CPU address
30	HA10	CPU address
31	HA9	CPU address
32	HA8	CPU address
33	HA7	CPU address
34	HA6	CPU address
35	HA5	CPU address
36	HA4	CPU address

Pin	Name	Description
37	HA3	CPU address
38	GND	Ground
39	HA2	CPU address
40	TD7	Cache tag data 7 (according to SRAM chip, may be permuted)
41	TD6	Cache tag data 6 (according to SRAM chip, may be permuted)
42	TD5	Cache tag data 5 (according to SRAM chip, may be permuted)
43	VCC5	Power supply +5V
44	TD4	Cache tag data 4 (according to SRAM chip, may be permuted)
45	TD3	Cache tag data 3 (according to SRAM chip, may be permuted)
46	TD2	Cache tag data 2 (according to SRAM chip, may be permuted)
47	TD1	Cache tag data 1 (according to SRAM chip, may be permuted)
48	TD0	Cache tag data 0 (according to SRAM chip, may be permuted)
49	/TWE	Cache tag write enable
50	/COE	Cache output enable via 33R
51	UNKNOWN1	TODO, maybe interleaved cache banks
52	GND	Ground
53	/CWE_U5	Cache write enable for U5 SRAM, TODO which HD[] octet
54	/CWE_U4	Cache write enable for U4 SRAM, TODO which HD[] octet
55	/WE_U3	Cache write enable for U3 SRAM, TODO which HD[] octet

Pin	Name	Description
56	/WE_U2	Cache write enable for U2 SRAM, TODO which HD[] octet
57	/CCE	Cache chip enable, via 33R
58	UNKNOWN2	TODO, maybe interleaved cache banks
59	CA11	Cache address 11, TODO
60	GND	Ground
61	VCC5	Power supply +5V
62	CA10	Cache address 10, TODO
63	HD31	CPU (host) data 31
64	HD30	CPU data 30
65	HD29	CPU data 29
66	HD28	CPU data 28
67	HD27	CPU data 27
68	HD26	CPU data 26
69	HD25	CPU data 25
70	HD24	CPU data 24
71	HD23	CPU data 23
72	HD22	CPU data 22
73	HD21	CPU data 21
74	HD20	CPU data 20
75	HD19	CPU data 19
76	HD18	CPU data 18
77	HD17	CPU data 17
78	GND	Ground
79	HD16	CPU data 16
80	HD15	CPU data 15
81	HD14	CPU data 14
82	HD13	CPU data 13
83	HD12	CPU data 12
84	HD11	CPU data 11
85	HD10	CPU data 10
86	HD9	CPU data 9
87	HD8	CPU data 8
88	HD7	CPU data 7
89	HD6	CPU data 6
90	HD5	CPU data 5
91	HD4	CPU data 4
92	HD3	CPU data 3
93	HD2	CPU data 2

Pin	Name	Description
94	HD1	CPU data 1
95	HD0	CPU data 0
96	GND	Ground
97	VCC5	Power supply +5V
98	/REFRESH	ISA /REFRESH, via R22 (470R) to +5V, via R23 (33R) to UM8886 p145, via C7 to GND
99	PMLED_TODO	U18.2 (AND input), via R38 to +5V, other AND input (?) UM8886 pin 54, output via R88 to turbo LED
100	AD31	PCI Address/Data 31
101	AD30	PCI Address/Data 30
102	AD29	PCI Address/Data 29
103	AD28	PCI Address/Data 28
104	AD27	PCI Address/Data 27
105	GND	Ground
106	AD26	PCI Address/Data 26
107	AD25	PCI Address/Data 25
108	AD24	PCI Address/Data 24
109	/CBE3	PCI command/byte enable 3
110	AD23	PCI Address/Data 23
111	AD22	PCI Address/Data 22
112	AD21	PCI Address/Data 21
113	AD20_IDSEL3	PCI Address/Data 20, IDSEL slot 3
114	VCC5	Power supply +5V
115	AD19_IDSEL2	PCI Address/Data 19, IDSEL slot 2
116	AD18	PCI Address/Data 18
117	AD17	PCI Address/Data 17
118	AD16	PCI Address/Data 16
119	GND	Ground
120	/CBE2	PCI command/byte enable 2
121	/FRAME	PCI frame signal
122	/IRDY	PCI initiator ready, via R17 (33R)
123	/TRDY	PCI target ready, via R18 (33R)
124	/DEVSEL	PCI target selected

Pin	Name	Description
125	/STOP	PCI target halt request
126	/PCILOCK	PCI locked transaction
127	/SERR	PCI systém error
128	PAR	PCI parity
129	/CBE1	PCI command/byte enable 1
130	GND	Ground
131	AD15	PCI Address/Data 15
132	AD14	PCI Address/Data 14
133	AD13	PCI Address/Data 13
134	AD12_IDSEL1	PCI Address/Data 12, IDSEL slot 1
135	AD11	PCI Address/Data 11
136	AD10	PCI Address/Data 10
137	AD9	PCI Address/Data 9
138	AD8	PCI Address/Data 8
139	/CBE0	PCI command/byte enable 0
140	AD7	PCI Address/Data 7
141	AD6	PCI Address/Data 6
142	GND	Ground
143	PCICLKIN	PCI clock input driven via 10R and buffer from UM8886 pin 53
144	/PCIRST	PCI bus reset
145	/CPUGNT	Input driven from UM8886 pin 121, CPU gets granted PCI bus
146	AD5	PCI Address/Data 5
147	VCC5	Power supply +5V
148	AD4	PCI Address/Data 4
149	AD3	PCI Address/Data 3
150	AD2	PCI Address/Data 2
151	AD1	PCI Address/Data 1
152	AD0	PCI Address/Data 0
153	/CPUREQ	Output sent to UM8886 pin 124, CPU requests PCI bus
154	/CAS0_SLOT1	DRAM column address strobe 0, SIMM slot 1 (possible permutations)
155	/CAS1_SLOT1	DRAM column address strobe 1, SIMM slot 1 (possible permutations)

Pin	Name	Description
156	GND	Ground
157	/CAS2_SLOT1	DRAM column address strobe 2, SIMM slot 1 (possible permutations)
158	/CAS3_SLOT1	DRAM column address strobe 3, SIMM slot 1 (possible permutations)
159	/CAS0_SLOT2	DRAM column address strobe 0, SIMM slot 2 (possible permutations)
160	/CAS1_SLOT2	DRAM column address strobe 1, SIMM slot 2 (possible permutations)
161	/CAS2_SLOT2	DRAM column address strobe 2, SIMM slot 2 (possible permutations)
162	/CAS3_SLOT2	DRAM column address strobe 3, SIMM slot 2 (possible permutations)
163	/RAS02_SLOT1	DRAM row address strobe 0/2, via buffer to SIMM slot 1 (possible permutations)
164	GND	Ground
165	VCC5	Power supply +5V
166	/RAS13_SLOT1	DRAM row address strobe 1/3, via buffer to SIMM slot 1 (possible permutations)
167	/RAS02_SLOT2	DRAM row address strobe 0/2, via buffer to SIMM slot 2 (possible permutations)
168	/RAS13_SLOT2	DRAM row address strobe 1/3, via buffer to SIMM slot 2 (possible permutations)
169	/MWE	DRAM write enable, via buffer to all slots
170	UNKNOWN3	TODO, possibly slot 3 and 4 signals
171	MA0	DRAM column/row address 0, via buffer

Pin	Name	Description
172	MA1	DRAM column/row address 1, via buffer
173	MA2	DRAM column/row address 2, via buffer
174	MA3	DRAM column/row address 3, via buffer
175	MA4	DRAM column/row address 4, via buffer
176	MA5	DRAM column/row address 5, via buffer
177	MA6	DRAM column/row address 6, via buffer
178	MA7	DRAM column/row address 7, via buffer
179	MA8	DRAM column/row address 8, via buffer
180	MA9	DRAM column/row address 9, via buffer
181	MA10	DRAM column/row address 10, via buffer
182	MA11	DRAM column/row address 11, via 10R
183	GND	Ground
184	/BOFF	CPU backoff from bus
185	HOLD	CPU bus hold, pin E15
186	/EADS	CPU external address strobe
187	/KEN	CPU cache enable
188	/RDY	CPU non-burst ready, pin F16
189	/BRDY	CPU burst ready, pin H15
190	DP3	CPU data parity 3
191	DP2	CPU data parity 2
192	DP1	CPU data parity 1
193	DP0	CPU data parity 0
194	/BE3	CPU byte enable 3
195	/BE2	CPU byte enable 2
196	/BE1	CPU byte enable 1
197	/BE0	CPU byte enable 0
198	WR	CPU write/read bus cycle, TODO goes to jumpers (J15, J17)

Pin	Name	Description
199	MIO	CPU memory/IO bus cycle
200	GND	Ground
201	VCC5	Power supply +5V
202	UNKNOWN4	TODO, probably CPU oriented, via RP12 (~4k7) to +5V
203	UNKNOWN5	TODO seems it leads nowhere
204	DC	CPU data/control bus cycle, pin M15
205	PCD	Page cache disable
206	/CPULOCK	CPU bus lock, pin N15
207	HLDA	CPU hold acknowledge, pin P15
208	/ADS	CPU address status