NEC

MOS INTEGRATED CIRCUIT

μPD481850

8M-bit Synchronous GRAM

Description

The μPD481850 is a synchronous graphics memory (SGRAM) organized as 131,072 words × 32 bits × 2 banks random access port.

This device can operate up to 100 MHz by using synchronous interface. Also, it has 8-column Block Write function to improve capability in graphics system.

This product is packaged in 100-pin plastic QFP (14 × 20 mm).

Features

- 131,072 words × 32 bits × 2 banks memory
- Synchronous interface (Fully synchronous DRAM with all input signals are latched at rising edge of clock)
  - : Pulsed interface
  - : Automatic precharge and controlled precharge commands
  - : Ping-pong operation between the two internal memory banks
  - : Up to 100 MHz operation frequency
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A9 (Bank Address: BA)
- Byte control using DQM0 to DQM3 signals both in read and write cycle
- 8-column Block Write (BW) function
- Persistent write per bit (WPB) function
- Wrap sequence: Sequential
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable $\overline{CAS}$ latency (2 and 3)
- Power Down operation and Clock Suspend operation
- Auto refresh (CBR refresh) or self refresh capability
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible inputs and outputs
- 100-pin Plastic QFP (14 × 20 mm)
- 1,024 refresh cycles/16 ms
- Burst termination by Precharge command
- Burst termination by Burst stop command (in case of full-page burst)

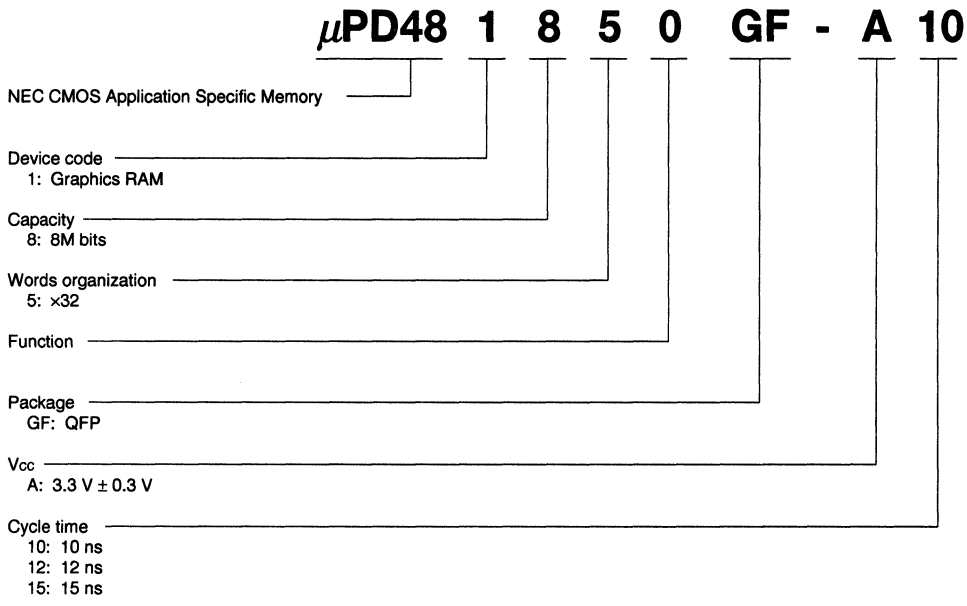
Ordering Information

Part number	Cycle time ns (MIN.)	Clock frequency MHz (MAX.)	Package
μPD481850GF-A10-JBT	10	100	100-pin Plastic QFP (14 × 20 mm)
μPD481850GF-A12-JBT	12	83	
μPD481850GF-A15-JBT	15	66	

The information in this document is subject to change without notice.

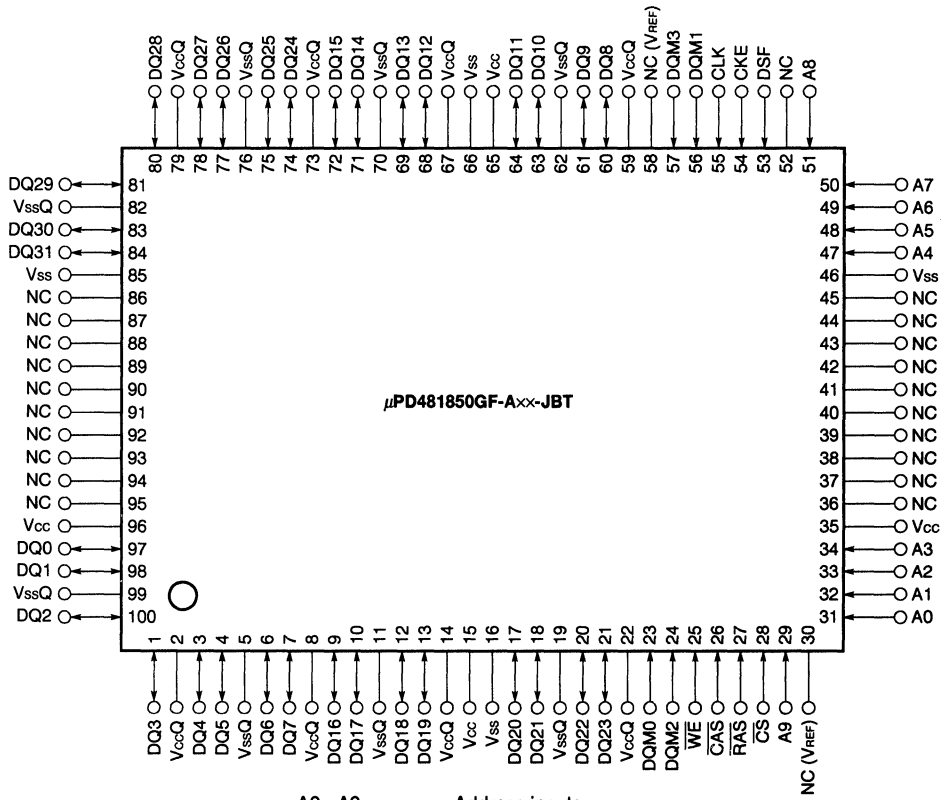
Part Number

Synchronous GRAM



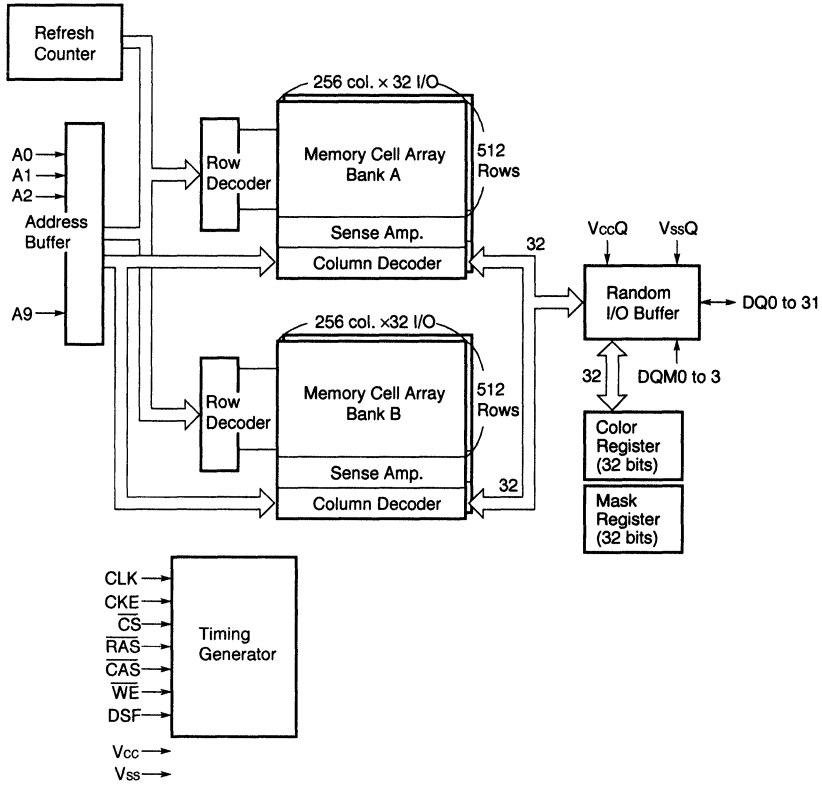
Pin Configuration (Marking Side)

100-pin Plastic QFP (14 × 20 mm)



A0 - A9	:	Address inputs
A0 - A8	:	Row address inputs
A0 - A7	:	Column address inputs
A9	:	Bank address
DQ0 - DQ31	:	Data inputs/outputs
$\overline{CS}$	:	Chip select
$\overline{RAS}$	:	Row address strobe
$\overline{CAS}$	:	Column address strobe
$\overline{WE}$	:	Write enable
DQM0 - DQM3	:	DQ mask enable
DSF	:	Special function enable
CKE	:	Clock enable
CLK	:	System clock input
V_{CC}	:	Supply voltage
V_{SS}	:	Ground
$V_{CC}Q$	:	Supply voltage for DQ
$V_{SS}Q$	:	Ground for DQ
NC	:	No connection

Block Diagram



1. Input/Output Pin Function

Pin name	Input/Output	Function
CLK	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the μPD481850 suspends operation. When the μPD481850 is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low. In Self refresh mode, low level on this pin is also used as part of the input command to specify Self refresh.
$\overline{CS}$	Input	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
DSF	Input	DSF is part of the inputs of graphics command of the μPD481850. If DSF is inactive (Low level), μPD481850 operates as same as SDRAM.
A0 - A8	Input	Row Address is determined by A0 - A8 at the CLK (clock) rising edge in the activate command cycle. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A8 defines the precharge mode. When A8 is high in the precharge command cycle, both banks are precharged; when A8 is low, only the bank selected by A9 is precharged. When A8 high in read or write command cycle, the precharge start automatically after the burst access.
A9		A9 is the bank address signal (BA). In command cycle, A9 low selects bank A and A9 high selects bank B.
DQM0 - DQM3	Input	DQM controls I/O buffers. DQM0 corresponds to the lowest byte (DQ0 to DQ7), DQM1 corresponds to DQ8 to DQ15, DQM2 corresponds to DQ16 to DQ23. DQM3 corresponds to DQ24 to DQ31. In read mode, DQM controls the output buffers like a conventional $\overline{OE}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ31	Input/Output	DQ pins have the same function as I/O pins on a conventional DRAM. These are normally 32-bit data bus and are used for inputting and outputting data. · Function as the mask data input pins in the special register set command. Write operations can be performed after Active command with WPB (old mask data). · Functions as the column selection data input pin in the block write cycle.
V_{CC} V_{SS} $V_{CC}Q$ $V_{SS}Q$	(Power supply)	V_{CC} and V_{SS} are power supply pins for internal circuits. $V_{CC}Q$ and $V_{SS}Q$ are power supply pins for the output buffers.