ICD2028

PC Motherboard Clock Generator

Features

- **Eight independent clock outputs handle all clocking requirements for personal computer motherboards**
- **CPU clock frequency range: 10 MHz to 100 MHz with user-defined duty cycle**
- **Four user-configurable outputs**
- **Skew-free CPU clock, CPU clock ÷2, and buffered CPU clock options on configurable outputs**
- **Ideally suited for desktop PCs**
- **Phase-locked loop oscillator input derived from single 14.31818 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **Battery input maintains 32.768 kHz clock during power-down**
- **Three-state oscillator control disables outputs for test purposes**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

A modern personal computer motherboard often requires as many as seven different crystal can oscillators. The System Logic family of frequency synthesis parts from Cypress/IC Designs replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2028 is a second-generation PC Motherboard Clock Generator built on the foundation of the industry-standard and most widely-used ICD2023. The ICD2028 offers most of the features of the ICD2023, as well as some important enhancements:

- An additional VCO
- An additional clock output
- Four customer-configured outputs which can be configured to have
  - — A skew-free divided-by-two CPU clock
  - — An additional skew-free CPU clock
- User-definable CPUCLK output duty cycle

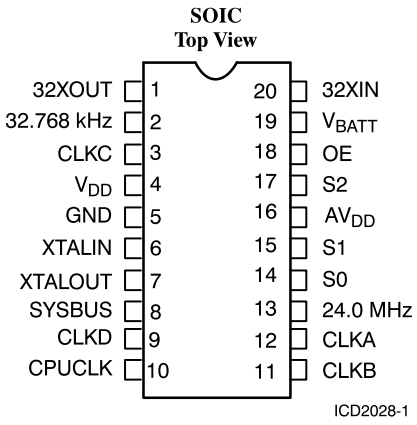
Because today's desktop PCs must support a myriad of new requirements, and each company's implementation tends to be unique, the most important new feature of the ICD2028 is its ability to tailor four of the outputs to the individual needs of today's system logic design engineer, and to configure the CPUCLK duty cycle for special microprocessor needs.

The ICD2028 was specifically designed to support such demanding clock requirements as:

- 486 and Pentium™ microprocessors both with and without clock doublers
- New single-chip system logic chip sets
- Super I/O combo chips
- New high-density floppy disk drive controllers

The ICD2028 consists of two crystal-controlled oscillators, three phase-locked loops, and eight different outputs in a single package. To sum up, the greatest asset of the ICD2028 lies in its ability to serve as the single source of all clocking requirements in modern desktop PCs.

Pin Configuration



ICD2028-1

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June 1994 − Revised April 1995

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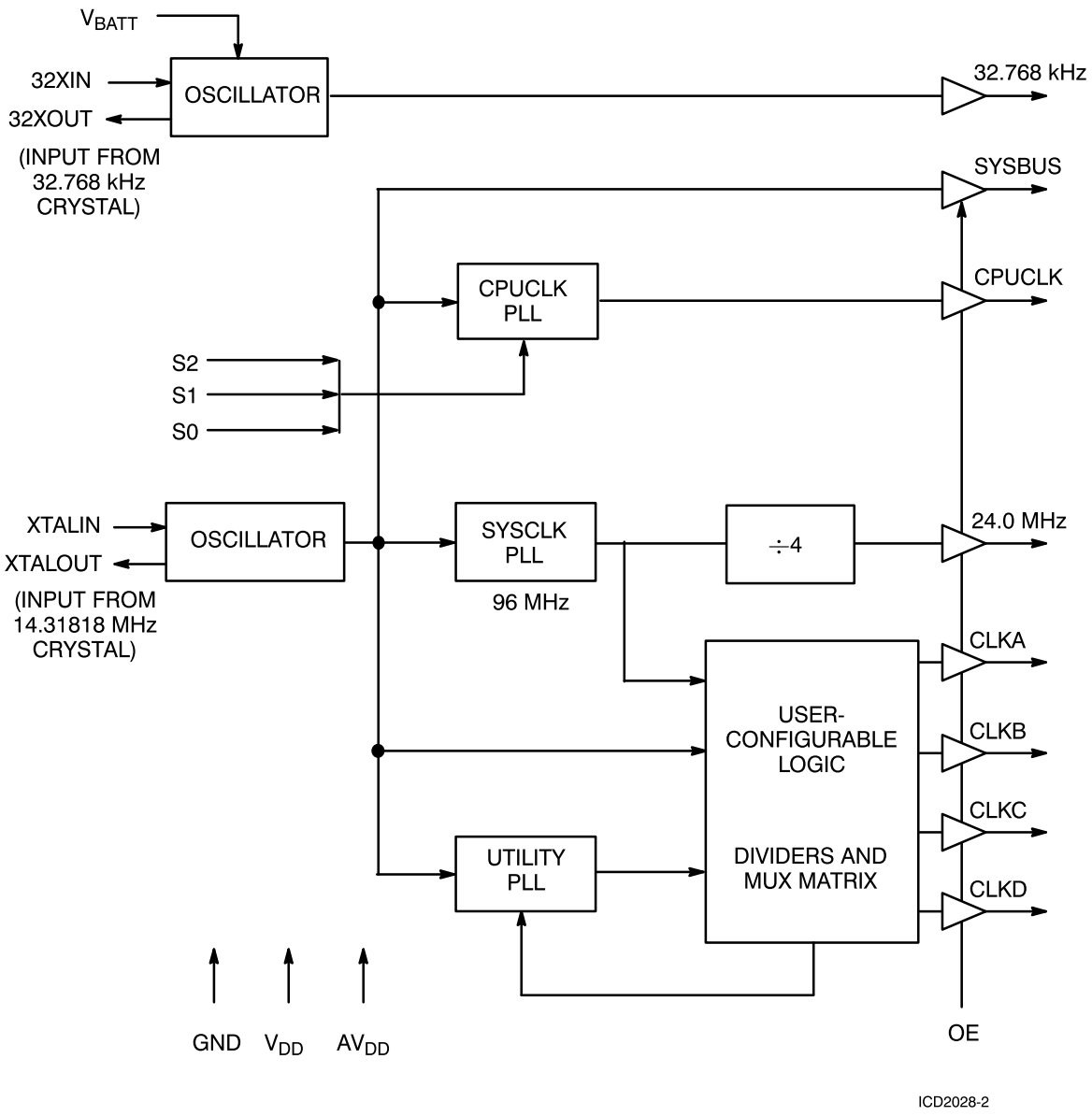
Block Diagram



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Pin Summary

Name	Number	Description
32XOUT[1]	1	Oscillator output to a 32.768 kHz parallel-resonant crystal
32.768 kHz	2	32.768 kHz clock output
CLKC	3	User-configurable clock output (See *User-Selectable Clock Options* for values.)
V_{DD}	4	+5V
GND	5	Ground
XTALIN[1]	6	Reference Oscillator input for all internal phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[1]	7	Oscillator Output to a reference crystal.
SYSBUS	8	Buffered 14.31818 MHz crystal output
CLKD	9	User-configurable clock output (See *User-Selection Clock Options* for values.)
CPUCLK	10	CPUCLK clock output (See *CPU Clock Selection* for values.)
CLKB	11	User-configurable clock output (See *User-Selection Clock Options* for values.)
CLKA	12	User-configurable clock output (See *User-Selection Clock Options* for values.)
24.0 MHz	13	24.0 MHz clock output
S0	14	Input select line 0 for CPUCLK (pin has internal pull-down)
S1	15	Input select line 1 for CPUCLK (pin has internal pull-down)
AV_{DD}	16	+5V to analog core
S2	17	Input select line 2 for CPUCLK (pin has internal pull-down)
OE	18	Output Enable three-states output when signal is LOW (pin has internal pull-up)
V_{BATT}	19	+2 to +5V for battery backup operation; powers 32.768 kHz oscillator.
32XIN[NO TAG]	20	Oscillator input from a 32.768 kHz parallel-resonant crystal.

Notes:
1. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD} = 17 pF.

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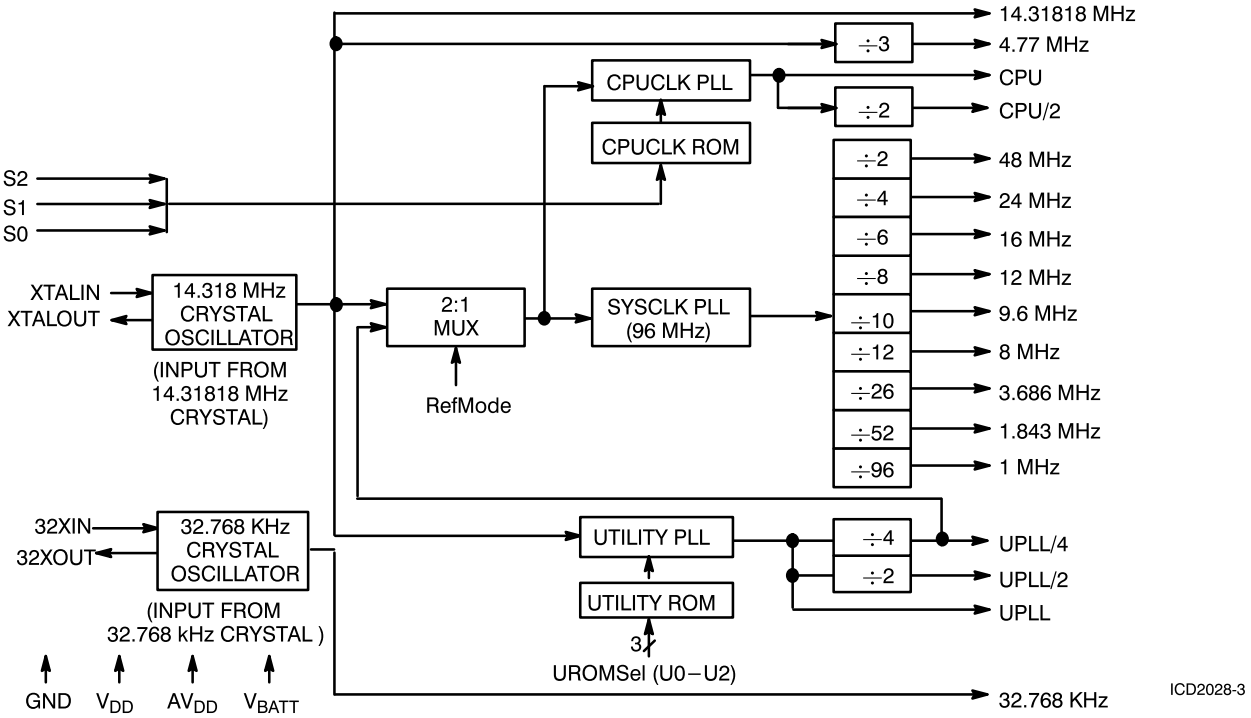

Figure 1. Inputs

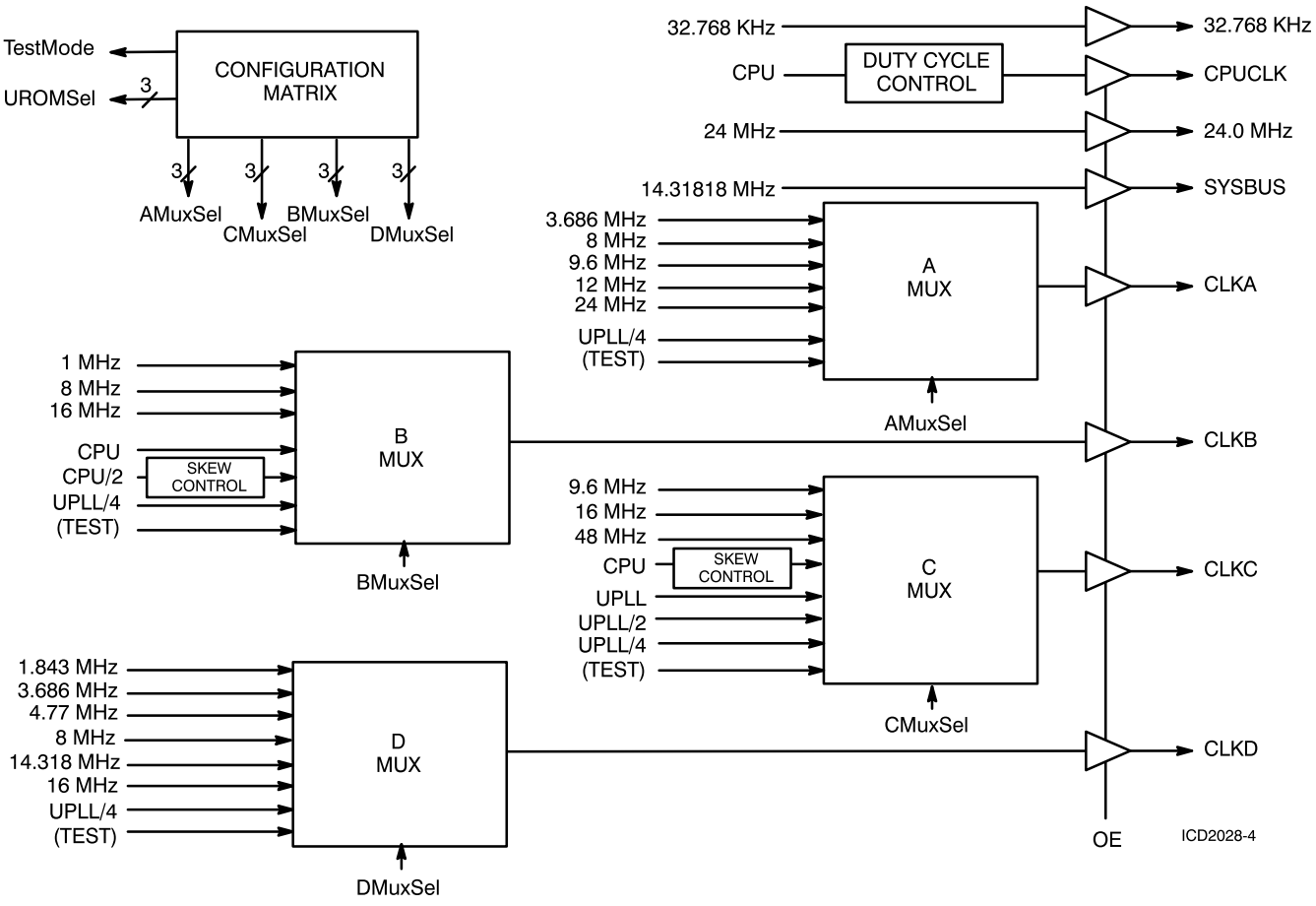

Figure 2. Outputs

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User-Selectable Clock Options

System and Utility Clock Selection

The heart of the ICD2028 is the rich set of frequencies which are generated internally, encompassing most known system logic motherboard requirements. From this set of outputs, the user may select four output frequencies.

Through a proprietary technique, Cypress/IC Designs can quickly configure samples of any desired output pin configuration. The configuration process involves no NRE (non-recurring engineering) charges or prototype delays, as are commonly associated with masked ROM changes. Samples of user-configured ICD2028s can generally be made available in 24 hours.

Tables NO TAG and *NO TAG* list all the available internally generated system clocks on the CLKA, CLKB, CLKC, and CLKD outputs, as well as the Utility PLL output.

Table 1. System Clock Options

Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)	Clock Source	Available on Pin (s)					
					CLKA	CLKB	CLKC	CLKD	SYSBUS	24.0 MHz
SYSCLK PLL	96.000	95.870	1361	SYSCLK						
	48.000	47.935	1361	SYSCLK/2			X			
Super Floppy	32.000	31.957	1361	SYSCLK/3	X	X				
Floppy Disk	24.000	23.967	1361	SYSCLK/4	X					X
Internal Bus	16.000	15.978	1361	SYSCLK/6		X	X	X		
System Bus	14.318	14.318	0	f_{REF}				X	X	
Keyboard	12.000	11.984	1361	SYSCLK/8	X					
	9.600	9.587	1361	SYSCLK/10	X		X			
Bus Clock	8.000	7.989	1361	SYSCLK/12	X	X		X		
	4.770	4.773	572	$f_{REF}/3$				X		
Alt. Comm. Port	3.686	3.687	242	SYSCLK/26		X		X		
Serial Port	1.843	1.844	242	SYSCLK/52				X		
Special CLK	1.000	0.999	1361	SYSCLK/96		X				

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Table 2. Utility PLL Options

Clock Function	ROM Source[2]	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)	Clock Source[3]	Available on Pin (s)			
						CLKA	CLKB	CLKC	CLKD
Alt. Comm. Port	A & B	18.432	18.431	62	Utility PLL/4	X	X	X	X
	A & B	36.864	36.862	62	Utility PLL/2			X	
	A & B	73.728	73.723	62	Utility PLL			X	
Custom	A & B	14.746	14.748	144	Utility PLL/4	X	X	X	X
	A & B	29.492	29.495	144	Utility PLL/2			X	
	A & B	58.984	58.991	144	Utility PLL			X	
Custom	A & B	19.200	19.199	32	Utility PLL/4	X	X	X	X
	A & B	38.400	38.399	32	Utility PLL/2			X	
	A & B	76.800	76.798	32	Utility PLL			X	
Super I/O−1	B	32.000	31.997	102	Utility PLL/4	X	X	X	X
	B	64.000	63.994	102	Utility PLL/2			X	
	B	128.000	127.987	102	Utility PLL			X	
Super I/O−2	B	16.000	16.003	167	Utility PLL/4	X	X	X	X
	B	32.000	32.005	167	Utility PLL/2			X	
	B	64.000	64.011	167	Utility PLL			X	
Shut VCO	A & B	–	–	–	–				
	A & B	–	–	–	–				
	A & B	–	–	–	–				

Notes:
2. Refers to the two currently available ROM Options: A and B.
3. Each clock function outputs three separate frequencies: UPLL, UPLL/2 and UPLL/4.

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CPU Clock Selection

The output frequency of the CPU clock oscillator (CPUCLK) is selected by the Clock Selection Inputs S0−S2. This lets the ICD2028 support different microprocessor speed configurations. There are two ROM options available, shown in *Table NO TAG* and *Table NO TAG*.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately seeks the new frequency. During the transition period (about 5 msec), the clock output is multiplexed glitch-free to the reference signal (14.318 MHz) until the PLL settles to the new frequency. The timing for this transition is shown in Electrical Characteristics.

Table 3. CPUCLK Output—ROM Option A

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.045	2272
0	0	1	24.000	23.967	1361
0	1	0	32.000	32.045	1422
0	1	1	40.000	40.091	2272
1	0	0	50.000	49.992	154
1	0	1	66.600	66.596	1058
1	1	0	80.000	80.182	2272
1	1	1	100.000	99.818	1822

Table 4. CPUCLK Output—ROM Option B

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	Error (PPM)
0	0	0	20.000	20.003	167
0	0	1	24.000	23.967	1359
0	1	0	60.000	59.974	429
0	1	1	40.000	40.007	167
1	0	0	50.000	50.000	0
1	0	1	66.600	66.645	331
1	1	0	80.000	80.013	167
1	1	1	100.000	99.840	1600

Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the equation I = C x V x f, where I=current, C=load capacitance (max. 25 pF), V=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and f=output frequency in MHz.

To calculate total operating current, sum the following:

32.768 KHz −> C_{32} x V x .032 x 10^{-3} mA
14.318 MHz −> C_{14} x V x 14.318 x 10^{-3} mA
24.0 MHz −> C_{24} x V x 24 x 10^{-3} mA
CPUCLK −> C_{CPUCLK} x V x f_{CPUCLK} x 10^{-3} mA
CLKA −> C_{CLKA} x V x f_{CLKA} x 10^{-3} mA
CLKB −> C_{CLKB} x V x f_{CLKB} x 10^{-3} mA
CLKC −> C_{CLKC} x V x f_{CLKC} x 10^{-3} mA
CLKD −> C_{CLKD} x V x f_{CLKD} x 10^{-3} mA
Internal −> 17 mA

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5−10 pF loading, depending on the package type.

Some typical values are displayed in *Table NO TAG*.

Table 5. Operating Current Typical Values

Frequency	Capacitive Load	Current (in mA)
		V_{DD}=5V
LOW	LOW	20
HIGH	LOW	35
HIGH	HIGH	65

General Considerations

V_{BATT}

The V_{BATT} input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable. If the 32-kHz output is not used, all related inputs and outputs and V_{BATT} should be grounded.

Three-State Output Operation

The OE signal, when pulled LOW, will three-state all the clock output lines (except 32.768 kHz). This supports Wired-OR connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The OE signal contains an internal pull-up; it can be left unconnected if three-state operation is not required.

Device Specifications

Standard Configurations

While the ICD2028 can easily be configured to the user's unique requirements, there are a few standard configurations available. These are defined in *Table NO TAG*.

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Table 6. Standard Configurations[4]

Signal Name	Pin #	−2 Configuration	−4 Configuration	−5 Configuration
Reference Crystal	–	14.318 MHz	14.318 MHz	14.318 MHz
Utility PLL	–	(Off)	(Off)	32.000 MHz
CPUCLK Duty Cycle	–	50%	50%	50%
ROM Option	–	A	B	B
CPUCLK	10	Available	Available	Available
SYSBUS	8	Available	Available	Available
24.0 MHz	13	Available	Available	Available
CLKA	12	12.000 MHz	12.000 MHz	12.000 MHz
CLKB	11	CPUCLK/2	CPUCLK/2	CPUCLK/2
CLKC	3	16.000 MHz	16.000 MHz	32.000 MHz (UPLL/4)
CLKD	9	1.843 MHz	1.843 MHz	1.843 MHz
32.768 kHz	2	Available	Available	Available

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential . . . . . −0.5V to +7.0V
DC Input Voltage . . . . . −0.5V to V_{DD} +0.5V
Storage Temperature . . . . . −65°C to +150°C
Max soldering temperature (10 sec) . . . . . 260°C
Junction temperature . . . . . 125°C
Power dissipation . . . . . 750 mW

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
0°C ≤ $T_{AMBIENT}$ ≤ 70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{BATT}	Backup Battery Voltage	Typical = 3.0 Volts	2.0	5.25	V
V_{OH}	Output HIGH Voltage	I_{OH} = −4.0 mA	V_{DD}−0.5		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{OH-32}	32.768 kHz Output HIGH	I_{OH} = −0.5 mA	V_{BATT}−0.5		V
V_{OL-32}	32.768 kHz Output LOW	I_{OL} = 0.5 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except crystal inputs	2.0	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	Except crystal inputs	−0.3	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V		−250	µA
I_{OZ}	Output Leakage Current	(Three-state)		10	µA
I_{DD}	Power Supply Current	V_{DD} = Max., fully loaded output, typical = 35[5]	20	85	mA
I_{BATT}	Backup Battery Current	V_{BATT} = 3V, fully loaded output, typical = 5 µA		15	µA

Notes:
4. −2 Compatible with most 486 chip sets, while adding skew-free CPUCLK/2 support.
   −4 Supports Pentium™ processor requirements.
   −5 Provides 486 support and Super I/O (32 MHz) support.
5. CPUCLK = 66 MHz and inputs at GND or V_{DD}.

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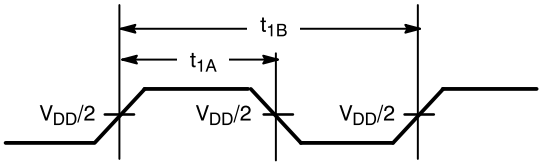
Switching Characteristics[6]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference input normal value		14.318		MHz
t_1	Input Duty Cycle	Duty cycle for the input oscillator defined as $t_1 = t_{1A} \div t_{1B}$	25%	50%	75%	
t_2	Output Period	Output frequency/period ranges (see tables under *User-Selectable Clock Options* for details)	8.3 100 MHz		2857 350 KHz	ns
t_3	Output Duty Cycle[7]	Duty cycle for the outputs, measured @ CMOS V_{TH} of $V_{DD} \div 2$	40%		60%	
t_4	Rise Times	Rise time for the outputs into a 25-pF load			4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load			4	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion			12	ns
t_7	clk Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH			12	ns
t_8	Buffered CPUCLK Skew	Skew delay between CPUCLK and buffered CPUCLK outputs, as measured @ CMOS V_{TH} of $V_{DD} \div 2$		<.25	1	ns
t_9	CPUCLK/2 Skew	Skew delay between CPUCLK and CPUCLK/2 outputs, as measured @ CMOS V_{TH} of $V_{DD} \div 2$		<.25	1	ns
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency	$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
t_B	t_{freq2} Mux Time[8]	Time clock output remains HIGH while output muxes to new frequency value	$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_{MUXREF}		Time for VCO to settle between changes		5		msec

Notes:
6. Input capacitance is typically 10 pF, except for the crystal pads.
7. Custom CPUCLK duty cycle may be special ordered. Contact your local Cypress representative for more information.
8. t_{freq2} dependent on frequency selected. freq1 and freq2 are frequencies on CPUCLK output before and after change in S0−S2.

Switching Waveforms

Duty Cycle Timing



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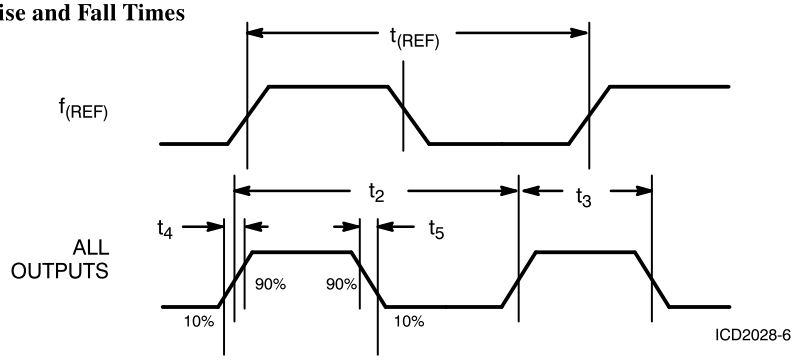
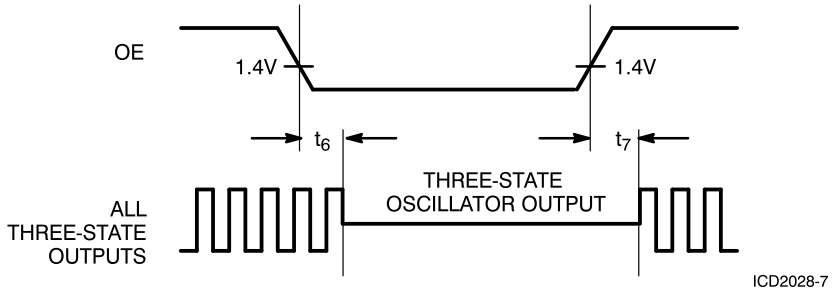
Timing Diagrams

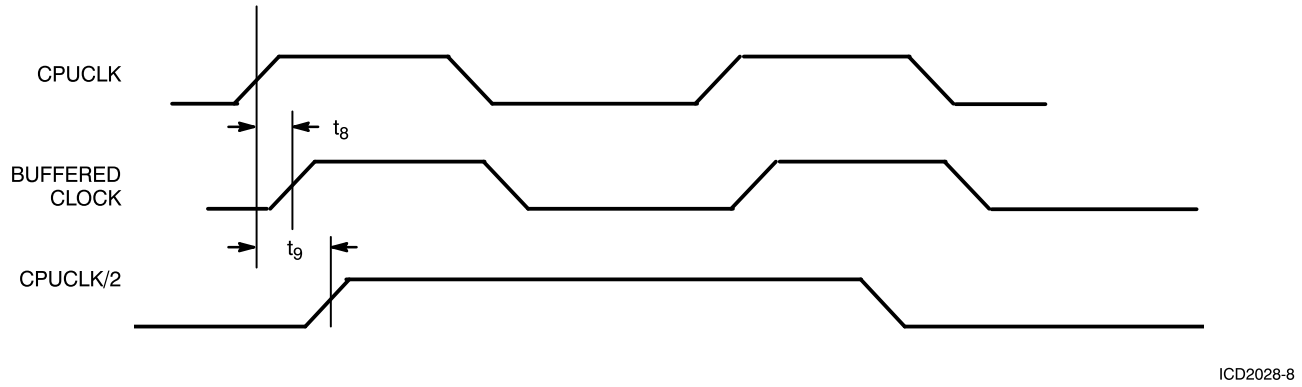
Rise and Fall Times



Three-State Timing



CPUCLK Skew



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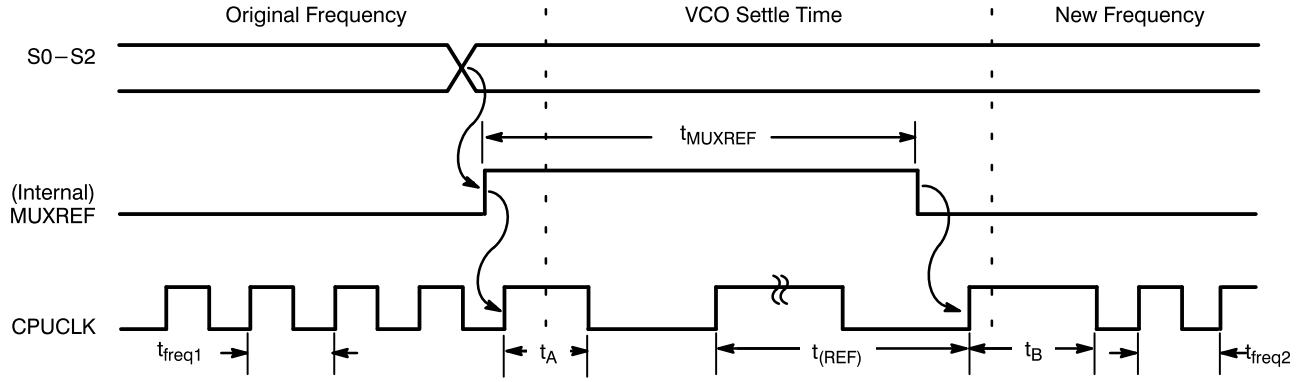
Timing Diagrams (continued)

Selection Timing



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Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2028	S5	20-Pin SOIC	C=0°C to +70°C @ V_{DD}=5V

Example: Order ICD2028SC–2 for the ICD2028, 20-pin plastic SOIC, 5V operating range device which uses the standard configuration code –2 (486 compatibility with CPUCLK/2 support). See *Table NO TAG* for details on the standard configurations.

Standard packaging is in a surface-mount configuration. The ICD2028 is also available in a through-hole DIP configuration by special order. Please contact your Cypress representative for current availability and lead times.

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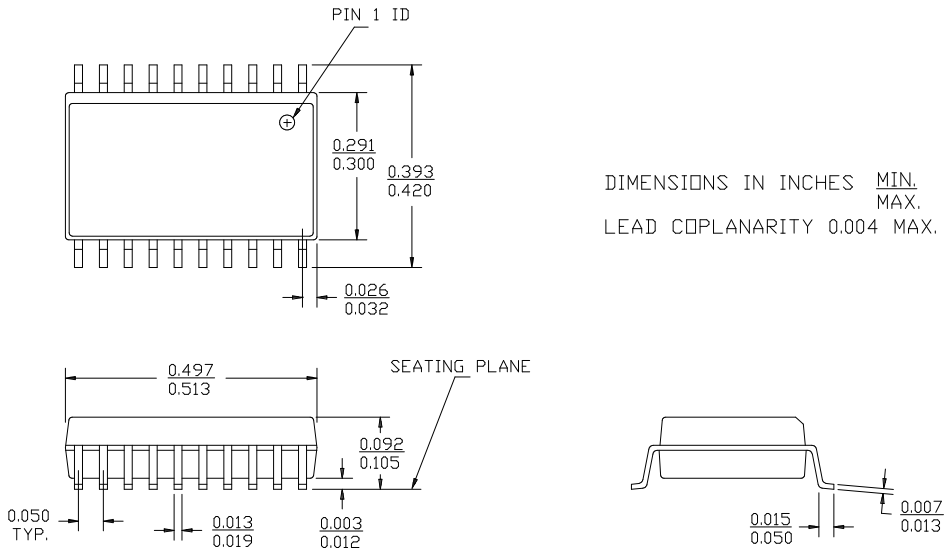
Package Diagram

20-Lead (300-Mil) Molded SOIC S5



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ICD2028 Custom Configuration Order Form

Company Name _____ Contact _____

Telephone _____ Fax _____

Output Signals

(All frequencies in MHz unless otherwise noted)

(Circle one in each line, or fill in the blanks.)

Operating Voltage (V_{DD} & AV_{DD}): 5V

Dedicated Pins: 32.768 KHz 24.000

Reference Xtal & SYSBUS Output: 14.31818

CPUCLK (Select desired ROM Option line below.)

ROM Opt. A	[20.0	24.0	32.0	40.0	50.0	66.6	80.0	100.0]
ROM Opt. B	[20.0	24.0	60.0	40.0	50.0	66.6	80.0	100.0]

CPUCLK: Duty Cycle _____ % (50%) (default) Load _____ pF (25 pF) Frequency _____ MHz (10−100 MHz)

UtilityPLL/4	18.432	14.746	20.000	19.2000	32.000	16.000[1]	OFF
CLKA	3.692	8.000	9.600	12.000	24.000	–	UPLL/4
CLKB	1.000	8.000	16.000	–	CPU[2]	CPU/2[2]	UPLL/4
CLKC	9.600	16.000	48.000	CPU[2]	UPLL	UPLL/2	UPLL/4
CLKD	1.843	3.686	4.770	8.000	14.318	16.000	UPLL/4

IC Designs Assignment Configuration Code _____ (For IC Designs use only)

Notes:
1. Only available with ROM Option B.
2. Skew-controlled to CPUCLK output.

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