

Version 30A

MS-6330 ATX

CPU:
AMD Socket-462 Processor

System Chipset:
VIA
KT133A(North)
+ 686B

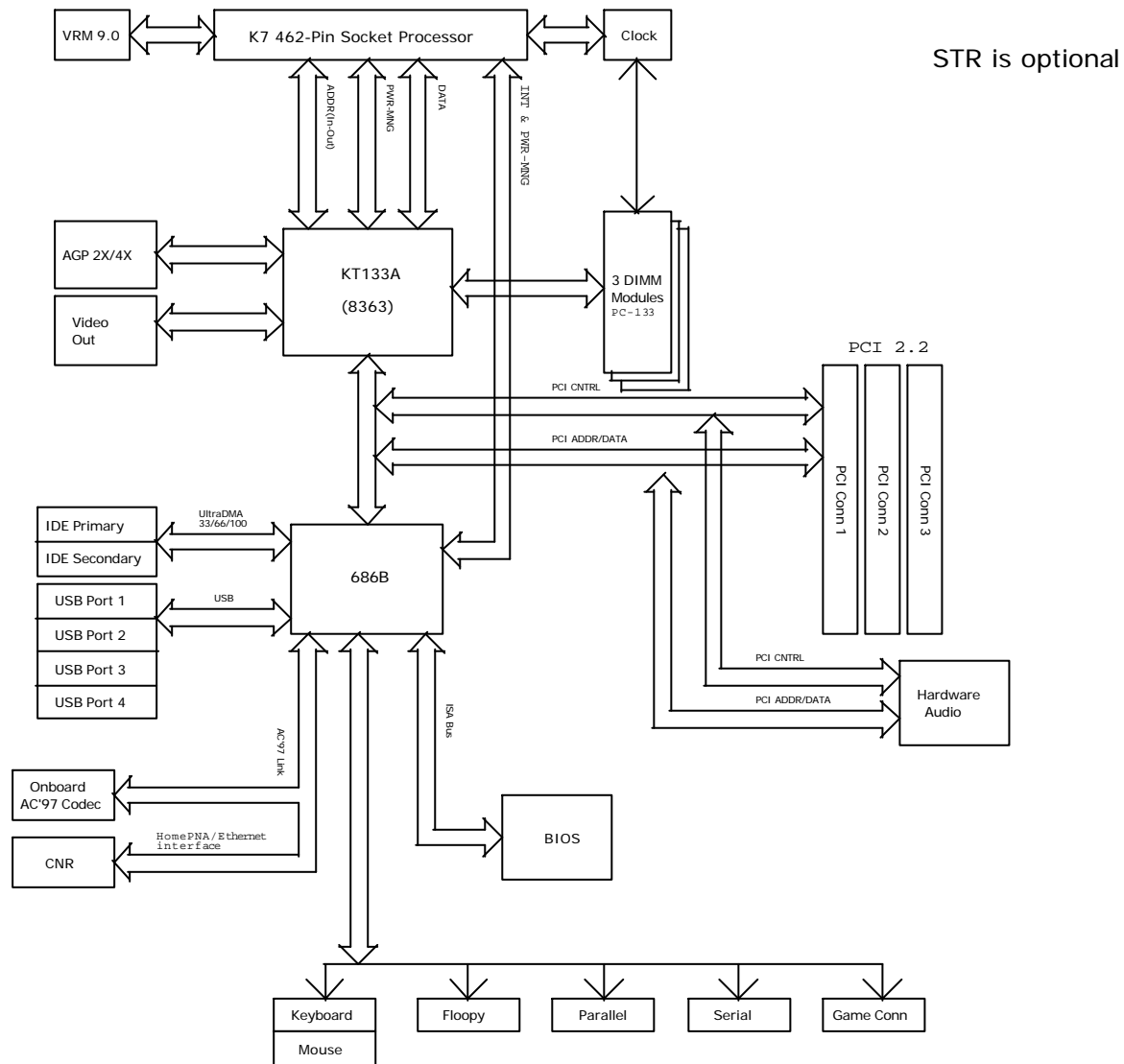
(South)
Expansion:
AGP SLOT* 1
PCI SLOT* 6
CNR SLOT* 1(Shared)

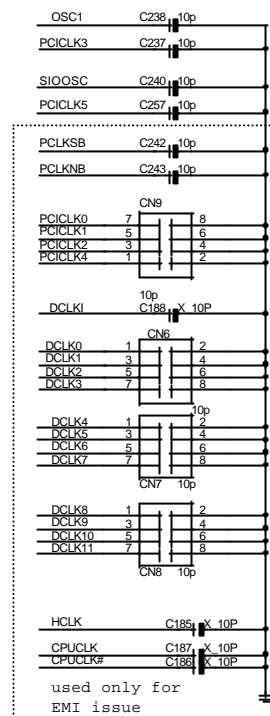
On Board: IDE RAID PDC20266

ON BOARD : AC97 CODEC

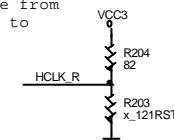
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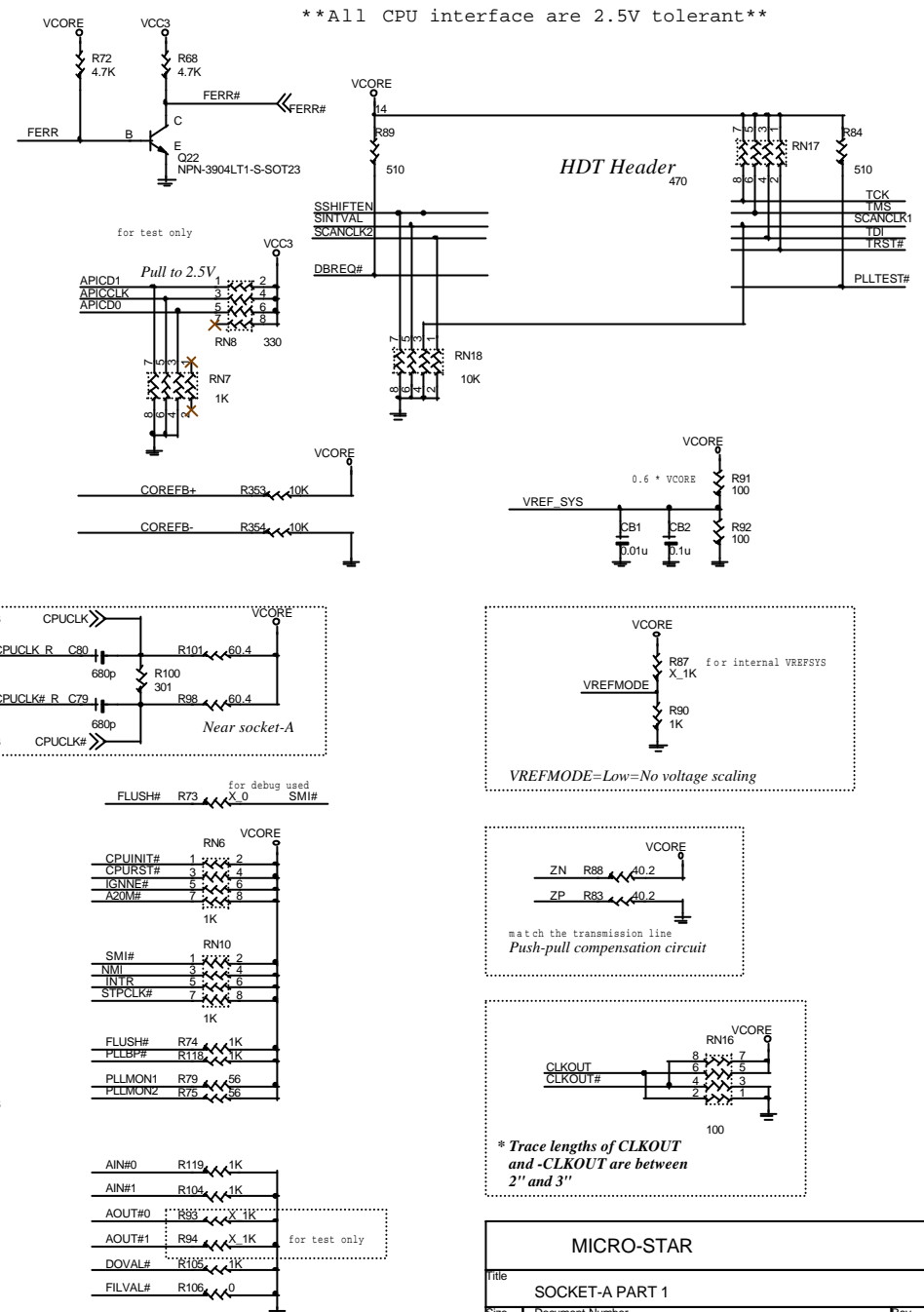
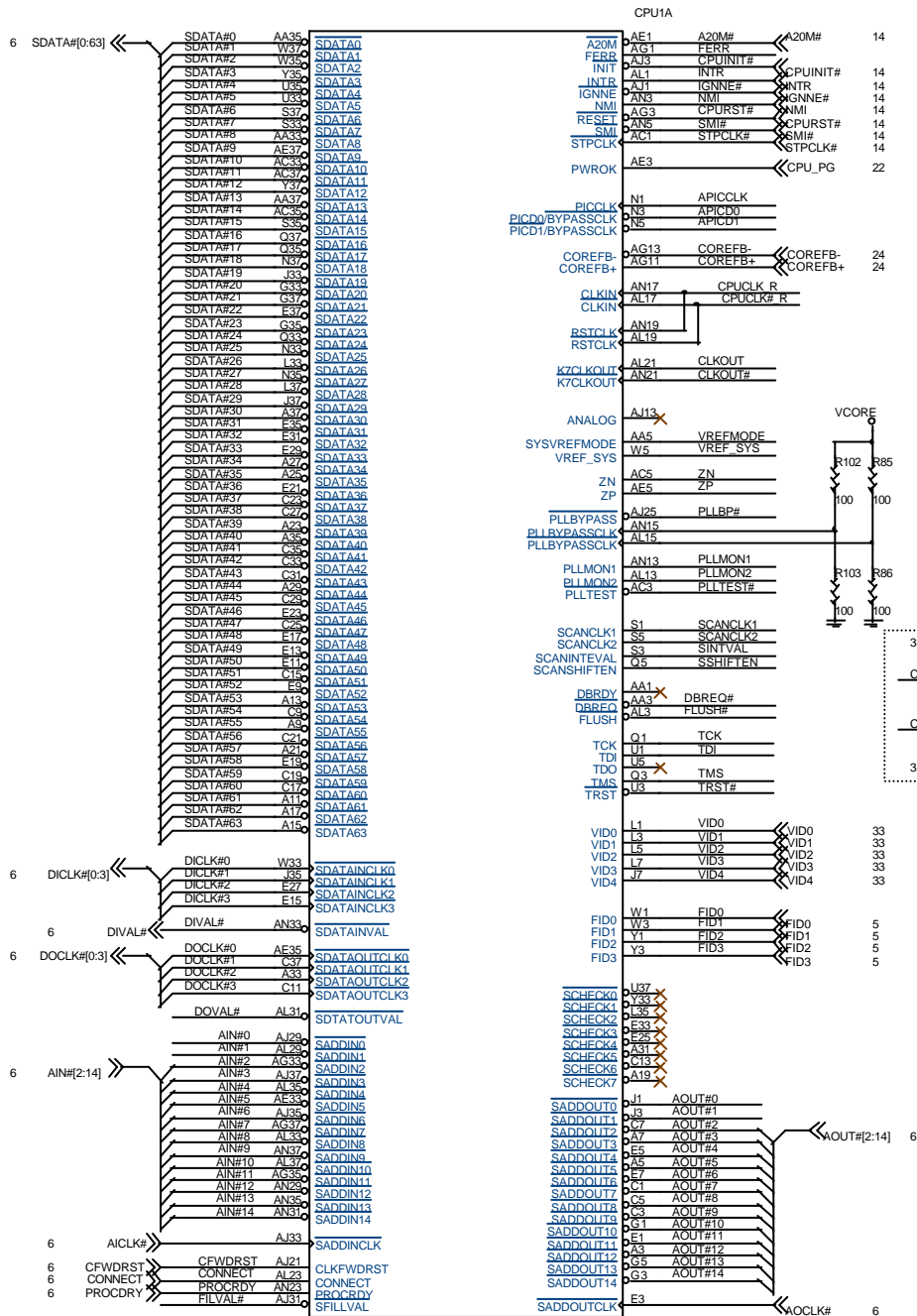
Block Diagram

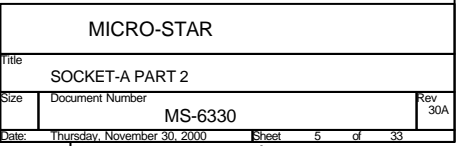


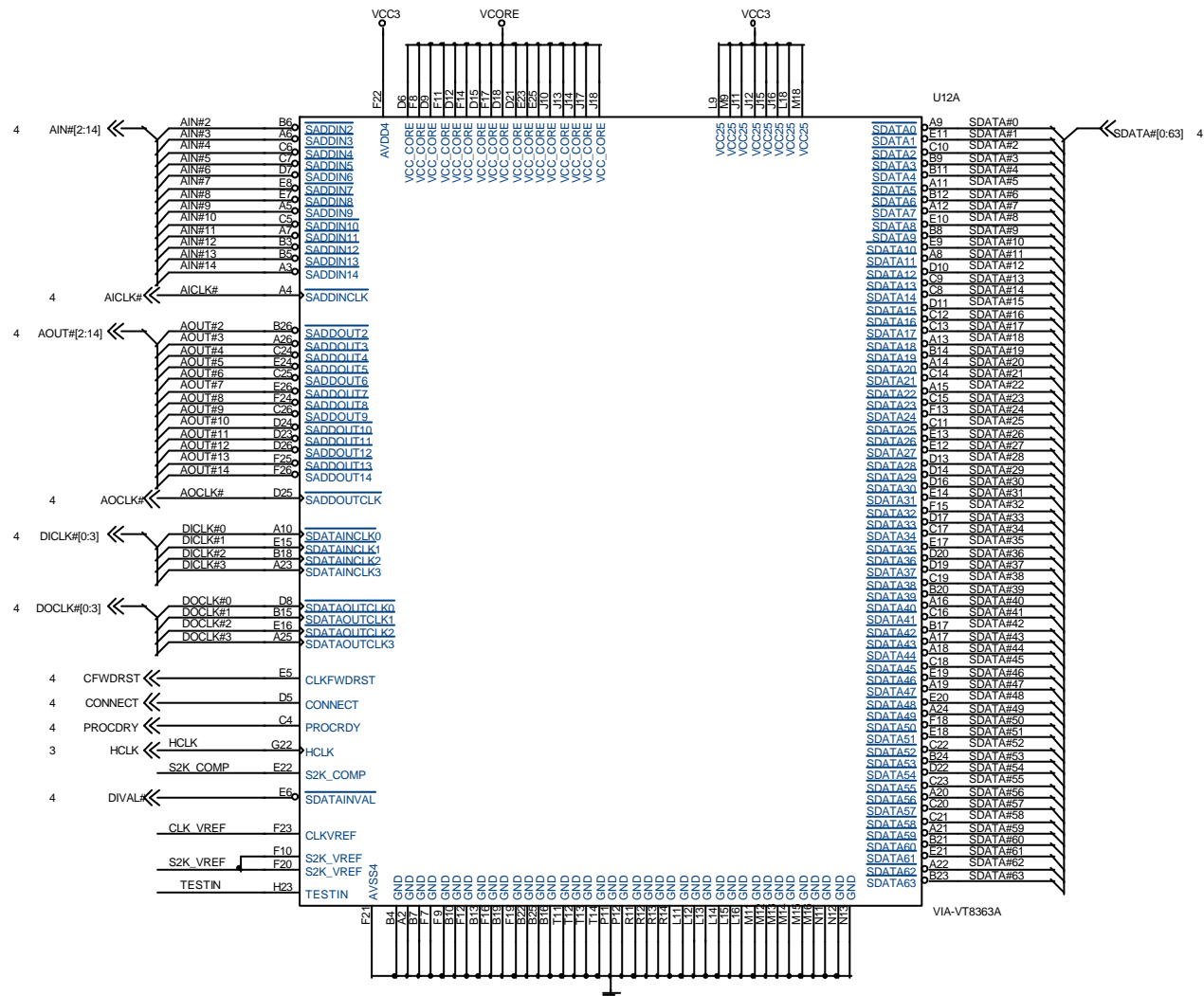


Range from
0.8V to
1.5V

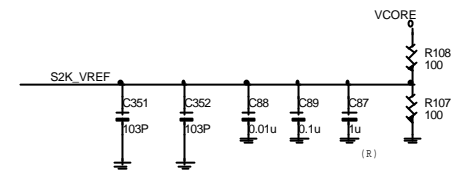




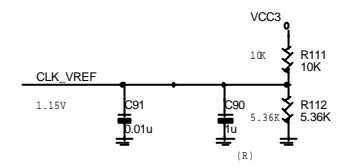




S2K_VREF at 60% @ 1.6V VREF = 0.96V



CLK_VREF at 60% @ 1.6V VREF = 0.96V



Populate R501 for S2KNCOMP of VT8365

Populate R208 for S2K_COMP (S2KNCOMP) of VT8363

VCCORE

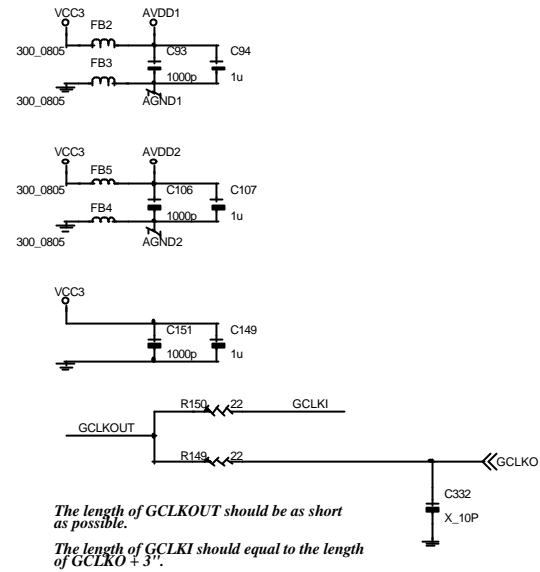
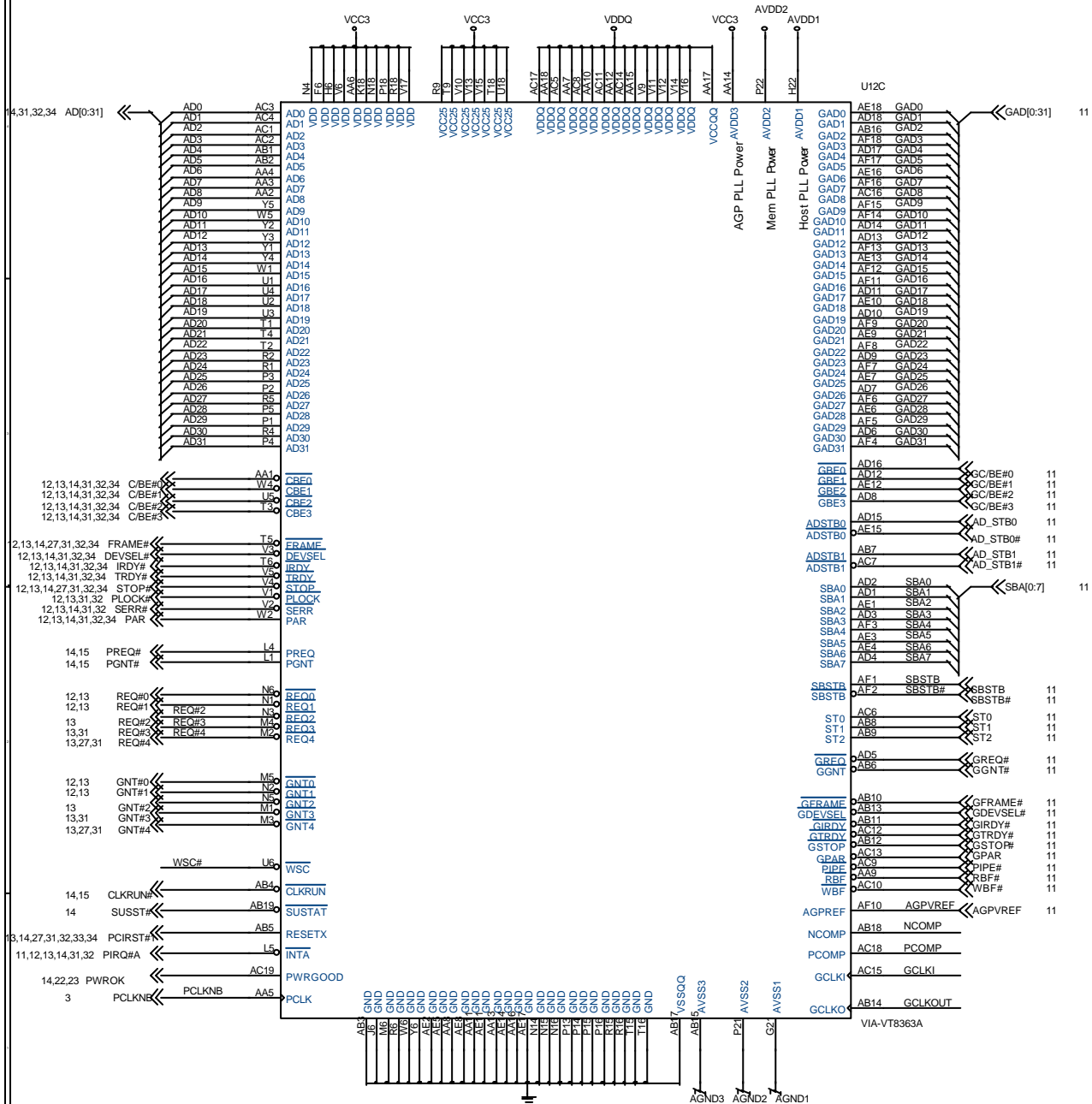
R109 X 60.4RST

S2KNCOMP S2K_COMP R110 40.2 (30~40 ohm)

R225=60 for S2KPCOMP of VT8365.

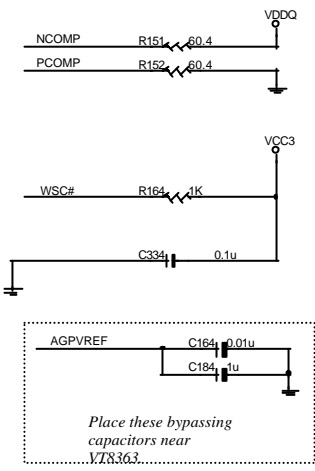
S2KPCOMP TESTIN R113 X 60.4RST

For TESTIN of VT8363: R225=4.7K in test mode. No population of R225 in normal mode

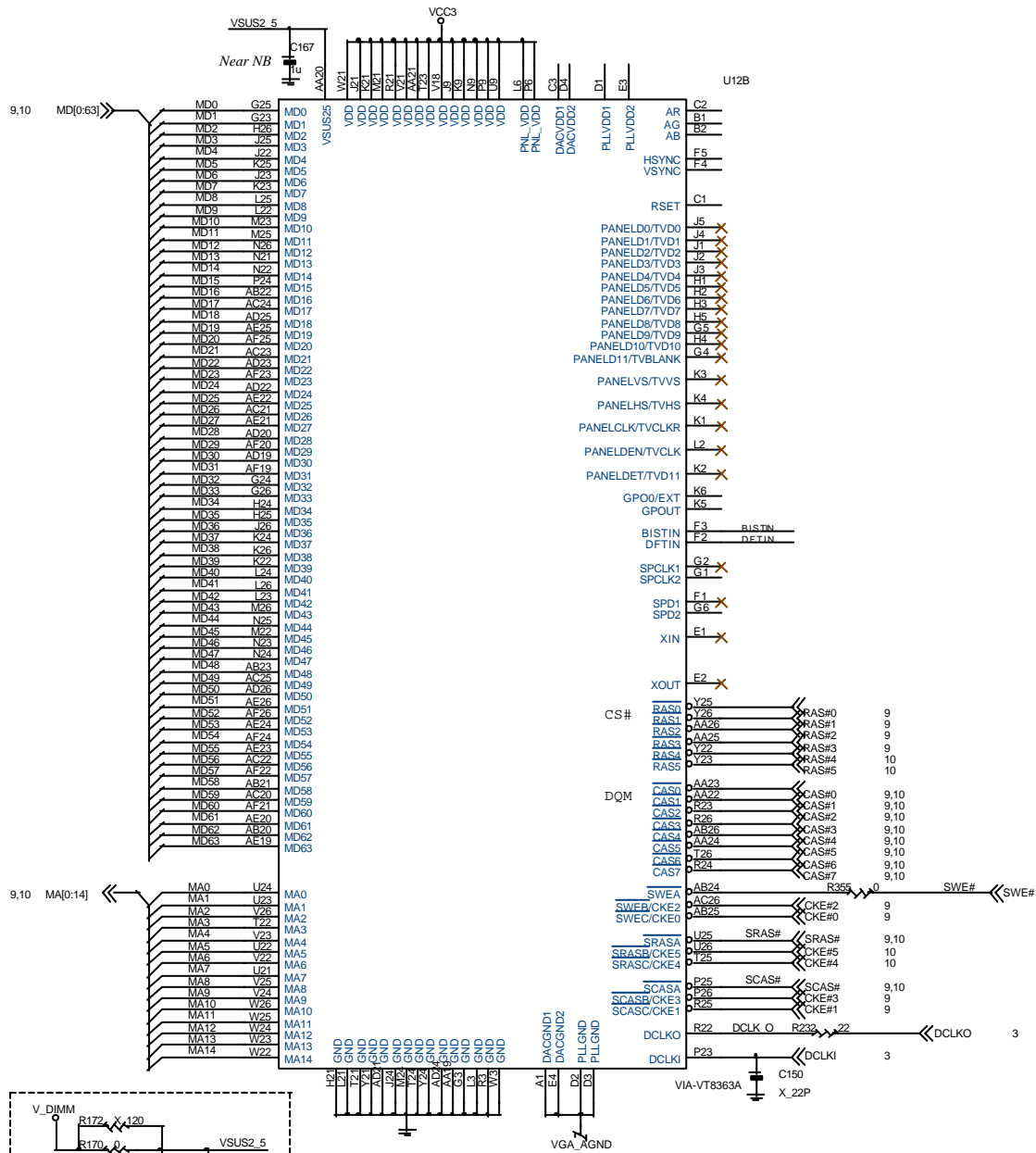


The length of GCLKOUT should be as short as possible.

The length of GCLKI should equal to the length of GCLKO + 3".



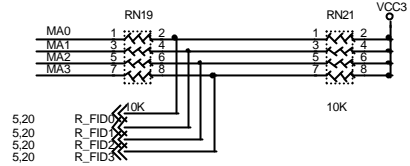
MICRO-STAR			
Title			
NORTH BRIDGE VT8363 (PCI & AGP)			
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Power Up Strappings: For Debug Only

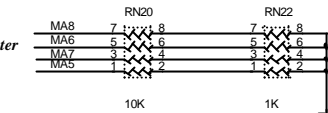
MA[3:0] => CPU Clock Divider

0000	3	1000	7
0001	3.5	1001	7.5
0010	4	1010	8
0011	4.5	1011	8.5
0100	5	1100	9
0101	5.5	1101	9.5
0110	6	1110	10
0111	6.5	1111	Reserved



MA[8:4] => S2K Strobe Delay Counter in Edge Mode

00000 - Auto Mode (Default)
00001-11111 - Strapping Mode



-SRAS => S2K Slew Rate Control

1 - Slew Rate Control Disable
0 - Slew Rate Control Enable (Default)

MA[14] => CPU Clock Frequency

0 - 133MHz (Default)

MA[13:12] => Internal Pull-Up Strength

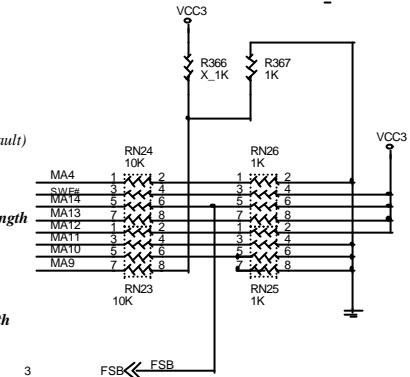
11 - Auto Mode
00-10 - Strapping mode

MA[11] => S2K DQ Select

0 - Central DQ (Default)
1 - Edge DQ

MA[10:9] => Output Driving Strength

01-11 - Auto Mode
0 - Disable (Default)

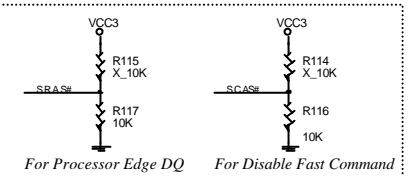


-SWE => Processor DQ Select

1 - Center DQ
0 - Edge DQ (Default)

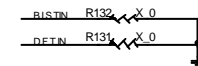
-SCAS => Fast Command Select

1 - Enable
0 - Disable (Default)



For Processor Edge DQ

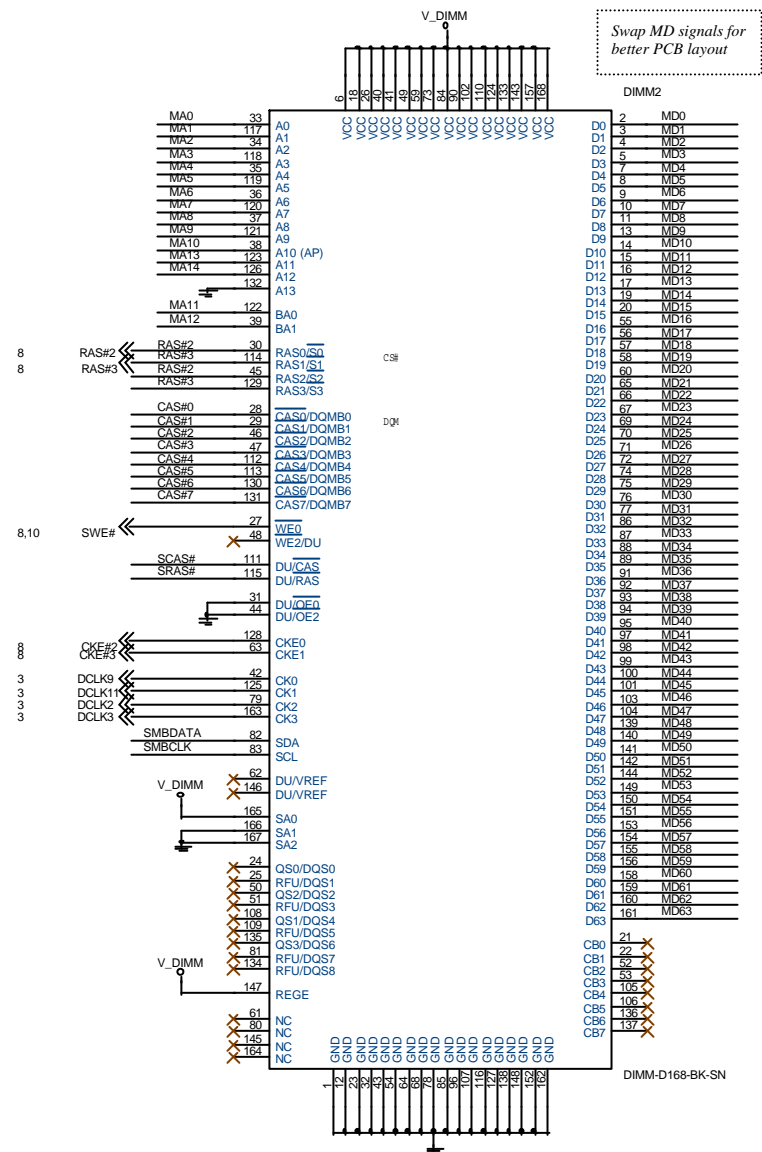
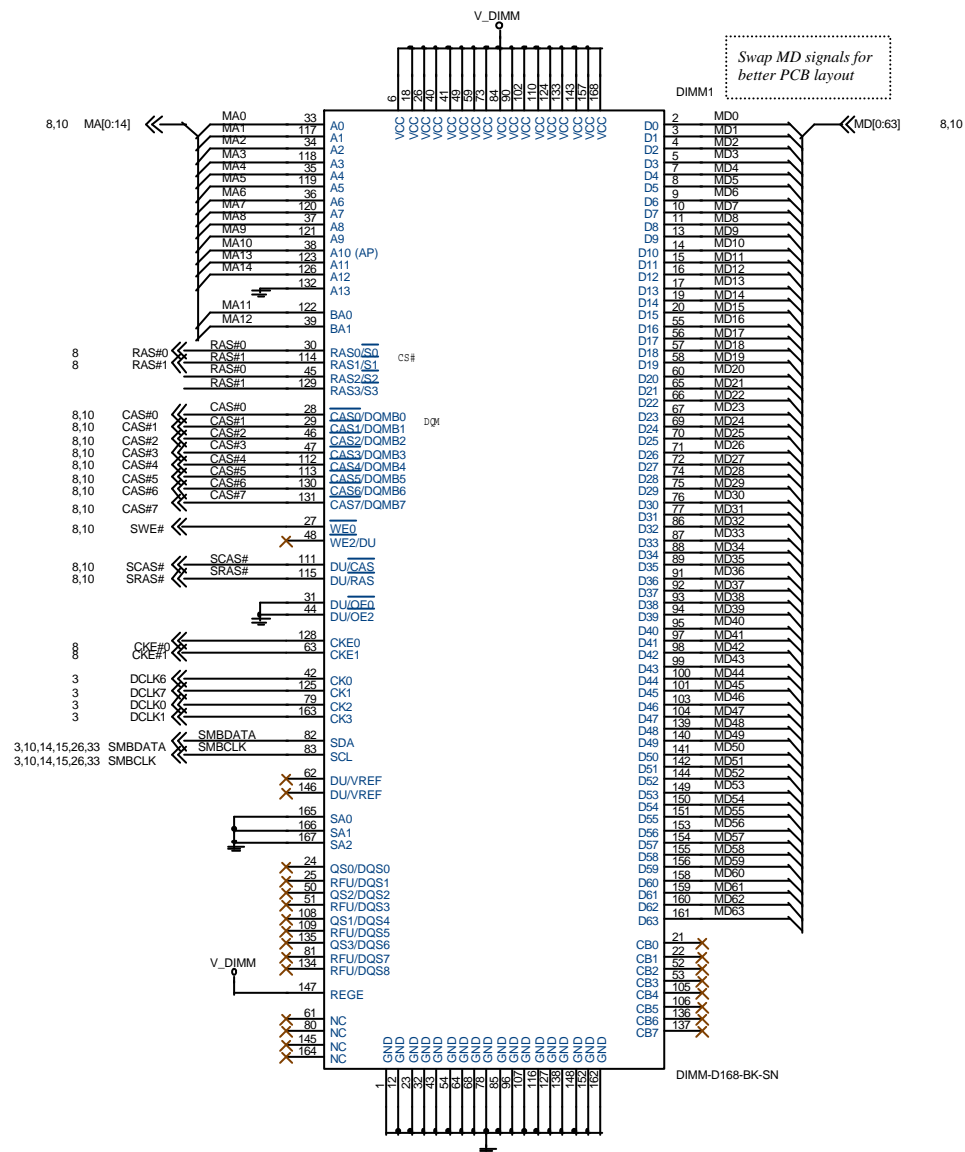
For Disable Fast Command

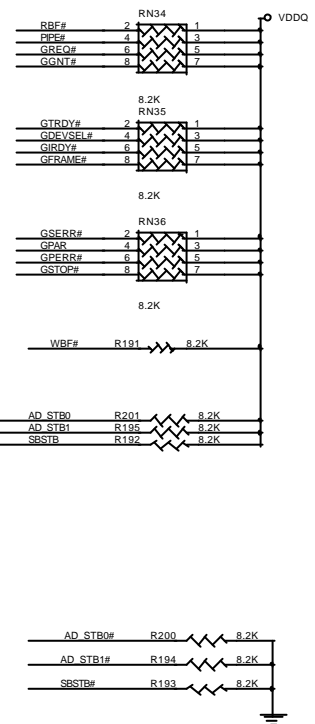
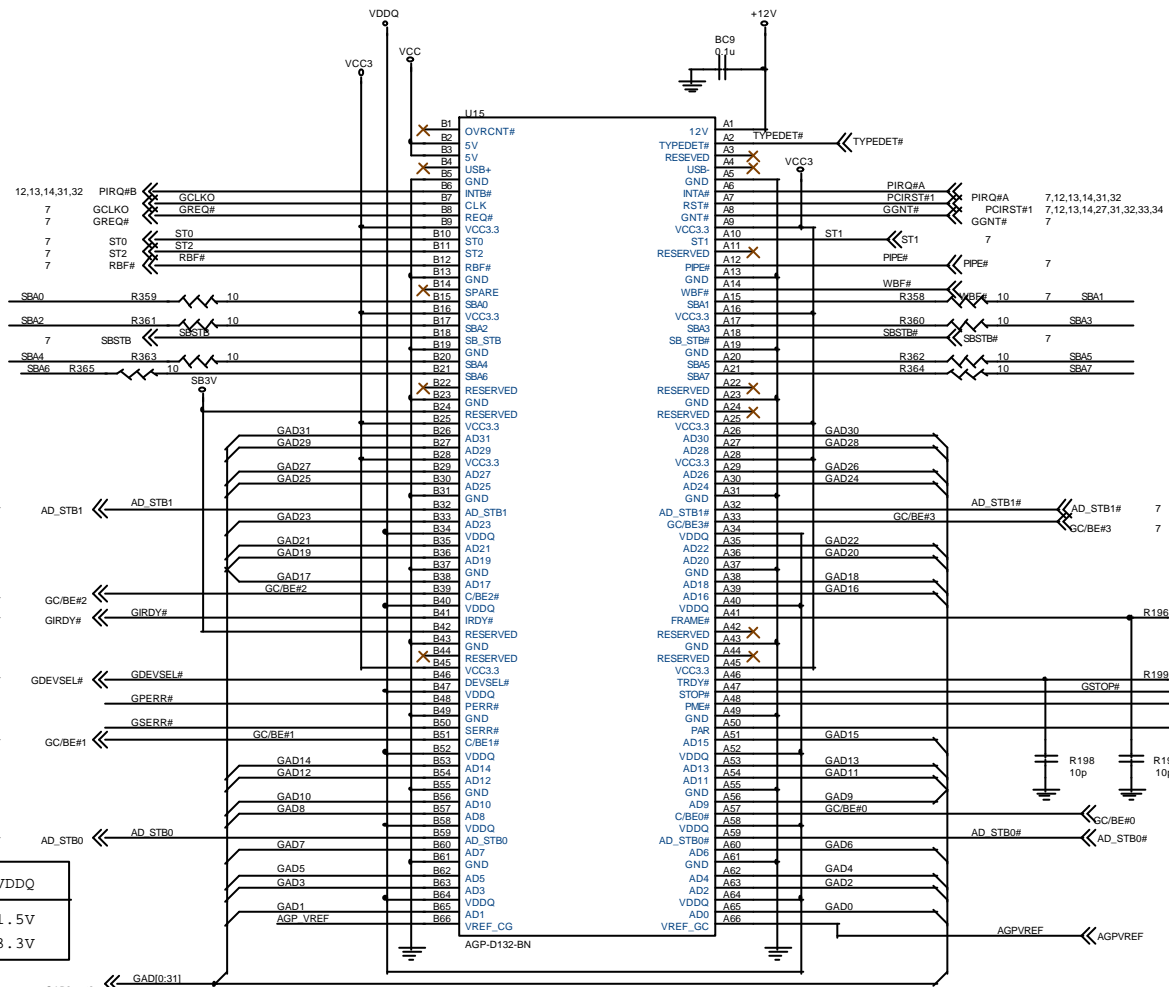


MICRO-STAR

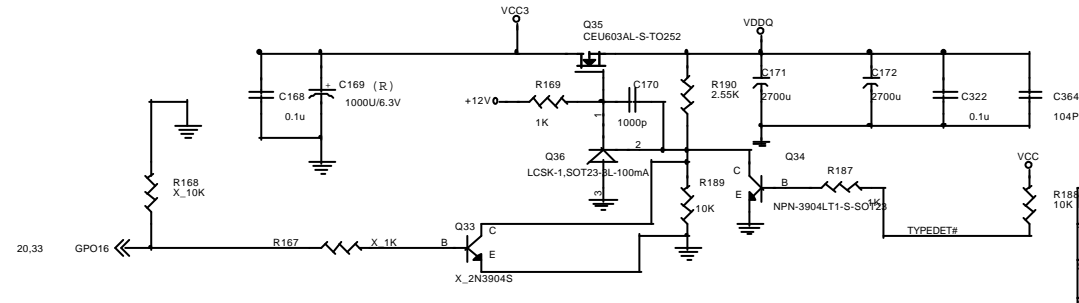
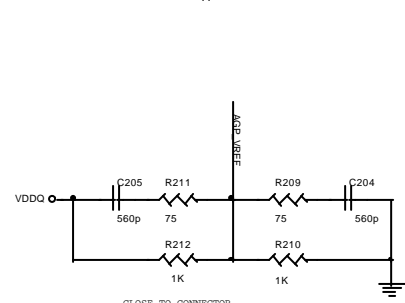
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VSUS2_5=3.3V for VT8363
(R238[120ohm(OPT)], R239[0ohm],
R233[0ohm(OPT)], D20(OPT))
VSUS2_5=2.5V for VT8365
(R238[120ohm], R239[120ohm],
R233[0ohm], D20)

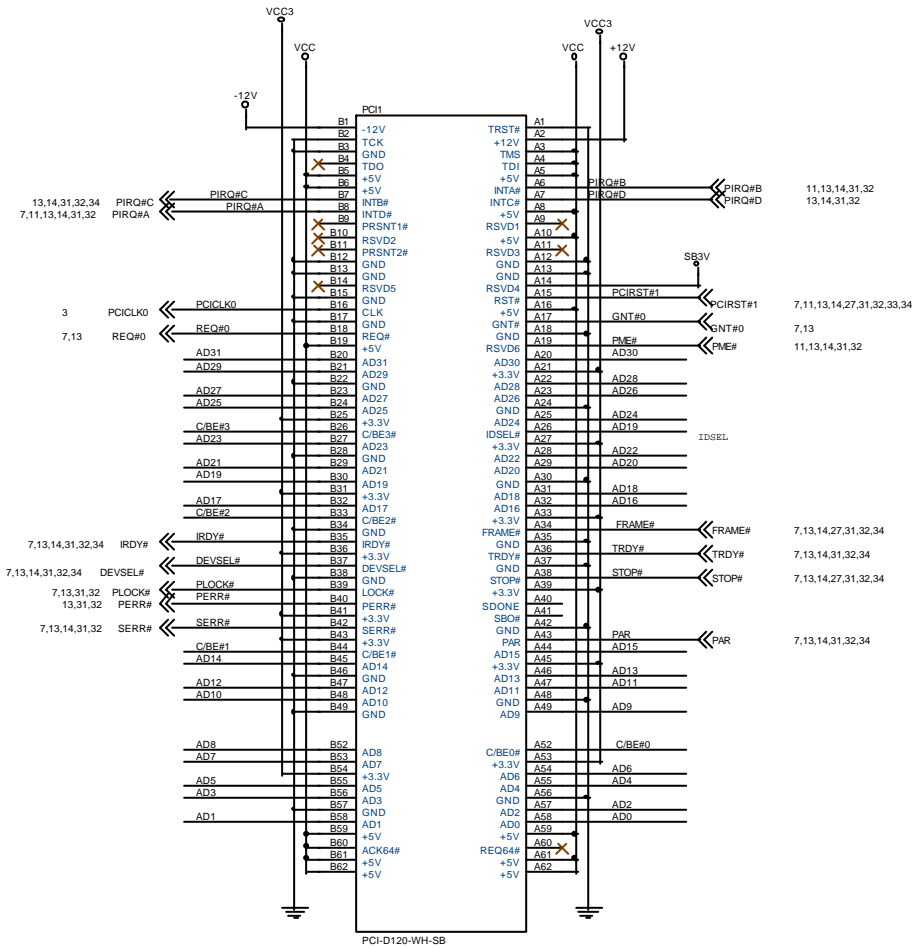




TYPEDET#	VDDQ
Low	1.5V
High	3.3V



7,13,14,31,32,34 AD[0:31] << AD[0:31]
7,13,14,31,32,34 C/BE#[0:3] << C/BE#[0:3]

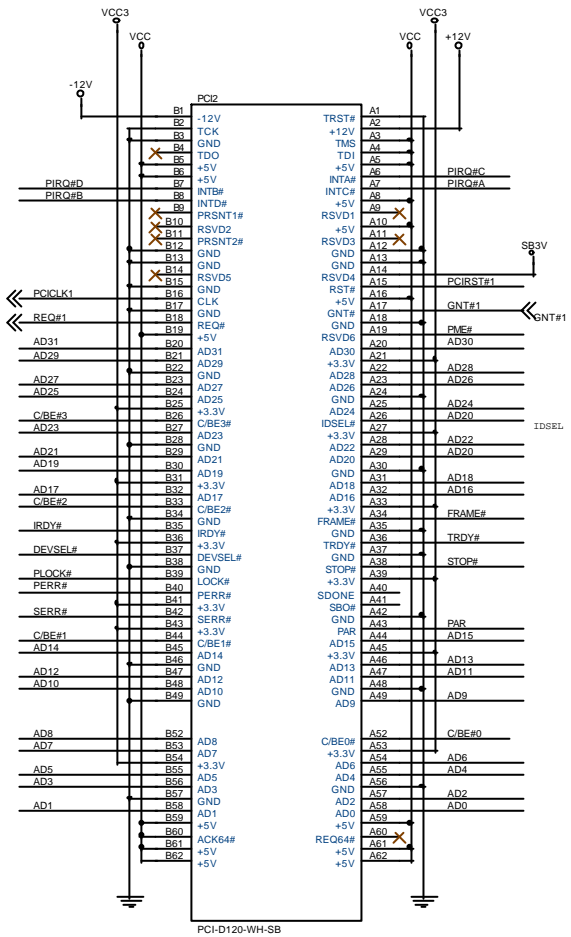


11,13,14,31,32
13,14,31,32

7,11,13,14,27,31,32,33,34
7,13
11,13,14,31,32

7,13,14,27,31,32,34
7,13,14,31,32,34
7,13,14,27,31,32,34

7,13,14,31,32,34

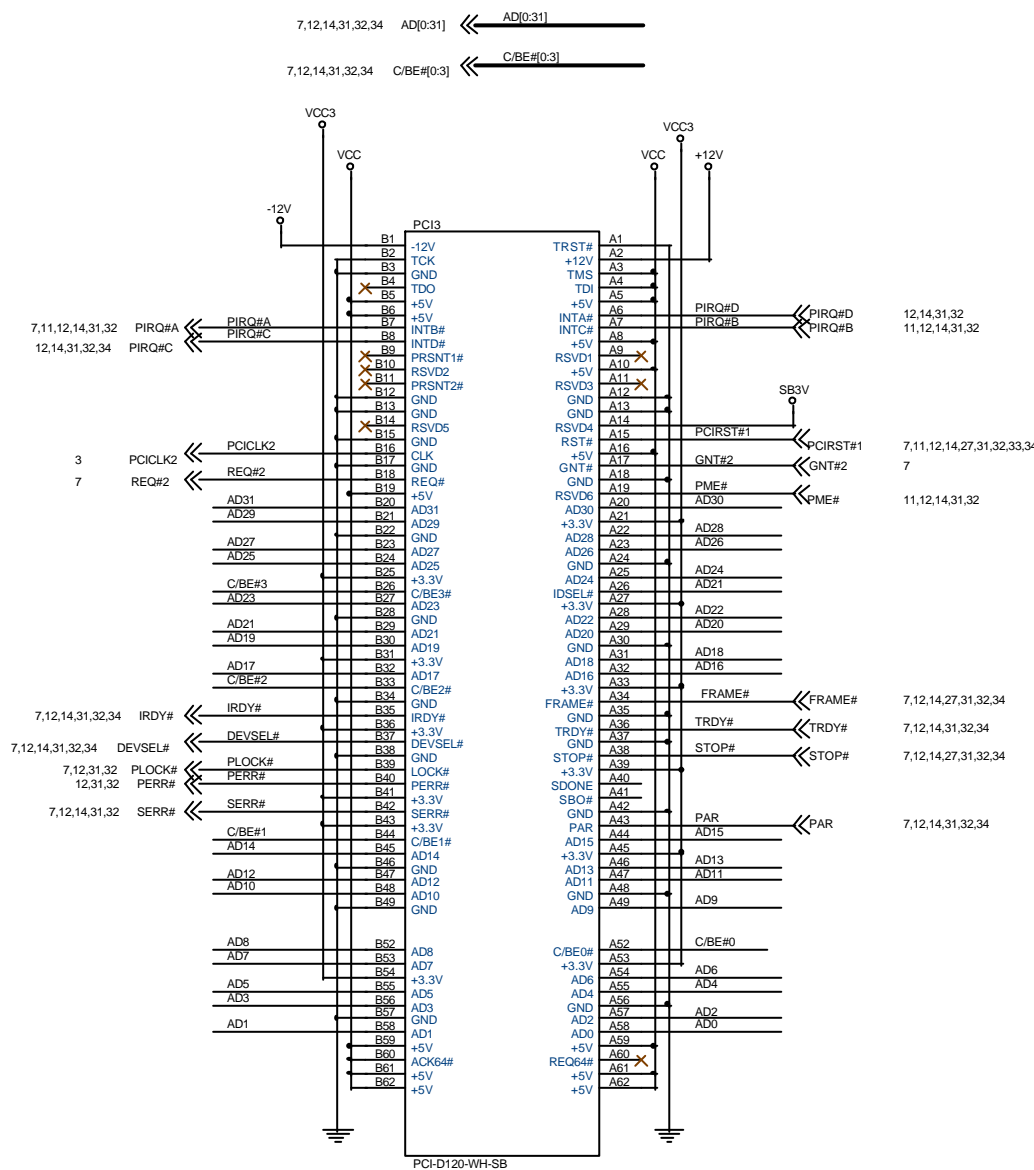


7,13

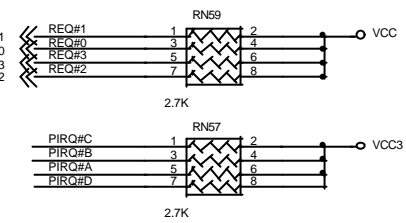
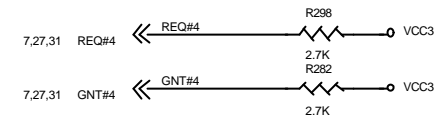
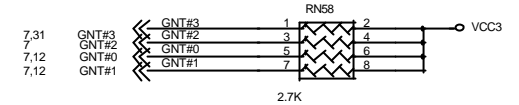
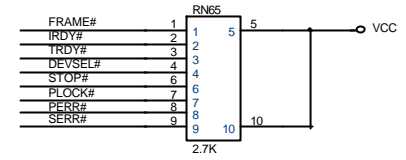
IDSEL

MICRO-STAR

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PCI 1 & 2			
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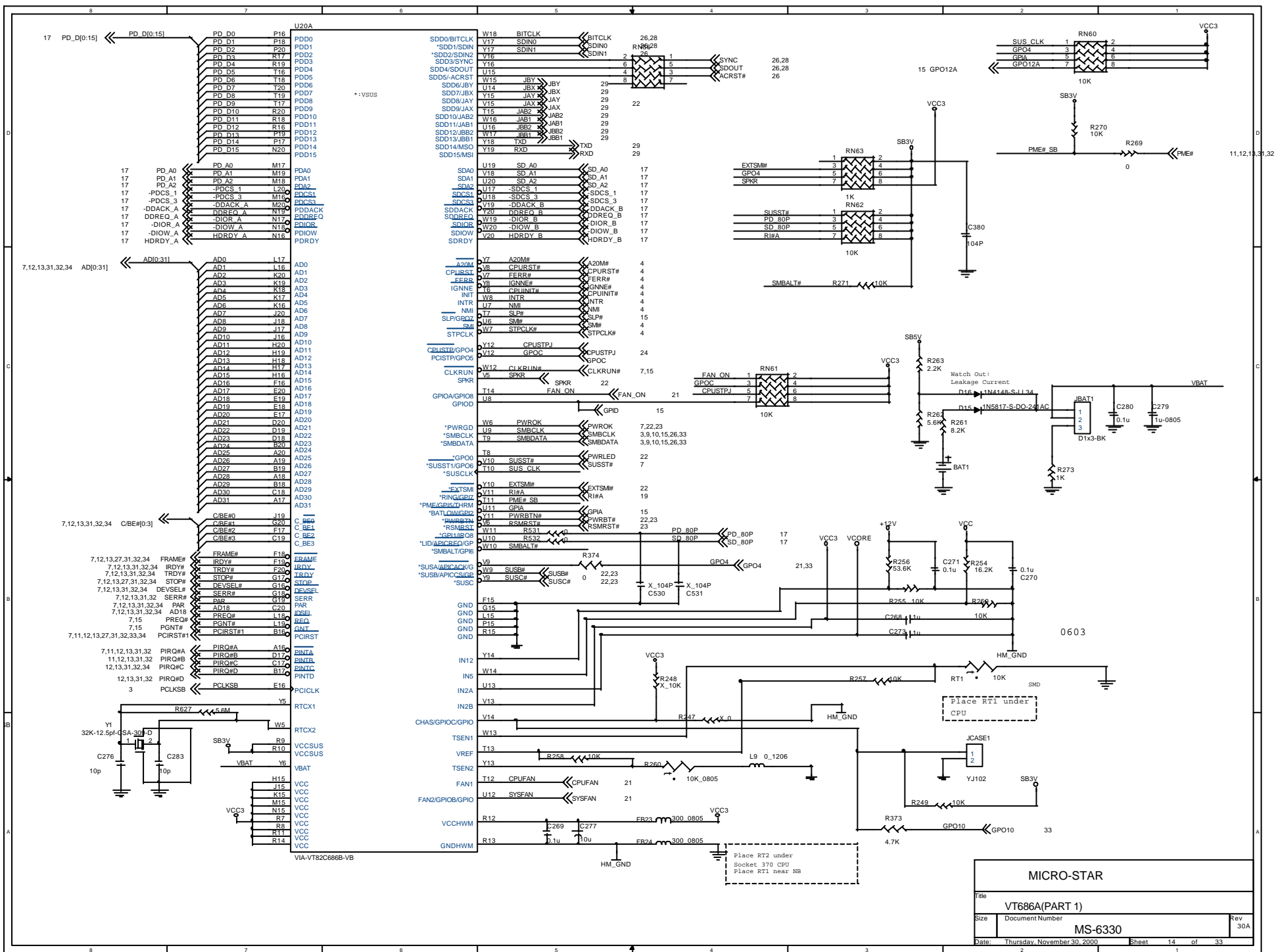


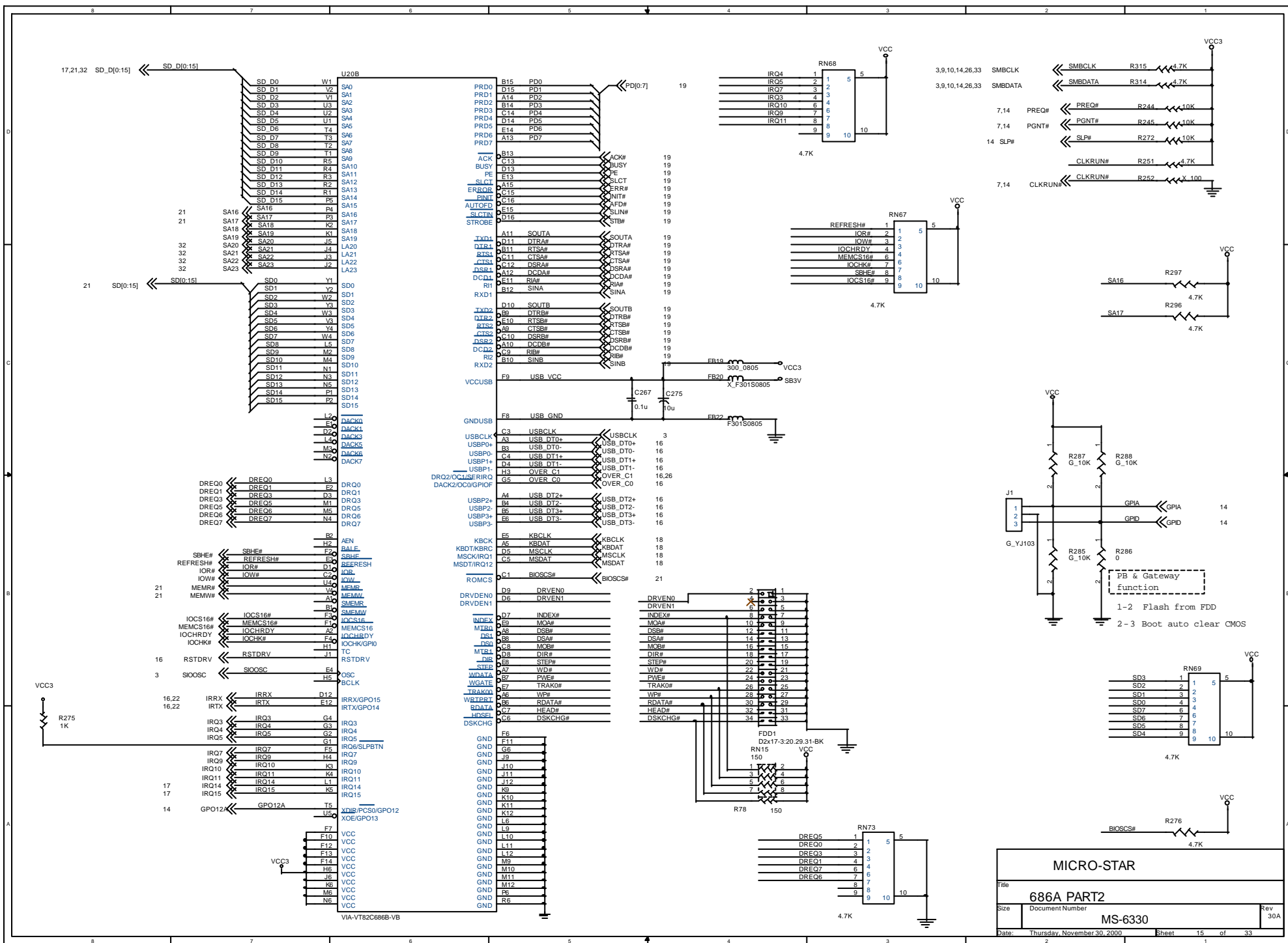
PCI

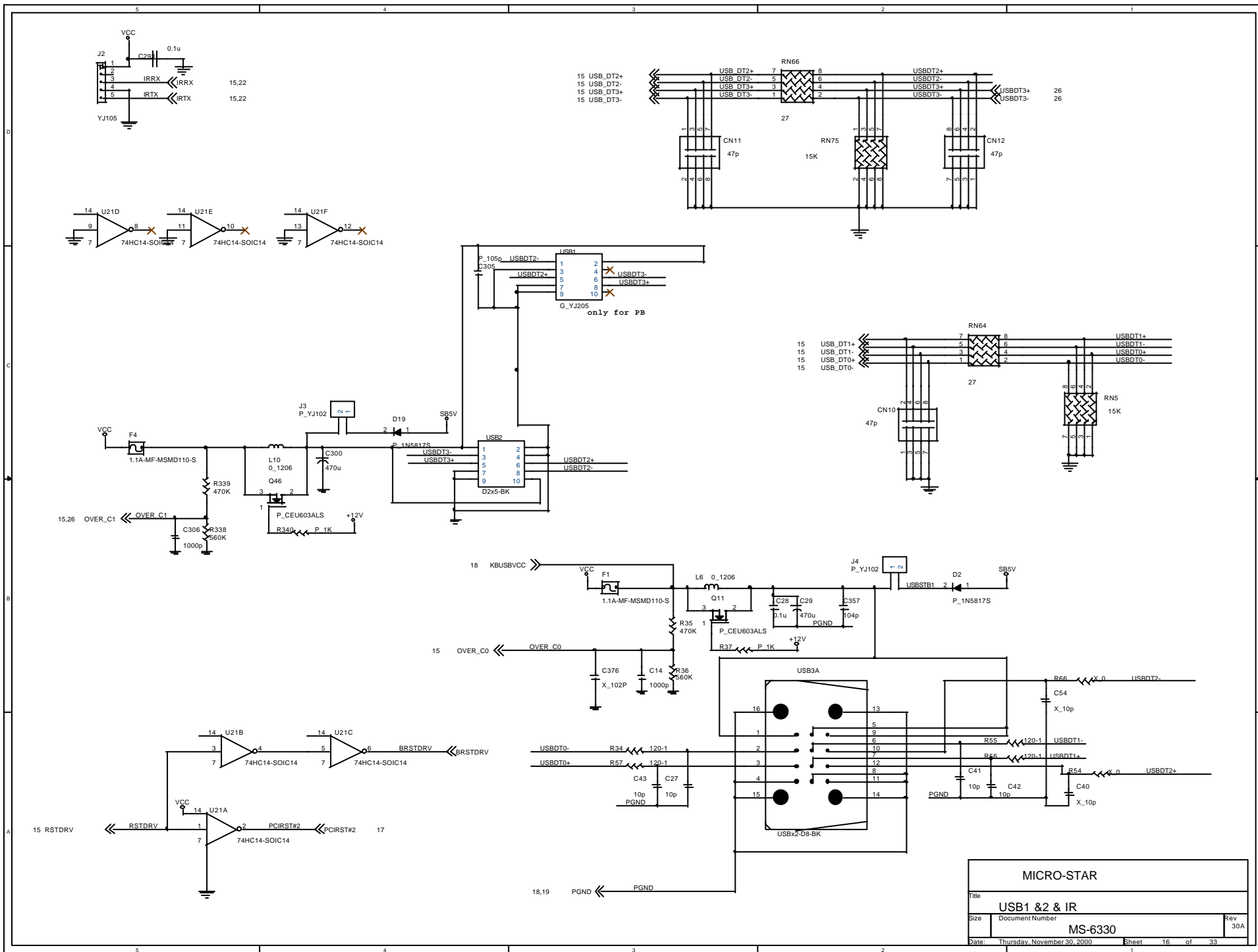


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PCI 3			
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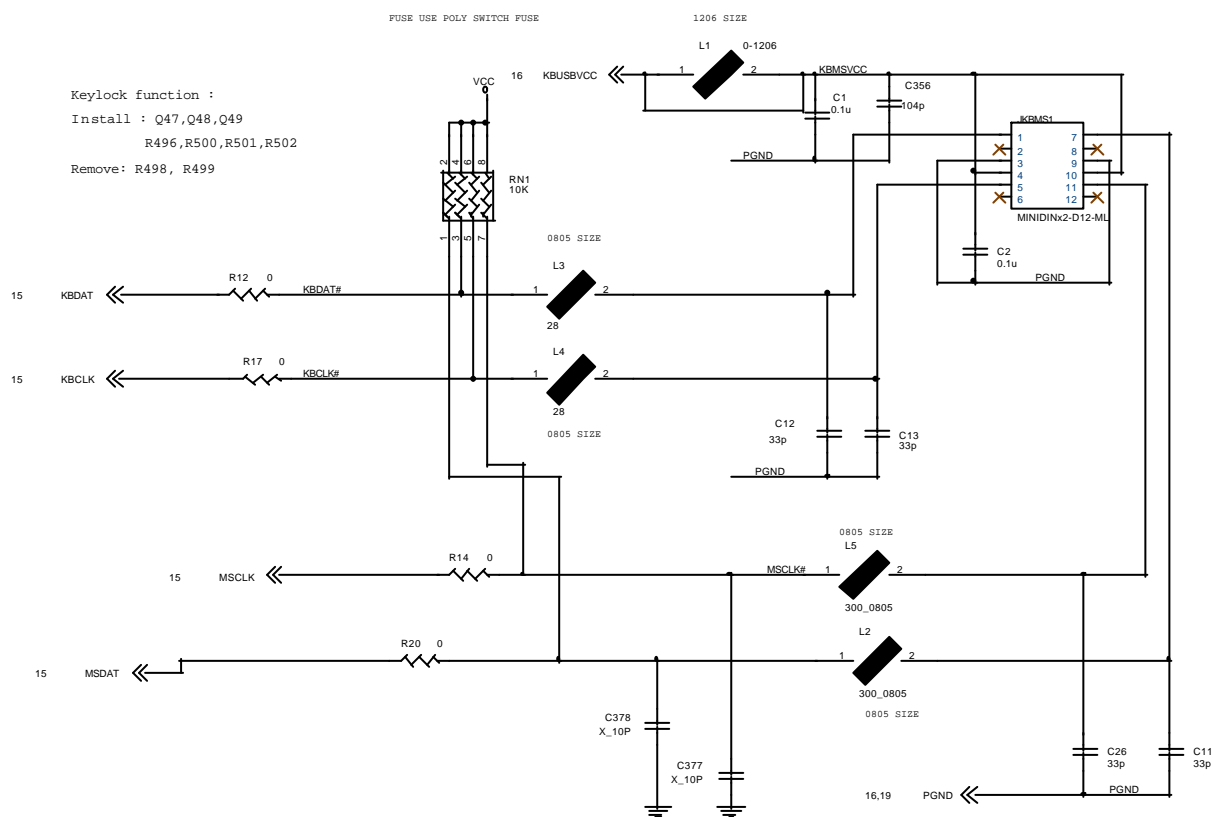
MICRO-STAR			
Title		USB1 & 2 & IR	
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Keylock function :

Install : Q47,Q48,Q49

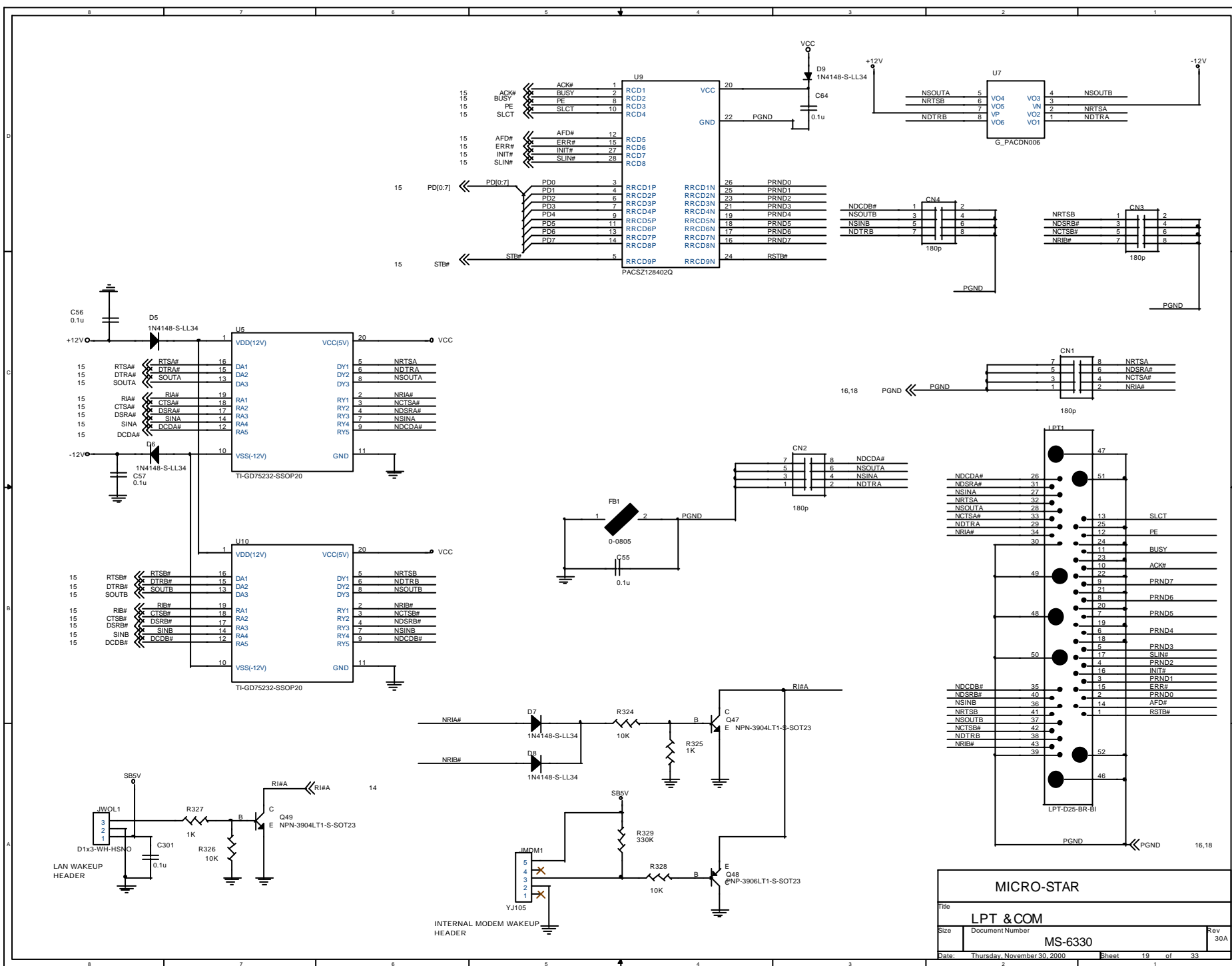
R496,R500,R501,R502

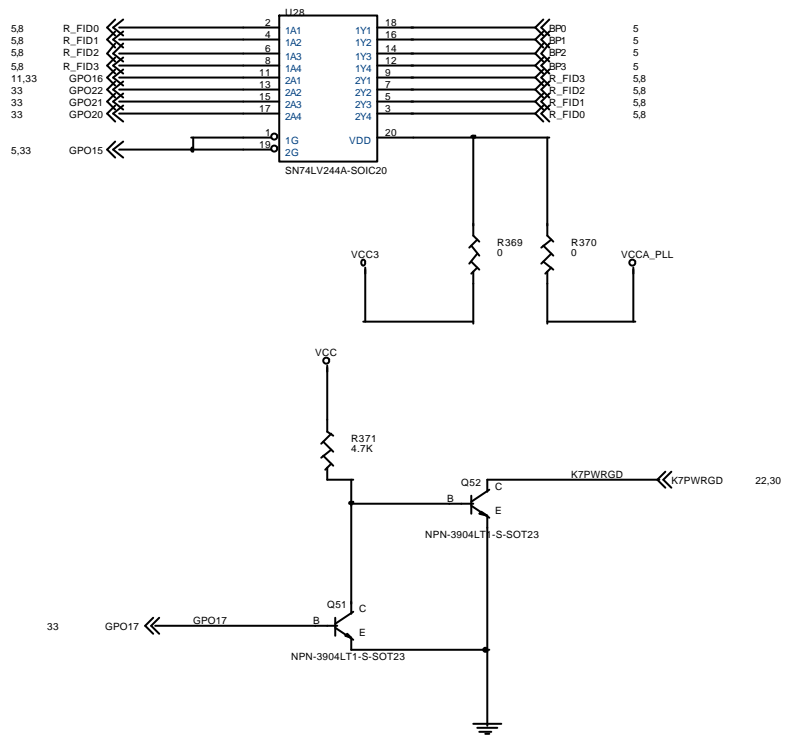
Remove: R498, R499



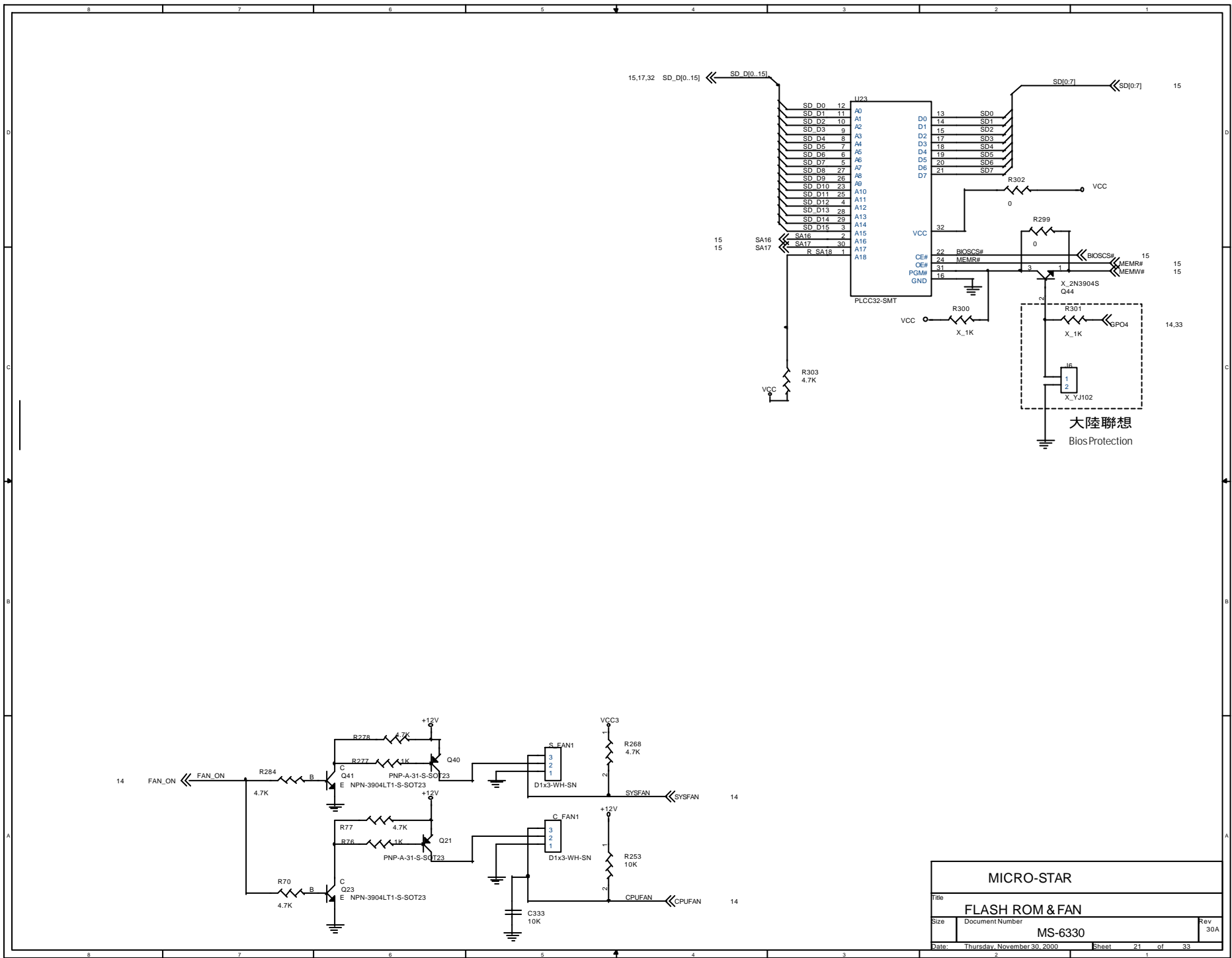
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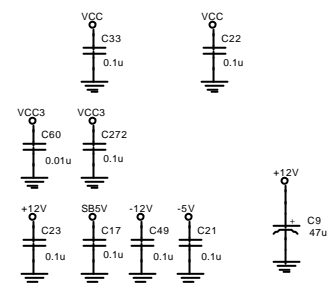
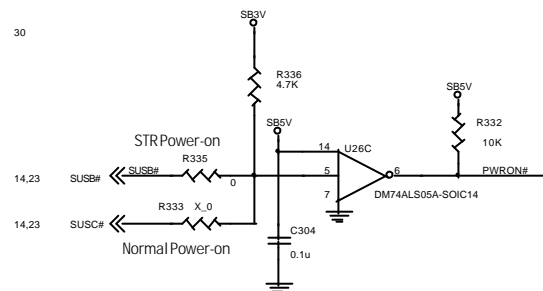
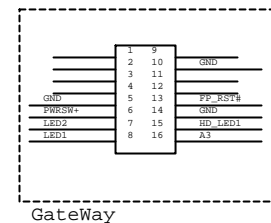
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USB 3&4 & KEYBOARD		
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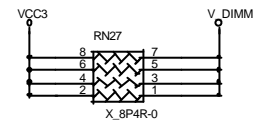
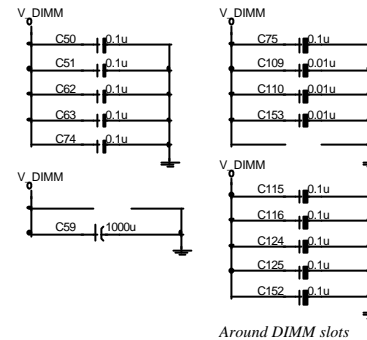
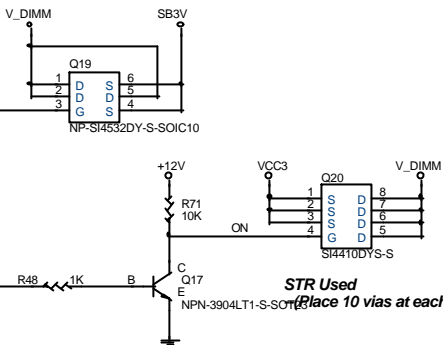


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JUMPERLESS RATIO		
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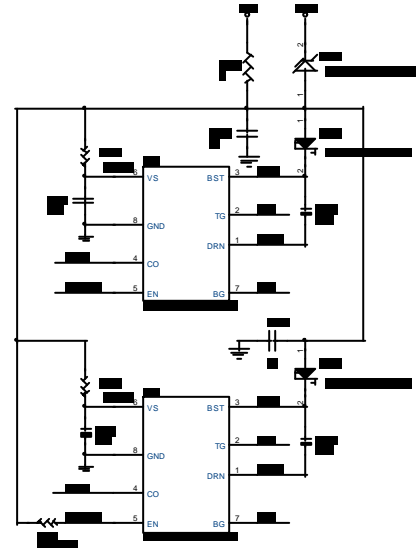
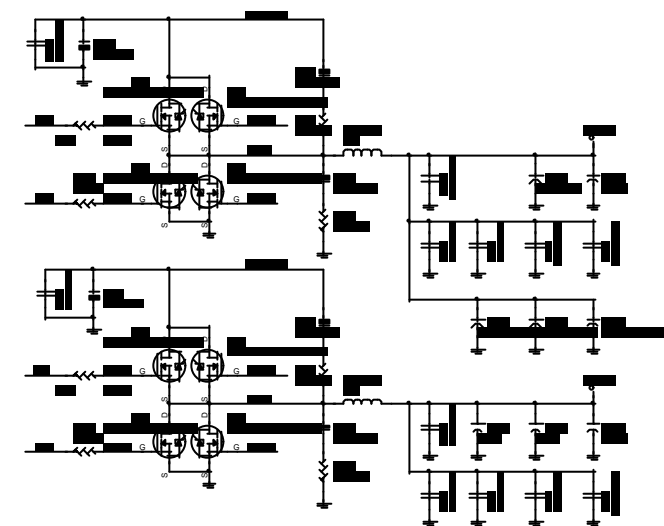
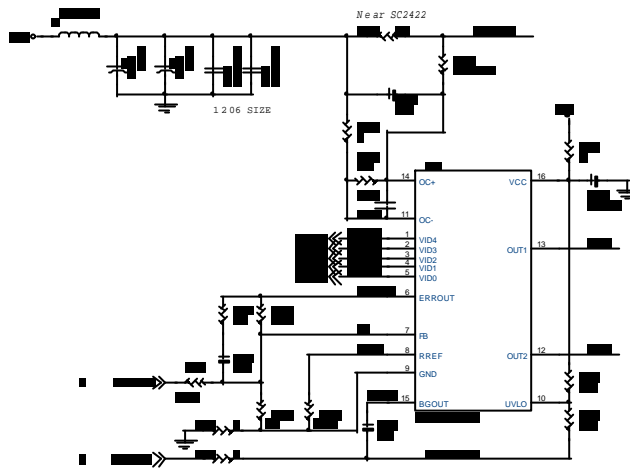
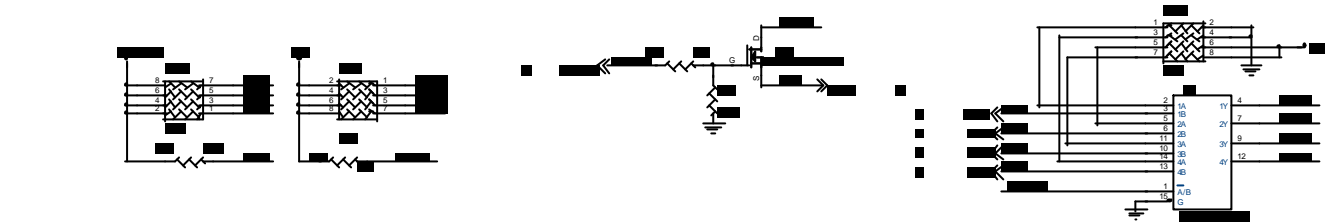
Put near ATX Power Connector
For EMI issue



3.3V or 2.5V Supply to VCC25 of NB

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Voltage Regular Module



Route COREFB and COREFB#
differentially at 15mil
width

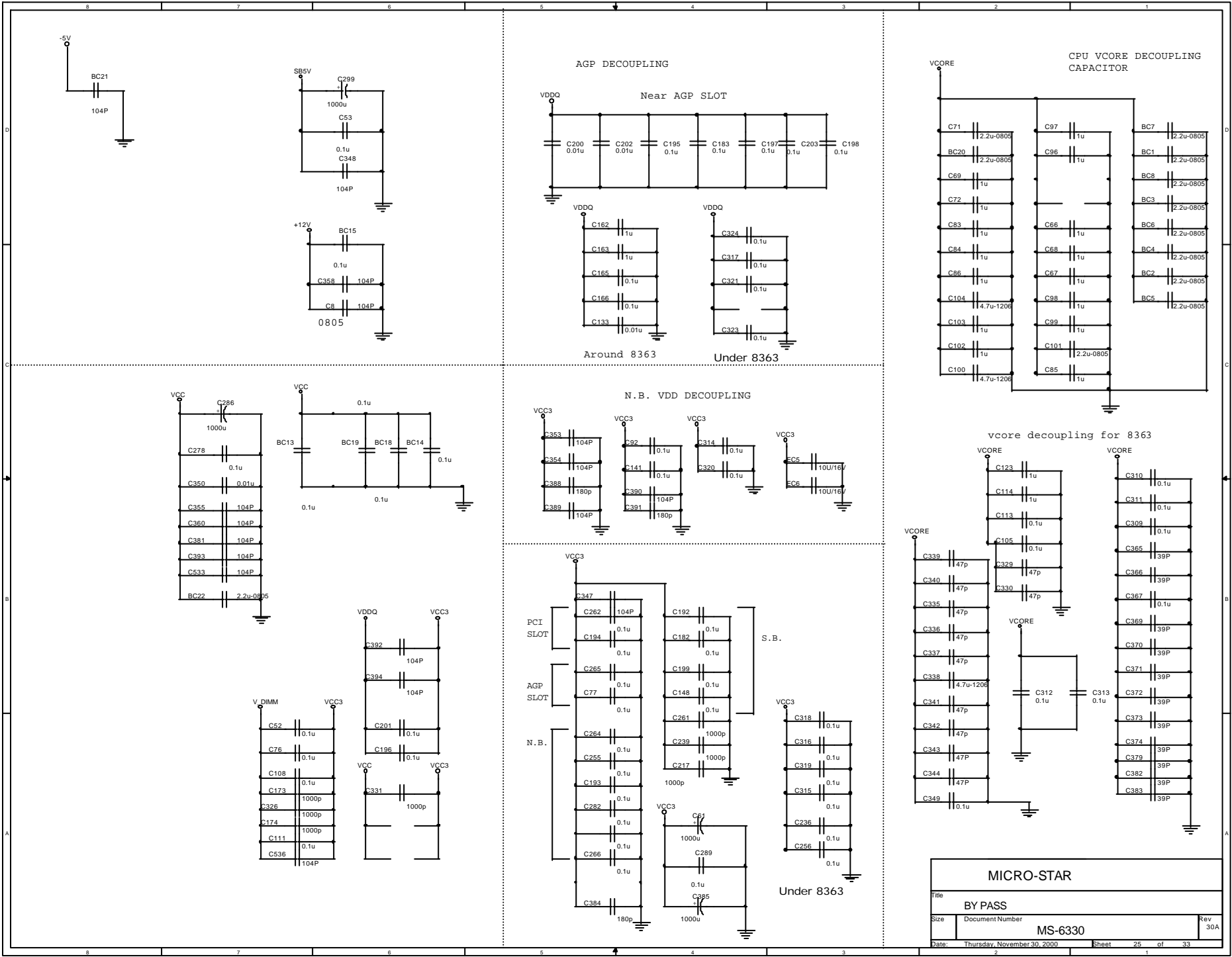
VID4	VID3	VID2	VID1	VID0	VDC(V)
1	0	1	1	0	1.30
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	0	1	1	0	1.70
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.80
0	0	0	0	1	1.825
0	0	0	0	0	1.85
1	1	1	1	1	NO CPU

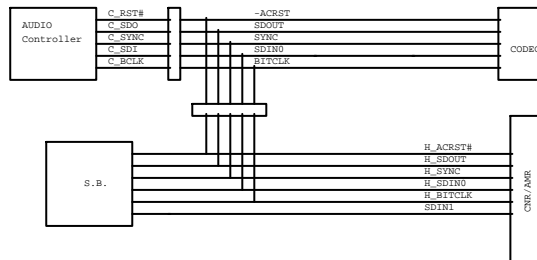
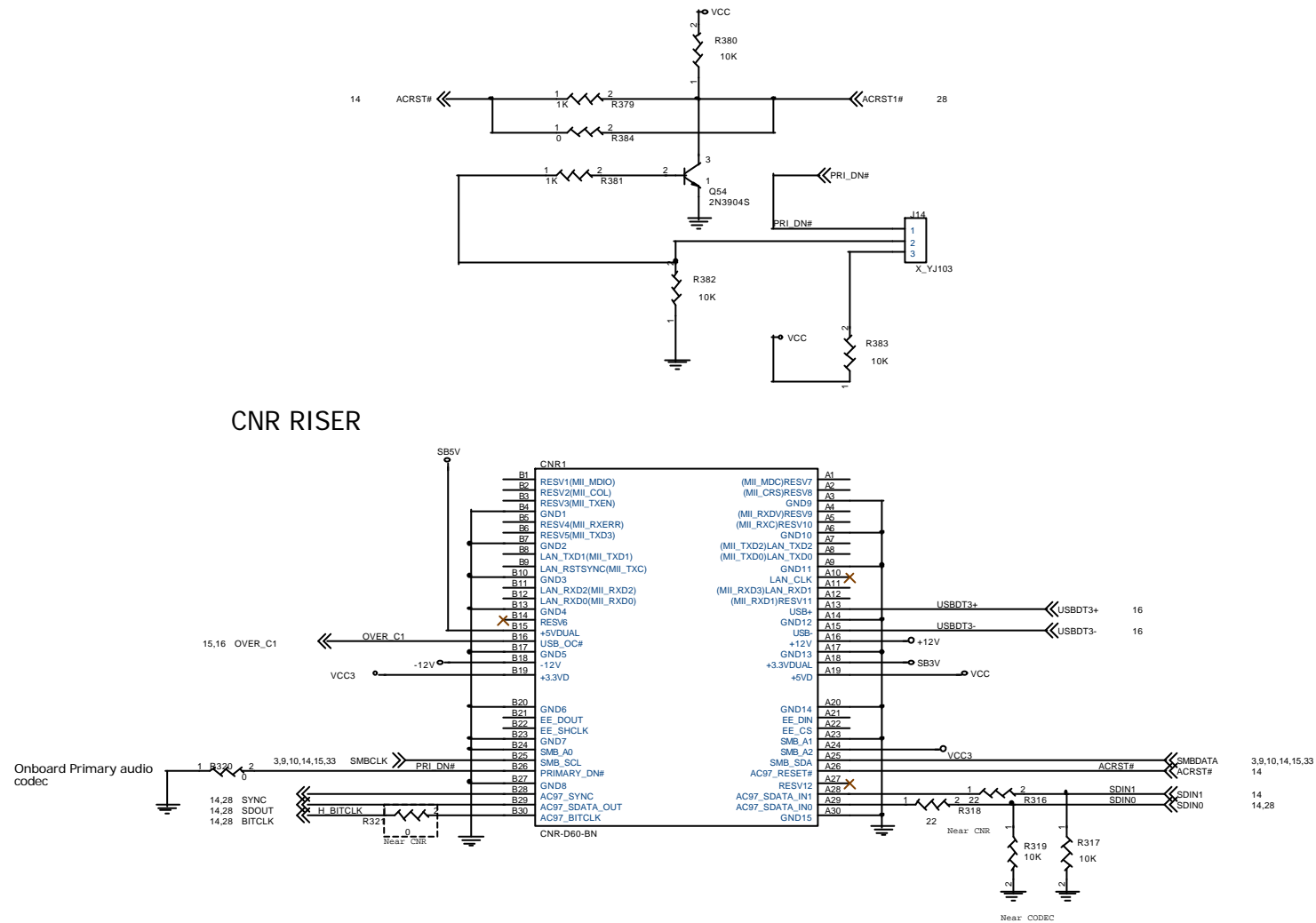
MICRO-STAR

SC2422

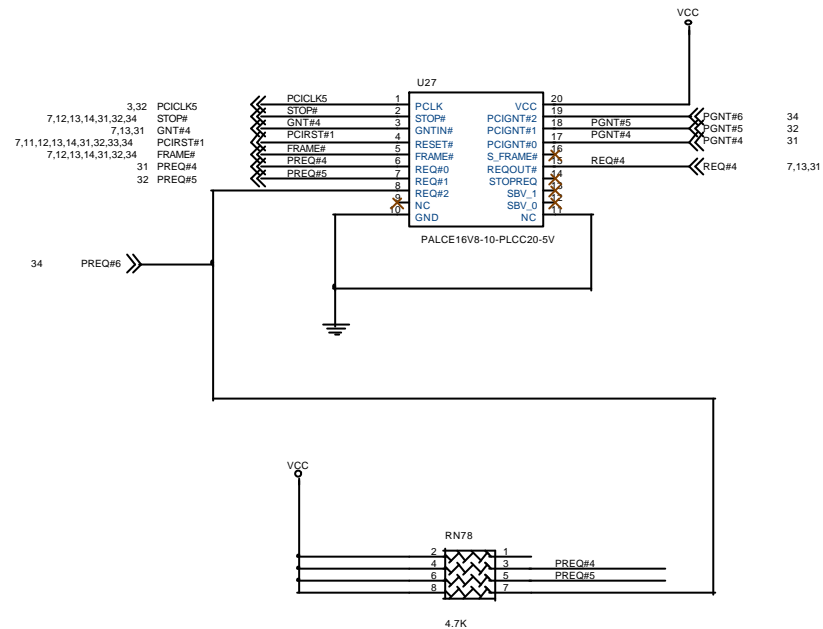
MS-6330



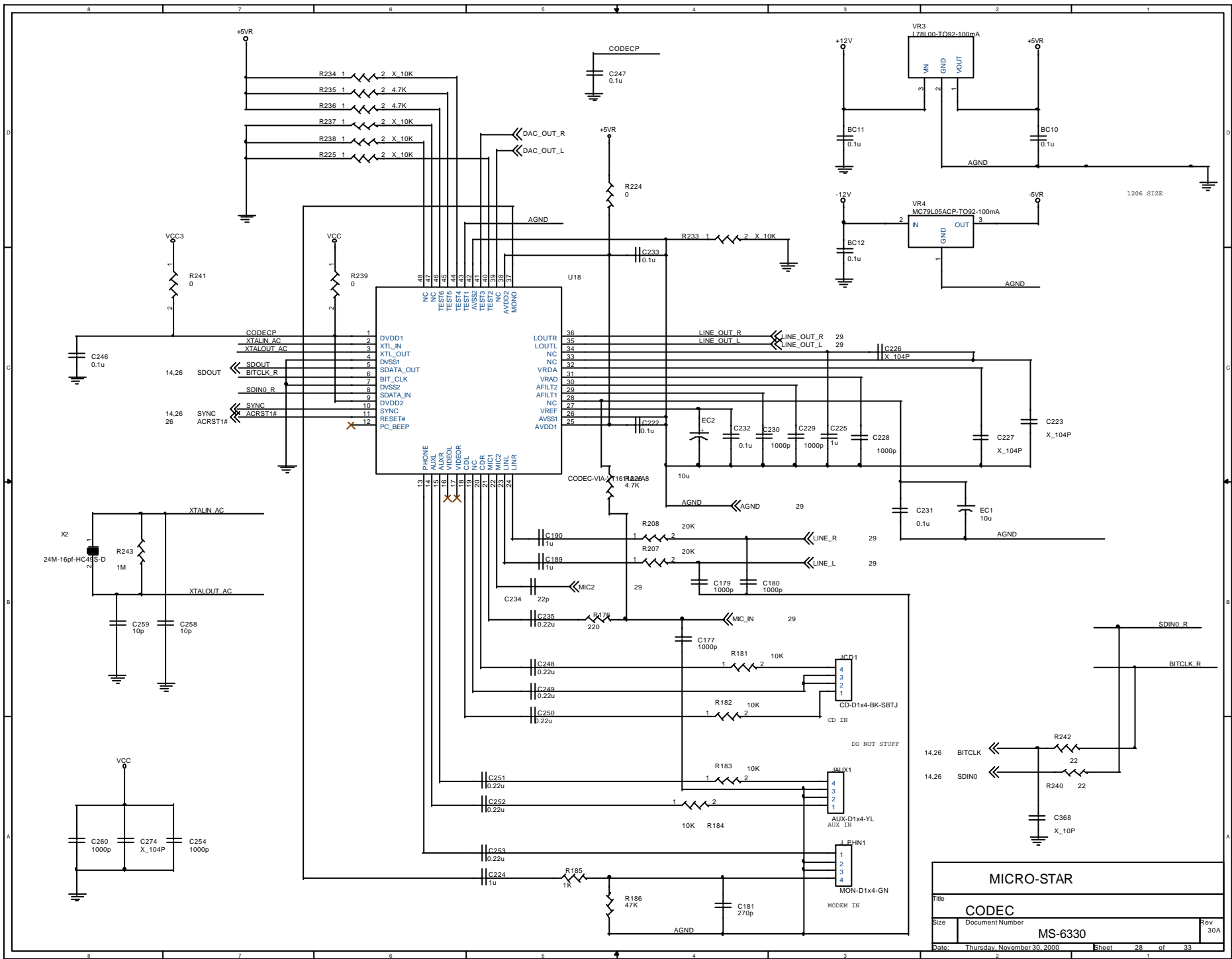
CNR RISER



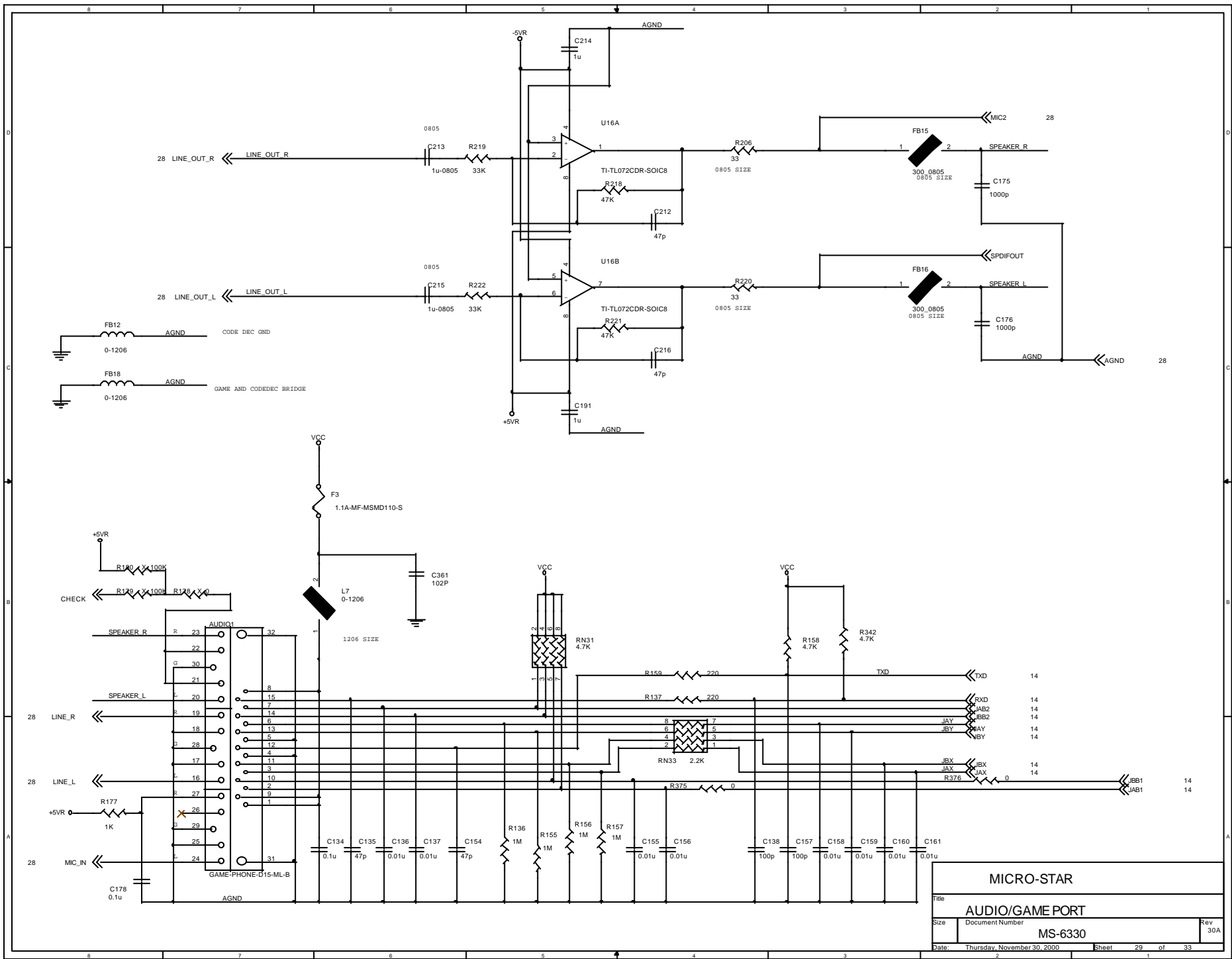
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CNR		
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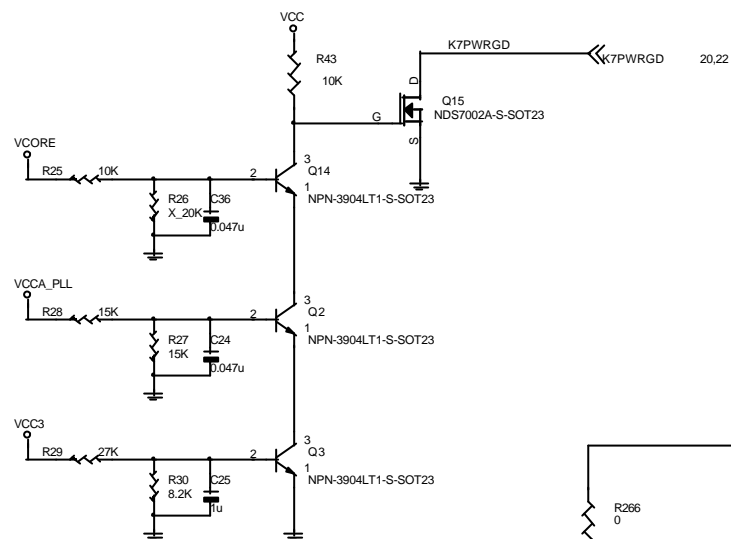
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PCI MASTER PAL DEVICE			
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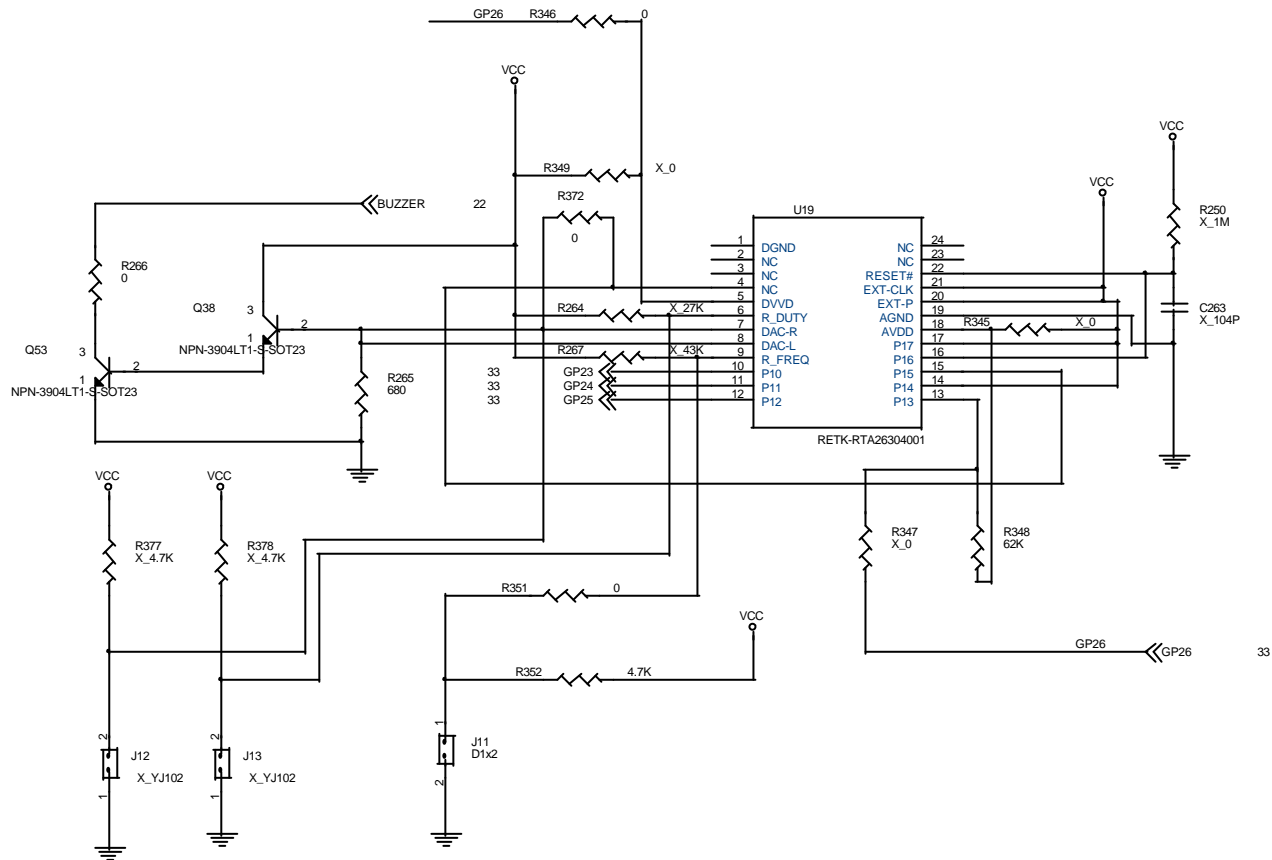
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AUDIO/GAME PORT		
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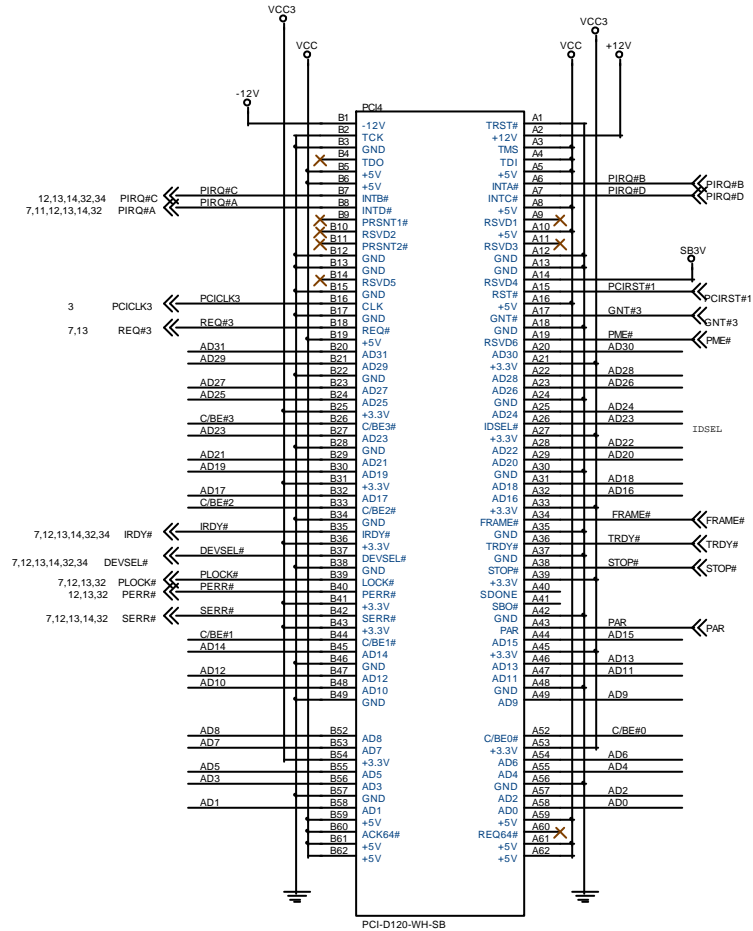
RTA 26301 USE R346,R348
HS 21300 USE R345 ,R347,R349



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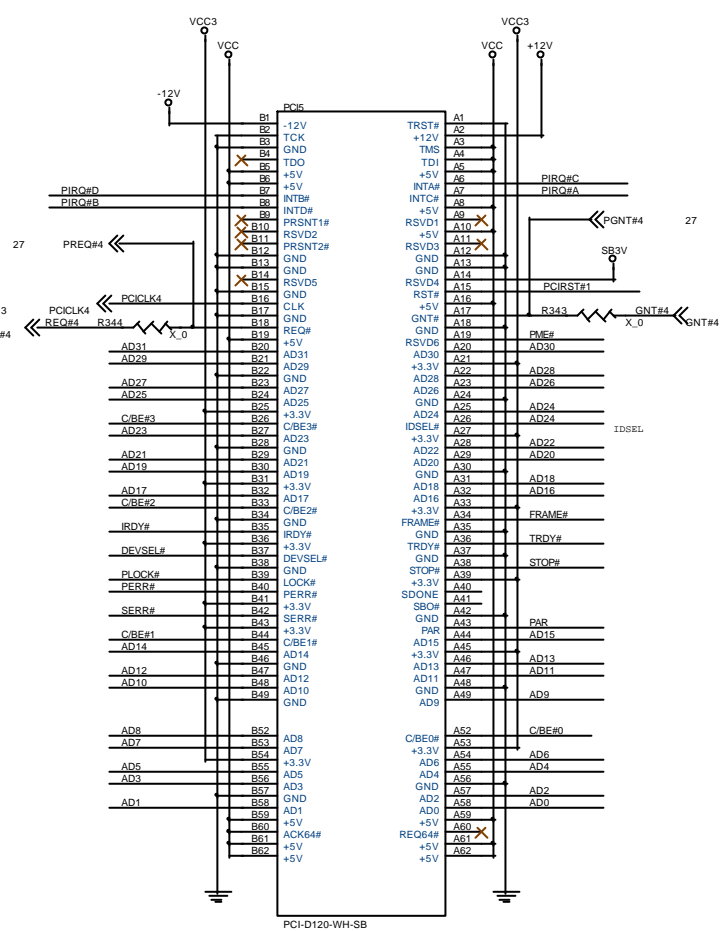
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POWER GOOD & HS21300		
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7,12,13,14,32,34 AD[0:31] << AD[0:31]
7,12,13,14,32,34 C/BE#[0:3] << C/BE#[0:3]



PCI-D120-WH-SB

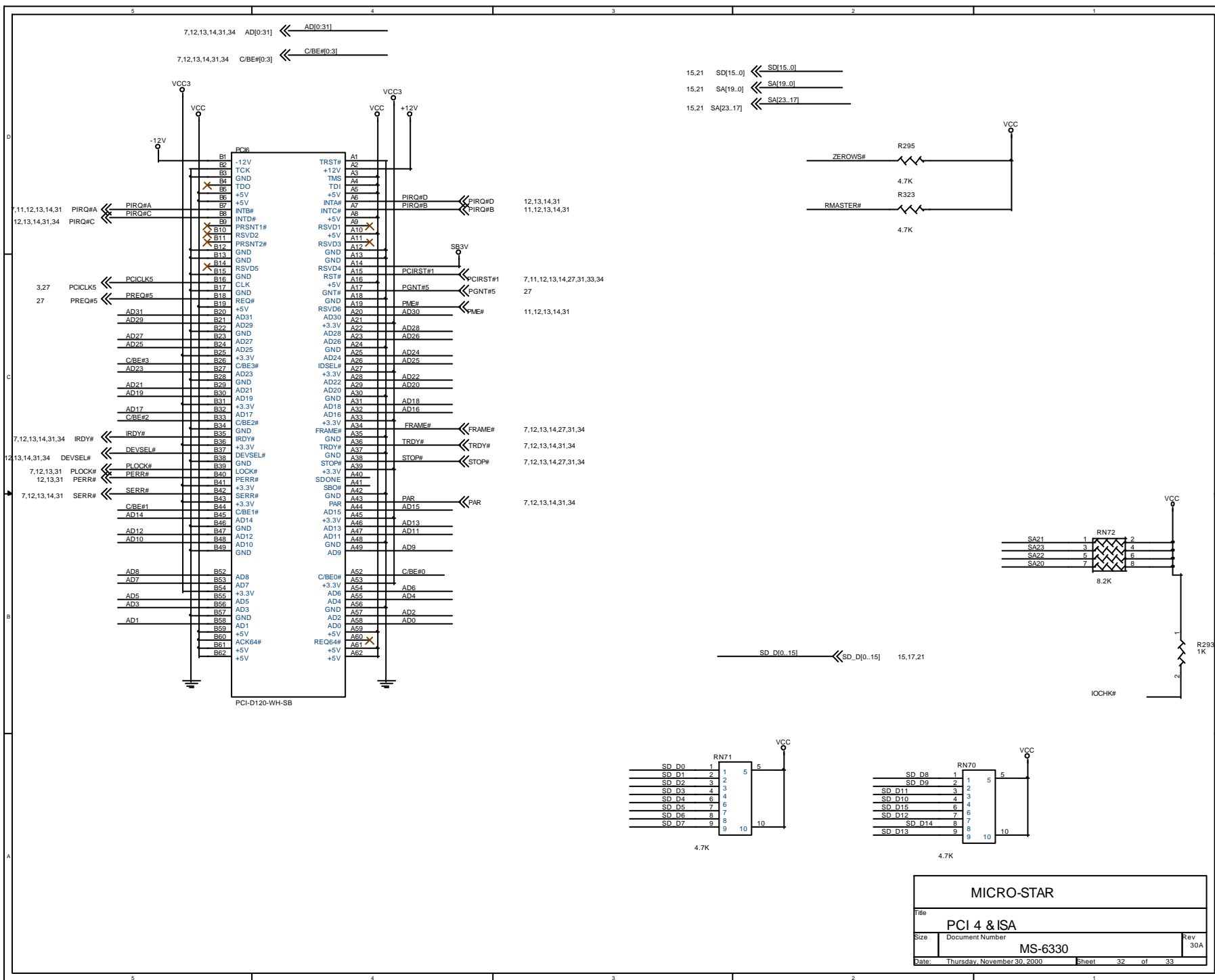
11,12,13,14,32
12,13,14,32
7,11,12,13,14,27,32,33,34
7,13
11,12,13,14,32 7,13,27
REQ#4

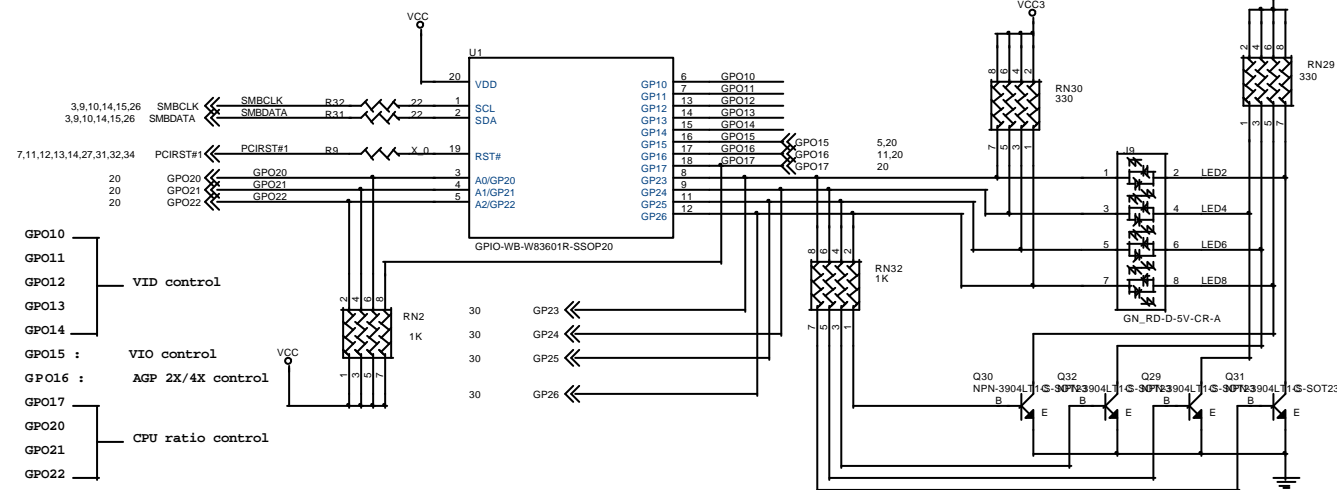
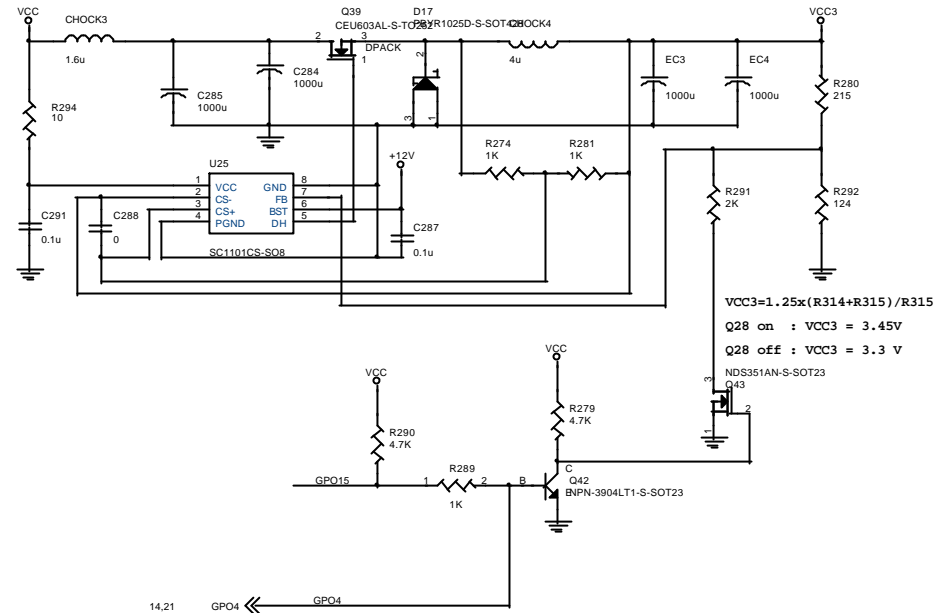
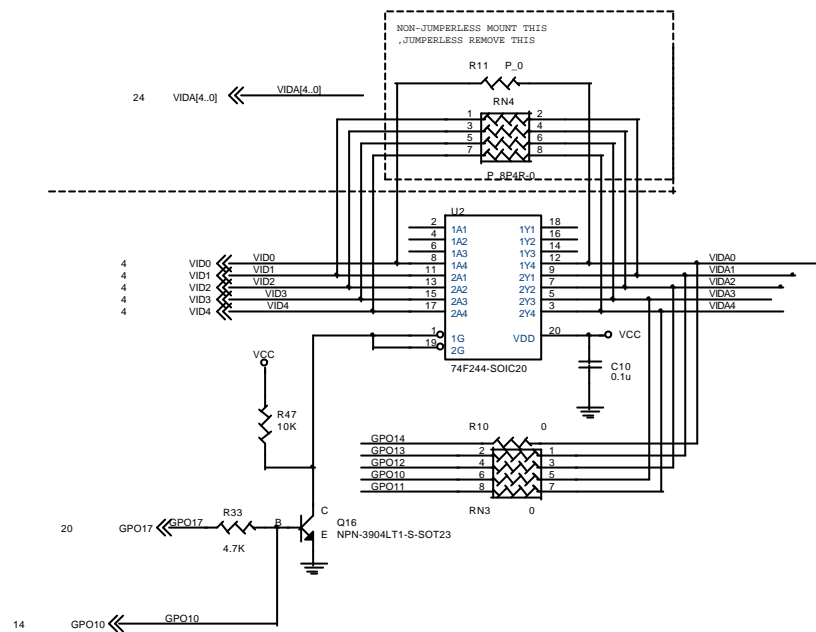


PCI-D120-WH-SB

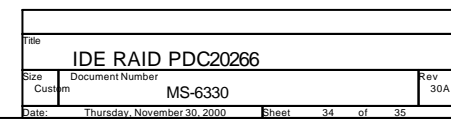
MICRO-STAR

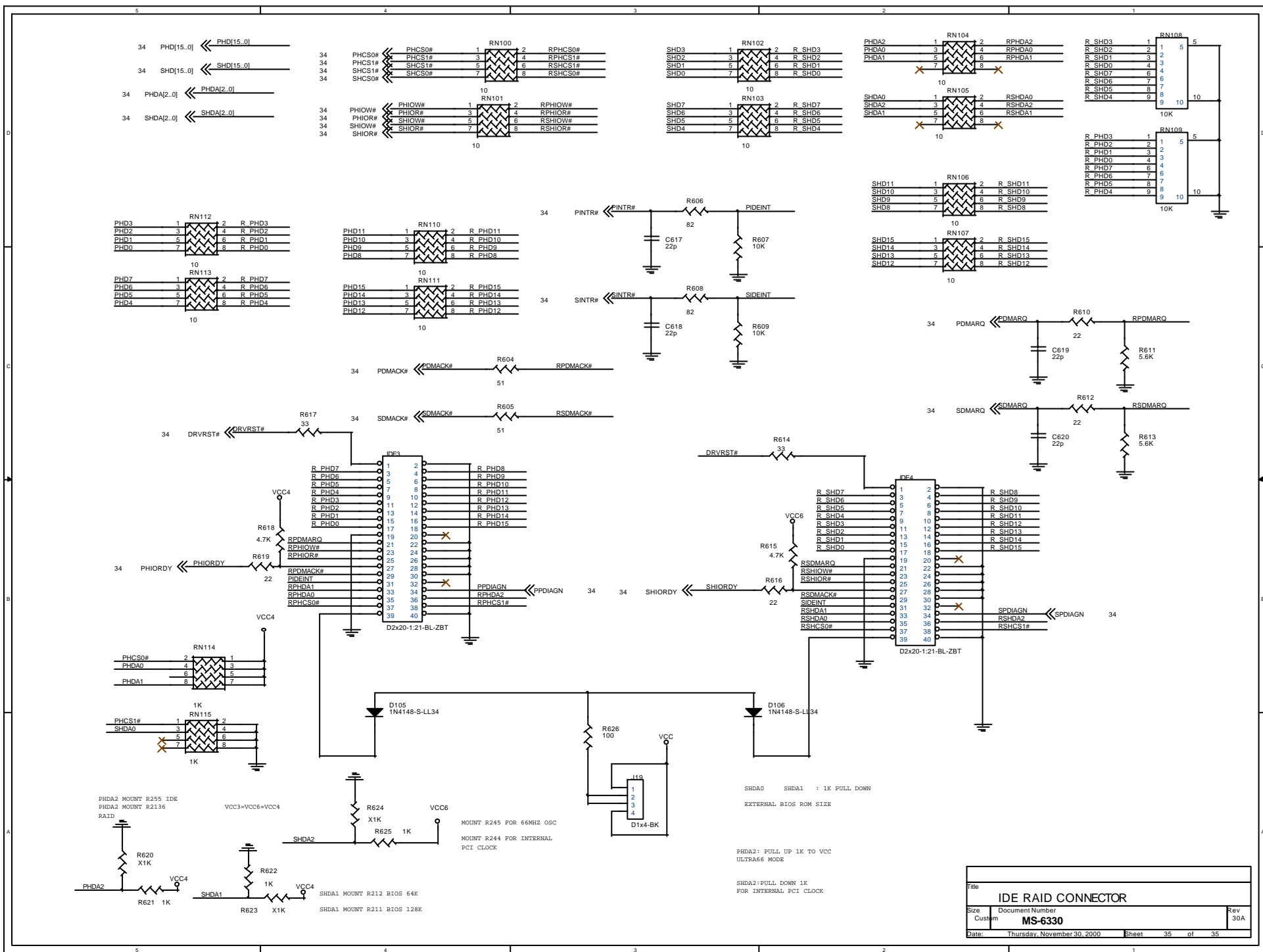
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PCI 4 & 5		
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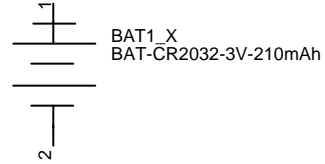
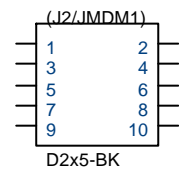
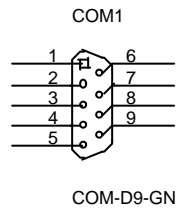
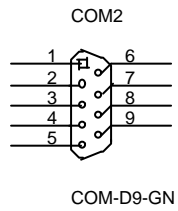
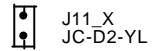
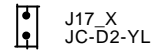
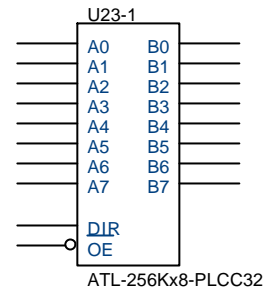
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- 1.R371,Q51,Q52,U28,R369,RN77,Q50 FOR CPU RATIO FUNCTION (1B1)
- 2.WINBOND 83601 GPO17/GPO15 CHANGE FUNCTION FOR CPU RATIO CONTROL PIN AND RESET PIN (1B1)
- 3.WINBOND 83601 GPO16/GPO20/GPO21/GPO22 ARE CPU FUNCTION TABLE PIN (1B1)
- 4.RN78 ADD U27 PIN 6/7/8 PULL HIGH RESISTOR (1B1)
- 5.J14 FOR CNR CODEC AND MB CODEC PRIMARY/SECONDARY SETTING (10C)
- 6.J11/J12/J13 FOR 8 LANGUAGE SUPPORT (10C)
- 7.R253 PULL HI VCC3 CHANGE TO PULL HI +12V FOR GERMAN CPU HEADSINK (10C)

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