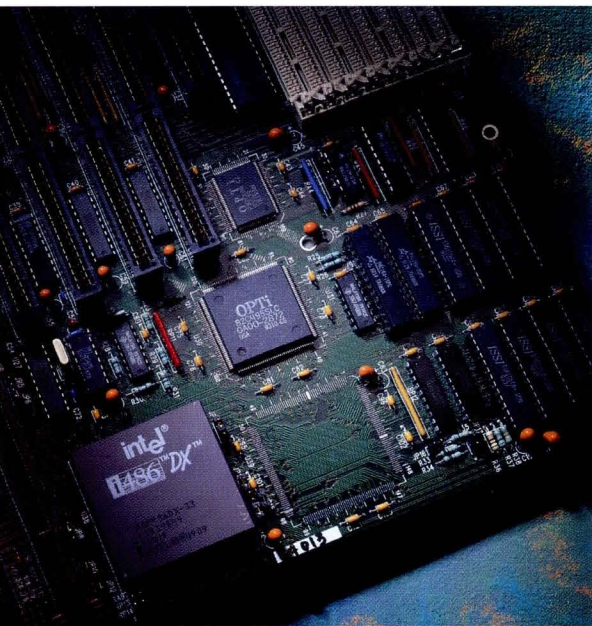
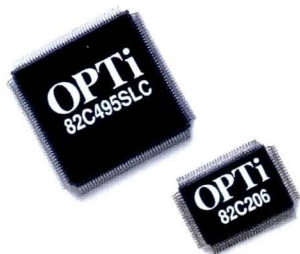


A.T.



.....386/486 Low Cost Write Back.....

The OPTi DXSLC was designed with two major objectives in mind. First, support the high volume, high performance 386/486

VL market. Second, be the most cost-efficient solution, even, in this extremely competitive market. The DXSLC redefines chipset solutions for that "value" market in a single broad-stroke.

The DXSLC vehicle provides all the above values—but still in, the OPTi tradition of reliability, compatibility, support and service throughout the design and after sales.

The DXSLC is designed to be the best combination of cost-effective packaging and partitioning, while keeping the feature set robust.

The DXSLC is the "only" solution if you want to have a competitive solution in today's and tomorrow's markets.

Features/Benefits

- One 160-pin CMOS Plastic Flat Package (PFP) plus 82C206
- Internal buffers and termination to reduce external parts count
- Copy-back Direct-Mapped Cache with size of 64Kb, 128Kb, 256Kb and 512Kb
- Up to 10% performance enhancement from write-through cache scheme
- Supports 2,1,1,1 or 3,2,2,2 cache cycles
- On-chip comparator determines cache hit or miss
- Up to 64-MB of local high-speed, page-mode, DRAM memory space
- Burst-line-fill during Cache-Read-Miss
- Control of two non-cacheable regions
- Shadow RAM support for System BIOS, Video Bios and adapter card BIOS
- Optional caching of shadowed Video BIOS
- Hidden refresh support to enhance system performance
- 8042 emulation for fast CPU-reset and gateA20 generation
- Turbo/slow speed selection
- AT-bus clock selectable from CLKI (/6,/5,/4,/3)
- CAS before RAS refresh reduces power consumption
- Optional 0 or 1 wait state for Cache-Write-Hit
- 387 Coprocessor support for 386 mode
- Internal CD and CA bus pull-up resistors to save components and board real-estate
- Comprehensive VESA VL and OPTi High Performance Local Bus support
- Low cost, low power, 1.0 μ CMOS Technology



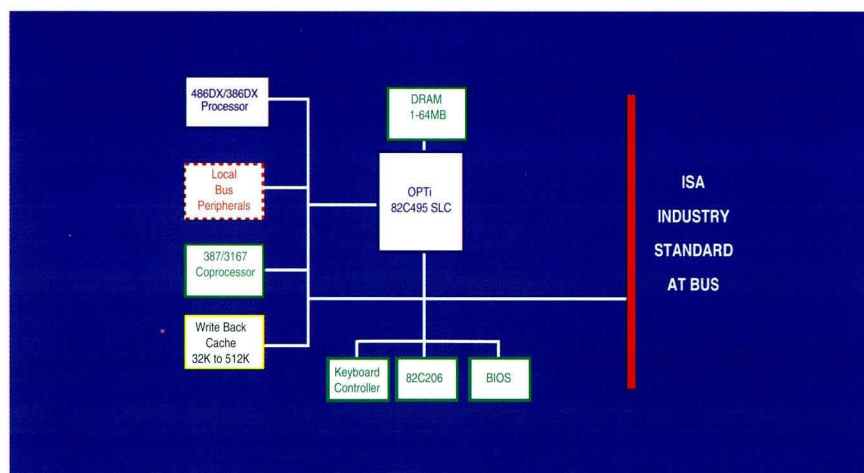
The OPTi logo, featuring the word 'OPTi' in a white serif font on a blue square background with a grid pattern.

The OPTi 495SLC is a "Super Low Cost", two chip solution offering optimal performance for low to mid-range 386/486 based AT systems. The OPTi 495SLC is designed for 386 systems running from 20, 25, 33 and 50 MHz. The 82C495SLC integrates

a write-back cache controller, a local DRAM controller, the CPU state machine, the AT bus state machine and data buffers, all in a single 160-pin PFP. New on-chip hardware provides the hooks for OPTi and VESA local bus device support.

Vital Statistics	486 DXSLC
Frequency	25/33/40/50
VLSI+TTL	2+16
Pals	0
Write-back Cache	64k-512k
DRAM capacity	64M
Video/system BIOS shadow/cache	Yes
Synchronous AT bus clock	8.33/8.25/8.0
Local Bus device support	Yes
Landmark v2.0 (MHz) @ 66MHz	223.04
Power Meter v1.3 (MIPS) @ 66MHz	29.304
Norton SI v6.0 (CI) @ 66 MHz	144.2

**OPTi
DXSLC:
The super
low-cost
leader.**



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