Section 13: Electrical Data

13.1 MAXIMUM RATINGS

Table 13-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to VSS	-0.5V to VDD+0.5V

13.2 DC SPECIFICATIONS

Table 13-2. DC Specifications (VDD = 5V ± 5%)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		0.8	V
V_{IH}	Input High Voltage	2.0		V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	V_{DD} - 0.4		V
I_{OL1}	Output Low Current	2 (Note 1)		mA
I_{OH1}	Output High Current	-1		mA
I_{OL2}	Output Low Current	4 (Note 2)		mA
I_{OH2}	Output High Current	-2		mA
I_{OL3}	Output Low Current	8 (Note 3)		mA
I_{OH3}	Output High Current	-4		mA
I_{OL4}	Output Low Current	16 (Note 4)		mA
I_{OH4}	Output High Current	-8		mA
I_{OL5}	Output Low Current	24 (Note 5)		mA
I_{OH5}	Output High Current	-12		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current	TBD		mA

Notes for Table 13-2

1. I_{OL1}, I_{OH1} for 86C801 pins $\overline{DACRD}$, $\overline{DACWR}$, MA[8:0], MB[8:0], $\overline{ROMCS}$, STWR
2. I_{OL2}, I_{OH2} for 86C801 pins $\overline{BLANK}$, $\overline{CAS[3:0]}$, DBENL, $\overline{DBENH}$, DBDIR, HC[1:0], HSYNC, IRQ, PA[7:0], PD[31:0], SD[15:0], SENS, VSYNC

   I_{OL2}, I_{OH2} for 86C805 pins $\overline{BLANK}$, $\overline{CAS[3:0]}$, $\overline{DACRD}$, $\overline{DACWR}$, $\overline{DBENL}$, HC[1:0], HSYNC, SENS, $\overline{STRD}$, PA[7:0], PD[31:0], $\overline{ROMCS}$, $\overline{ENEID}$, SD[15:0], $\overline{SINTR}$, STWR, VSYNC.
3. I_{OL3}, I_{OH3} for 86C801 pins $\overline{RAS[1:0]}$, VCLK, VGAEN, $\overline{WE[1:0]}$

   I_{OL3}, I_{OH3} for 86C805 pins DBDIR, $\overline{DBENH}$, $\overline{RAS[1:0]}$, SD[28:16], SD31, $\overline{WE[1:0]}$.
4. I_{OL4}, I_{OH4} for 86C801 and 86C805 pin $\overline{OE}$.
5. I_{OL5}, I_{OH5} for 86C801 pins IOCHRDY, $\overline{NOWS}$, SD[30:29]

   I_{OL5}, I_{OH5} for 86C805 pins $\overline{LOCA}$, SD[30:29], $\overline{SRDY}$

13.3 AC SPECIFICATIONS

Note: All timing units are in nanoseconds unless otherwise stated.

Table 13-3. Test Loads for AC Timing

86C801	
Pin Name	**Capacitive Load**
$\overline{MEMCS16}$, $\overline{IOCS16}$, $\overline{NOWS}$, IOCHRDY	240pf
$\overline{VGAEN}$, IRQ	120pf
$\overline{RAS[1:0]}$, $\overline{OE}$, $\overline{WE[1:0]}$	80pf
DBDIR, MA[8:0], MB[8:0]	60pf
SD[15:0], $\overline{DBENH}$, $\overline{ROMCS}$, HC[0:1], SENS, $\overline{DACRD}$, $\overline{DACWR}$, STWR	50pf
PA[3:0], $\overline{CAS[3:0]}$	40pf
$\overline{DBENL}$, $\overline{BLANK}$, VSYNC, HSYNC, PA[7:4], VCLK, PD[31:0]	30pf
86C805	
Pin Name	**Capacitive Load**
SD[30:29], $\overline{SRDY}$, $\overline{LOCA}$	240pf
SD[31:16], $\overline{LOCA}$, $\overline{SINTR}$	120pf
$\overline{RAS[1:0]}$, $\overline{OE}$, $\overline{WE[1:0]}$	80pf
DBDIR, MA[8:0], MB[8:0]	60pf
SD[15:0], $\overline{DBENH}$, $\overline{ENEID}$, $\overline{ROMCS}$, HC[1:0], SENS, $\overline{DACRD}$, $\overline{DACWR}$, STWR	50pf
PA[3:0], $\overline{CAS[3:0]}$	40pf
$\overline{DBENL}$, $\overline{BLANK}$, VSYNC, HSYNC, PA[7:4], VCLK, PD[31:0]	30pf

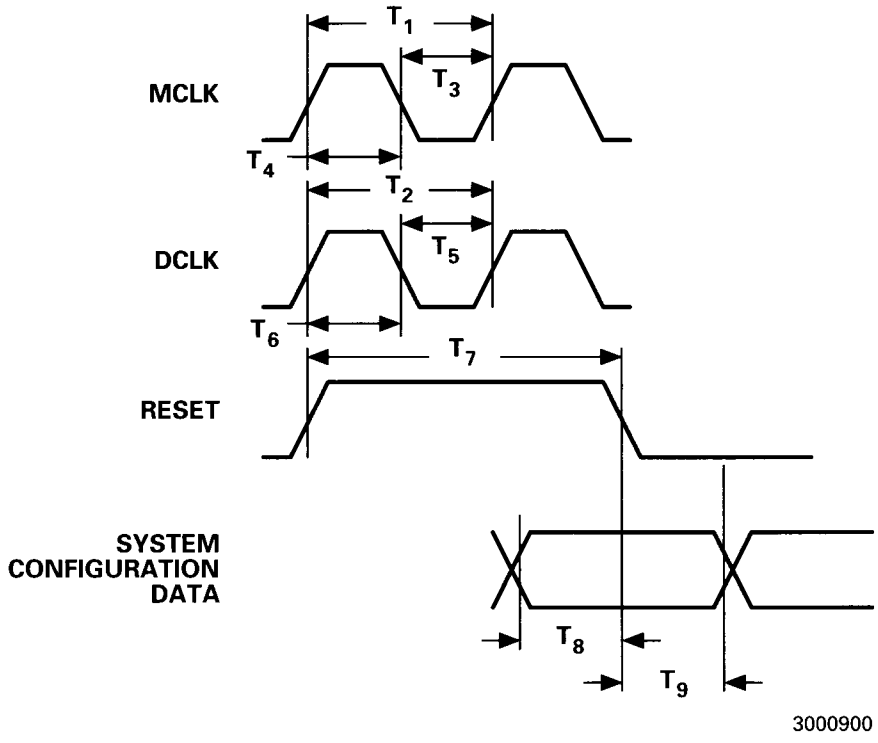

Figure 13-1. Clock And Reset Cycles

Table 13-4. Clock and Reset Timing

Symbol	Parameter	Min	Max
T_1	MCLK Period	20	
T_2	DCLK Period	9	
T_3	MCLK Low Time	8	
T_4	MCLK High Time	8	
T_5	DCLK Low Time	3	
T_6	DCLK High Time	3	
T_7	Reset High Time	400	
T_8	System Configuration Data Setup Time	20	
T_9	System Configuration Data Hold Time	10	

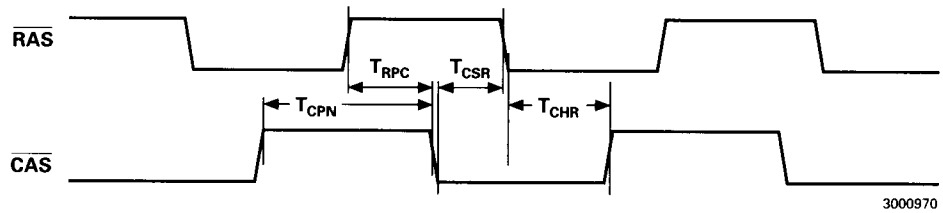

Figure 13-2. CAS Before RAS Refresh Cycle

Table 13-5. CAS Before RAS Refresh Cycle Timing

Sym.	Parameter	T-Value		MCLK 45MHz		MCLK 50MHz	
		Min	Max	Min	Max	Min	Max
TCPN	$\overline{CAS}$ Precharge Time	1		22		20	
TRPC	$\overline{RAS}$ High to $\overline{CAS}$ Low Precharge Time	1		22		20	
TCSR	$\overline{CAS}$ Before $\overline{RAS}$ Setup Time	1.5		33		30	
TCHR	$\overline{CAS}$ Before $\overline{RAS}$ Hold Time	3.5		77		70	

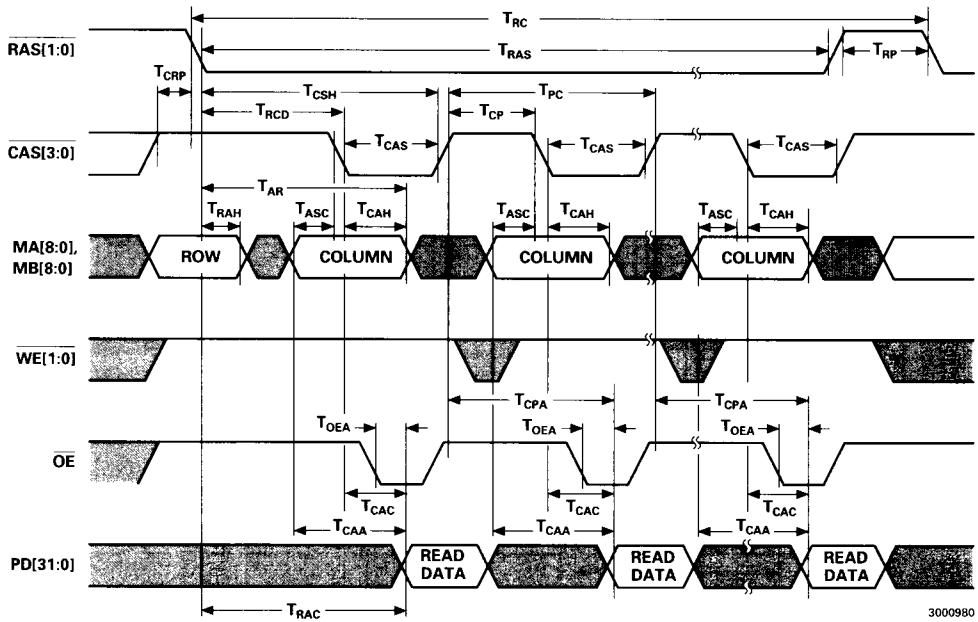

Figure 13-3. Video Memory Fast Page Mode Read Cycle

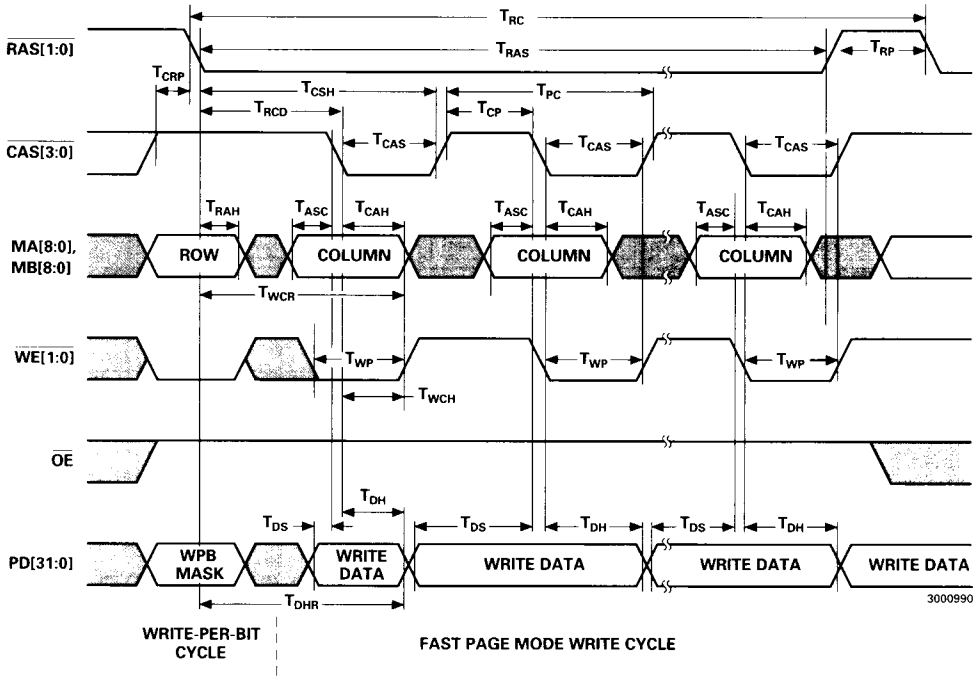

Figure 13-4. Video Memory Fast Page Mode Write Cycle

Table 13-6. Video Memory Fast Page Mode Read/Write Cycle Timing

Guaranteed Timings							
		T-Value		MCLK 45MHz		MCLK 50MHz	
Sym.	Parameter	Min	Max	Min	Max	Min	Max
TCAS	CAS Pulse Width	1		22		20	
TCRP	CAS to RAS Precharge Time	1.5		33		30	
TCSH	CAS Hold Time	3.5		77		70	
TPC	CAS Cycle Time	2		45		40	
TCP	CAS Precharge Time	1		22		20	
TRP	RAS Precharge Time	2.5		55		50	
TRC	RAS Cycle Time	6		133		120	
TRAS	RAS Pulse Width	3.5		77		70	
TRCD	RAS to CAS Delay Time	2.5		55		50	
TRAH	Row Address Hold Time	1.5		33		30	
TAR	Column Address Hold From RAS	3.5		77		70	
TASC	Column Address Setup Time	1		22		20	
TCAH	Column Address Hold Time	1		22		20	
TWCH	Write Command Hold Time	1		22		20	
TWCR	Write Command Hold Referenced to RAS	3.5		77		70	
TWP	Write Command Pulse Width	1		22		20	
TDS	Data-in Setup Time	1		0		0	
TDH	Data-in Hold Time	1		22		20	
TDHR	Data Hold Referenced to RAS	3.5		77		70	
Required Timings							
		T-Value		MCLK 45MHz		MCLK 50MHz	
Sym.	Parameter	Min	Max	Min	Max	Min	Max
TCPA	Data Access Time from CAS Precharge		2		44		40
TRAC	Data Access Time From RAS		3.5		77		70
TCAC	Data Access Time from CAS		1		22		20
TOEA	Data Access Time From OE		1		22		20
TCAA	Data Access Time From Column Address		2		44		40

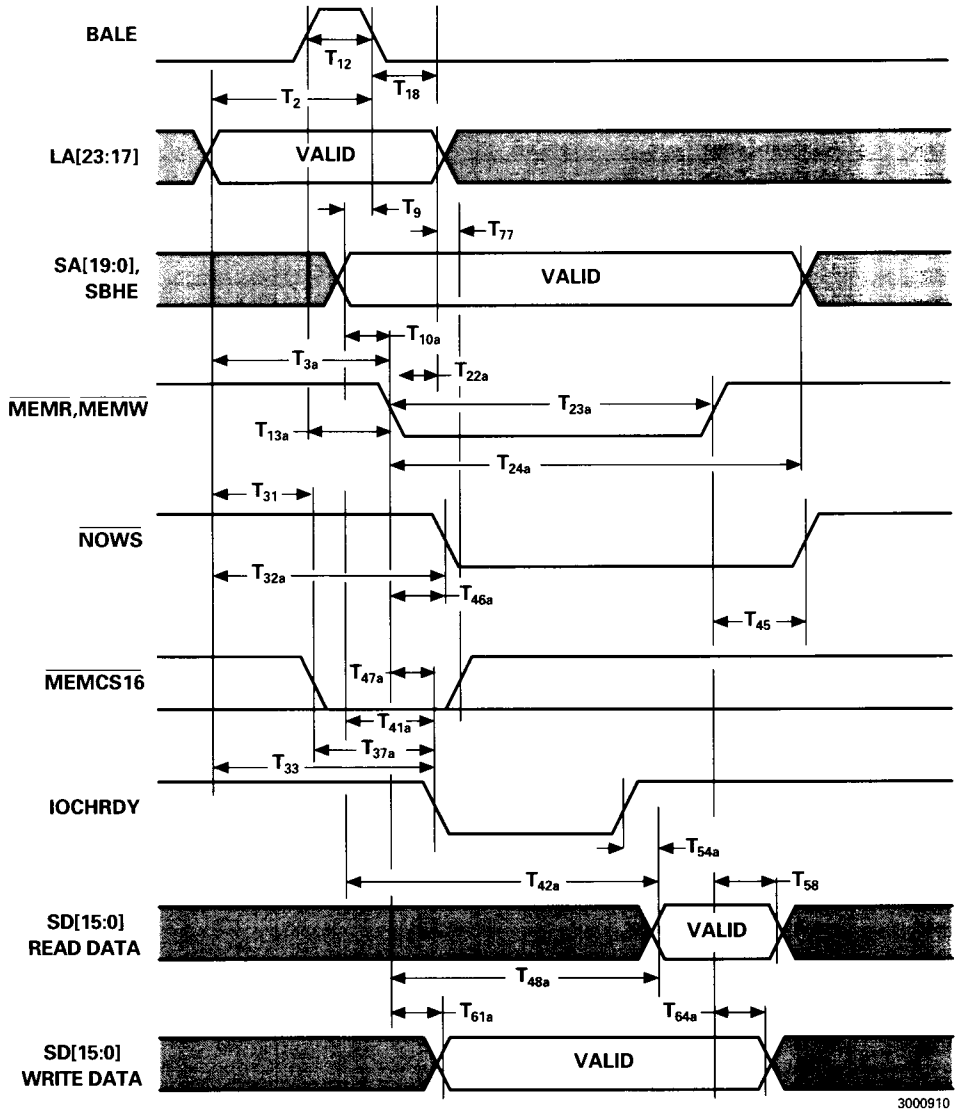

Figure 13-5. ISA Memory Read/Write Cycles

Table 13-7. ISA Memory Read/Write Cycles Timing

Symbol	Parameter	Req/ Guar	Min	Max	Notes
T_2	LA Valid before BALE Low	Req	77		Req = required for input
T_{3a}	LA Valid before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	79		
T_9	SA, $\overline{SBHE}$ Valid Before BALE Low	Req	19		
T_{10a}	SA, $\overline{SBHE}$ Valid Before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	21		
T_{12}	BALE High	Req	25		
T_{13a}	BALE High Before $\overline{MEMR}$, $\overline{MEMW}$ Low	Req	27		
T_{18}	BALE Low Before LA Invalid	Req	32		
T_{22a}	$\overline{MEMR}$, $\overline{MEMW}$ Low Before LA Invalid	Req	30		
T_{23a}	$\overline{MEMR}$, $\overline{MEMW}$ Low	Req	86		For 3 BCLK cycle, T_{23b} >150
T_{24a}	$\overline{MEMR}$, $\overline{MEMW}$ Low Before SA, $\overline{SBHE}$ valid	Req	99		For 3 BCLK cycle, T_{24b} >158
T_{31}	LA Valid to $\overline{MEMCS16}$ Low	Guar		22	Guar = guaranteed output
T_{32a}	LA Valid to $\overline{NOWS}$ Low	Guar	95		
T_{33}	LA Valid to IOCHRDY Low	Guar		99	
T_{37a}	BALE High to IOCHRDY Low	Guar		47	
T_{41a}	SA, $\overline{SBHE}$ Valid to IOCHRDY Low	Guar		40	
T_{42a}	SA, $\overline{SBHE}$ Valid to Read Data Valid	Guar		65	For 3 BCLK cycle, T_{42b} <350
T_{45}	$\overline{MEMR}$, $\overline{MEMW}$ High to $\overline{NOWS}$ Floated	Guar		22	
T_{46a}	$\overline{MEMR}$, $\overline{MEMW}$ Low to $\overline{NOWS}$ Low	Guar		18	
T_{47a}	$\overline{MEMR}$, $\overline{MEMW}$ Low to IOCHRDY Low	Guar		21	
T_{48a}	$\overline{MEMR}$ Low to Read Data Valid	Guar		45	For 3 BCLK cycle, T_{48b} <330
T_{54a}	IOCHRDY High to Read Data Valid	Guar		0	
T_{58}	$\overline{MEMR}$, $\overline{IOR}$ High to Read Data Invalid	Guar	14		
T_{61a}	$\overline{MEMW}$ Low to Write Data Valid	Req		25	
T_{64a}	$\overline{MEMW}$ High to Write Data Invalid	Req	16		
T_{77}	LA Invalid to $\overline{MEMCS16}$ Invalid	Guar	15		

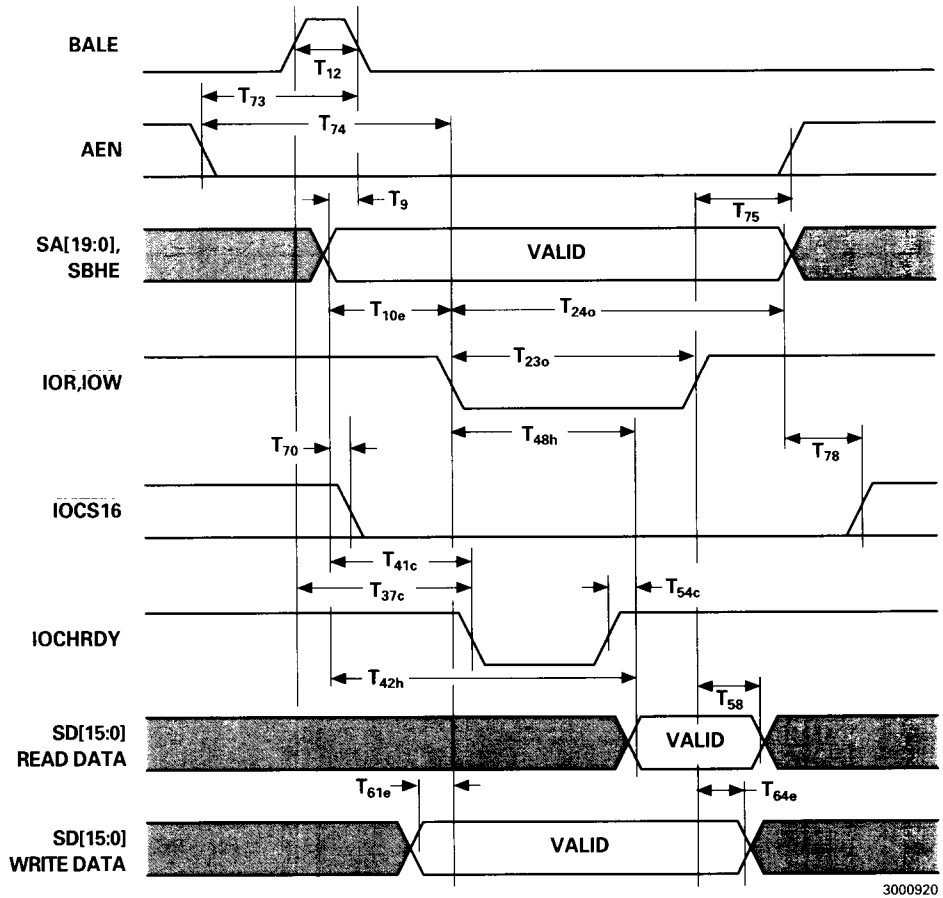

Figure 13-6. ISA I/O Read/Write Cycles

Table 13-8. ISA I/O Read/Write Cycles Timing

Symbol	Parameter	Req Guar	Min	Max	Notes
T_9	SA, $\overline{SBHE}$ Valid Before BALE Low	Req	19		Req = required for input
T_{10e}	SA, $\overline{SBHE}$ Valid before $\overline{IOR}$, $\overline{IOW}$ Low	Req	63		
T_{12}	BALE High	Req	25		
T_{23o}	$\overline{IOR}$, $\overline{IOW}$ Low	Req	106		
T_{24o}	$\overline{IOR}$, $\overline{IOW}$ Low Before SA, $\overline{SBHE}$ Invalid	Req	114		
T_{37c}	BALE High to IOCHRDY Low	Guar		99	Guar = guaranteed output
T_{41c}	SA, $\overline{SBHE}$ Valid to IOCHRDY Low	Guar		94	
T_{42h}	SA, $\overline{SBHE}$ Valid to Read Data Valid	Guar		240	
T_{48h}	$\overline{IOR}$ Low to Read Data Valid	Guar		230	
T_{54c}	IOCHRDY High to Read Data Valid	Guar		205	
T_{58}	$\overline{IOR}$ High to Read Data Invalid	Guar	10		
T_{61e}	$\overline{IOW}$ Low to Write Data Valid	Guar		25	
T_{64e}	$\overline{IOW}$ High to Write Data Invalid	Req	14		
T_{70}	SA, $\overline{SBHE}$ Valid before $\overline{IOCS16}$ Low	Guar		25	
T_{73}	AEN Valid Before BALE Low	Req	75		
T_{74}	AEN Valid Before $\overline{IOR}$, $\overline{IOW}$ Low	Req	122		
T_{75}	$\overline{IOR}$, $\overline{IOW}$ High Before AEN High	Req	8		
T_{78}	SA Invalid to $\overline{IOCS16}$ Invalid	Guar	21		

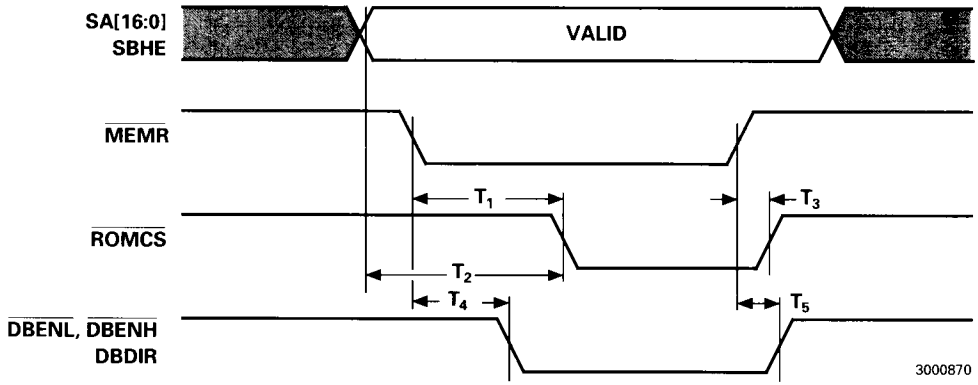

Figure 13-7. ISA BIOS Read Cycle

Table 13-9. ISA BIOS Read Cycle Timing

Symbol	Parameter	Min	Max	Notes
T_1	$\overline{MEMR}$ Low to $\overline{ROMCS}$ Low		36	
T_2	SA[16:0] , $\overline{SBHE}$ Valid to $\overline{ROMCS}$ Low		54	
T_3	$\overline{MEMR}$ High to $\overline{ROMCS}$ High	10		
T_4	$\overline{MEMR}$ Low to Data Buffer Enable Low		25	
T_5	$\overline{MEMR}$ High to Data Buffer Enable High		25	

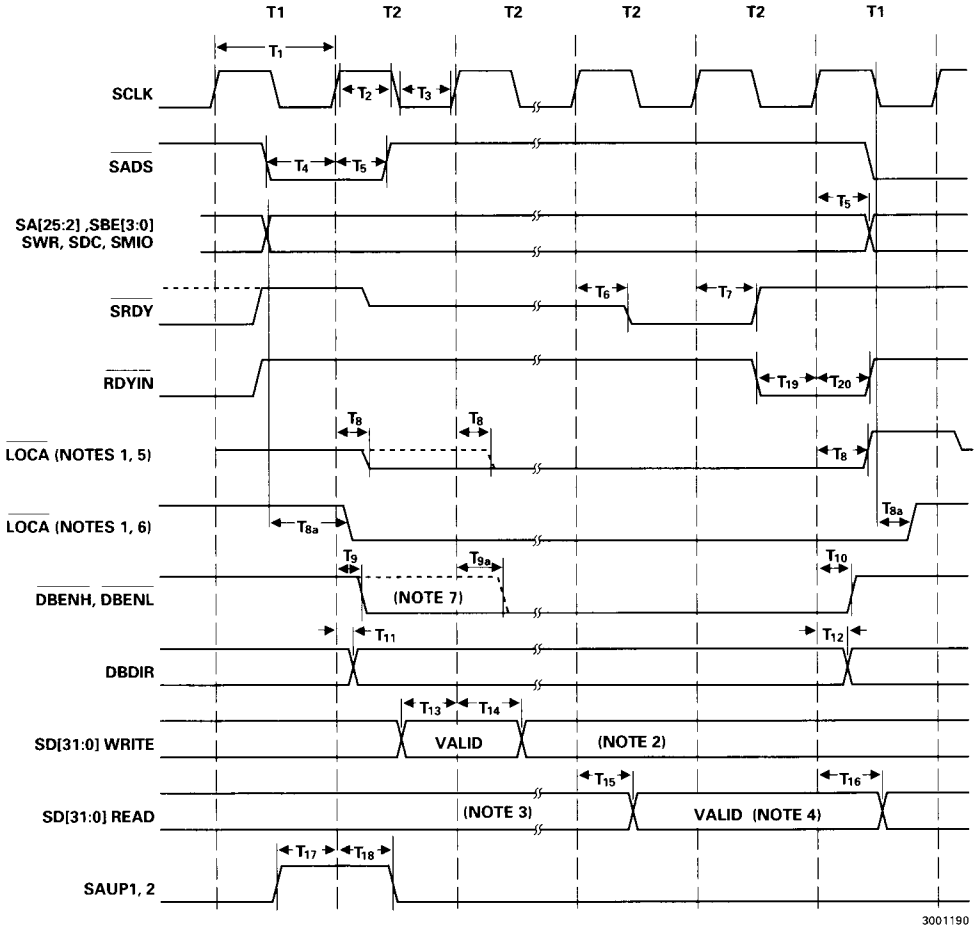

Figure 13-8. Local Bus AC Cycles

Notes for Figure 13-8

1. LOCA will be generated according to one of two waveforms selected through bit 11 of the power-on strapping pins. If bit 11 is strapped high, LOCA is tri-state until driven low at a period determined by the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). It is held low until SRDY is asserted, driven high for one clock, and then tri-stated. If bit 11 is strapped low, LOCA is never tri-stated and is held low as long as SA[19:0] and the control signals are valid.
2. Write data is latched into the 86C805 at the beginning of the first T2 cycle.
3. For 33 MHz operation, the System Configuration register (3?5H, Index 40) must be programmed with one read wait state (bit 2 = 1) and with a "Decode Wait Control" (bits 5-4) value of 01.
4. Read data is valid before the end of the T2 cycle indicated by SRDY until after the last T2 cycle (indicated by RDYIN).
5. The T-state in which LOCA goes active depends on the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). If these bits are programmed to a value of 00, then tri-state LOCA will be active in the first T2 cycle. If these bits are programmed to 01, then tri-state LOCA will be active in the second T2 cycle.
6. Parameter T_{8a} is measured from the latest of: SADS leading edge, SCLK going low, or address/status/SAUP[1:2] active for an 86C805 cycle.
7. The T-state in which DBENL/H goes active during read operations depends on the setting of "Decode Wait Control" (bits 5-4) of the System Configuration register (3?5H, Index 40). If these bits are programmed to a value of 00, then DBENL/H will go active in the first T2 cycle. If these bits are programmed to 01, then DBENL/H will go active in the second T2 cycle.

Table 13-10. Local Bus AC Cycles Timing

Symbol	Parameter	Req Guar	Min	Max	Notes
T_1	SCLK Period	Req	30/20*		Req = required for input
T_2	SCLK High Time	Req	11/7*		Measured at 2.0V
T_3	SCLK Low Time	Req	11/7*		Measured at 0.8V
T_4	SA, $\overline{SBE}$, SWR, SDC, SMIO, $\overline{SADS}$ Setup	Req	8		
T_5	SA, $\overline{SBE}$, SWR, SDC, SMIO, $\overline{SADS}$ Hold	Req	3		
T_6	$\overline{SRDY}$ Delay	Guar		15	Guar = guaranteed output
T_7	$\overline{SRDY}$ Hold	Guar	4		
T_8	$\overline{LOCA}$ Active Delay (Tri-state)	Guar		16	Tri-state $\overline{LOCA}$ selection
T_{8a}	$\overline{LOCA}$ Active Delay (Level)	Guar		20	Level $\overline{LOCA}$ selection
T_9	Data Buffer Enable Delay (Write Cycle)	Guar		15	Write cycle
T_{9a}	Data Buffer Enable Delay (Read Cycle)	Guar		20	Read cycle
T_{10}	Data Buffer Enable Hold	Guar	4	15	
T_{11}	Data Buffer Direction Delay	Guar		15	
T_{12}	Data Buffer Direction Hold	Guar	4		
T_{13}	Write Data Setup	Req	4		
T_{14}	Write Data Hold	Req	0		
T_{15}	Read Data Valid After Beginning of SRDY T-state	Guar		12	
T_{16}	Read Data Hold After end of RDYIN T-state	Guar	5	15	
T_{17}	SAUP1, SAUP2 Setup	Req	5		
T_{18}	SAUP1, SAUP2 Hold	Req	5		
T_{19}	$\overline{RDYIN}$ Setup	Req	7		
T_{20}	$\overline{RDYIN}$ Hold	Req	3		

* 33 MHz/50 MHz CPU clock speed

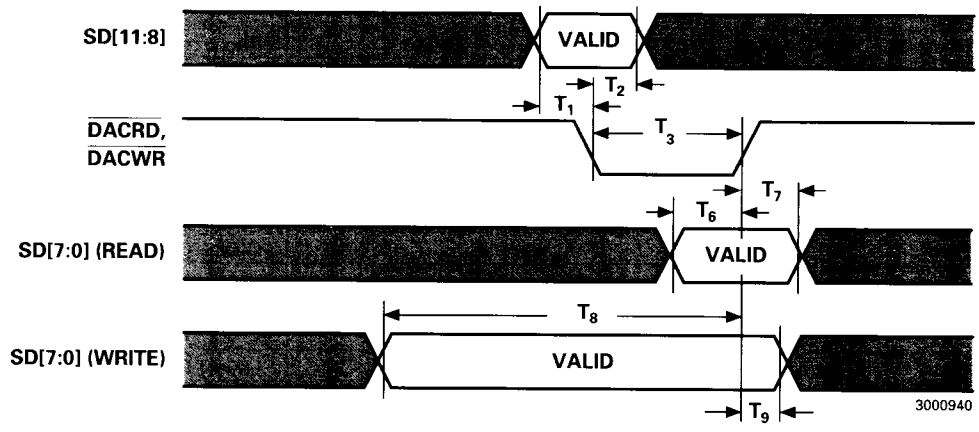

Figure 13-9. Video DAC Read/Write AC Cycles

Table 13-11. Video DAC AC Cycles Timing

Symbol	Parameter	Min	Unit
T_1	SD[10:8] Setup to $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low	2	MCLK
T_2	SD[10:8] Hold from $\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low	2	MCLK
T_3	$\overline{\text{DACRD}}$, $\overline{\text{DACWR}}$ Low Time	4	MCLK
T_6	Read Data Valid Setup to $\overline{\text{DACRD}}$ High	2	MCLK
T_7	Read Data Valid Hold to $\overline{\text{DACRD}}$ High	2	MCLK
T_8	Write Data Valid Setup to $\overline{\text{DACWR}}$ High	2	MCLK
T_9	Write Data Valid Hold to $\overline{\text{DACWR}}$ High	2	MCLK

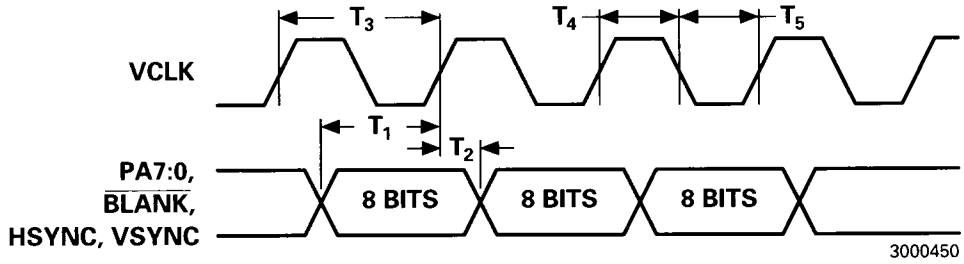

Figure 13-10. Video Timing - 4, 8, 24 Bits/Pixel Modes

Table 13-12. 4, 8 and 24 BPP Video AC Timing

Symbol	Parameter	Min	Max	Notes
T_1	P[7:0], $\overline{\text{BLANK}}$, SYNC Setup Time	3		
T_2	PA[7:0], $\overline{\text{BLANK}}$, SYNC Hold Time	3		
T_3	VCLK Period	13.3		
T_4	VCLK High Time	5		
T_5	VCLK Low Time	5		

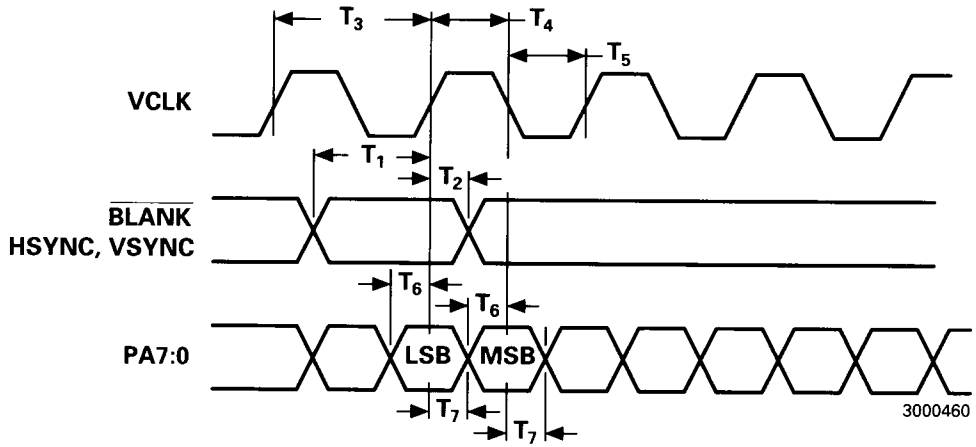

Figure 13-11. Video Timing - 16 Bits/Pixel Mode

Table 13-13. 16 BPP Video AC Timing

Symbol	Parameter	Min	Max	Notes
T_1	BLANK, SYNC Setup Time	3		
T_2	BLANK, SYNC Hold Time	3		
T_3	VCLK Period	20		
T_4	VCLK High Time	8		
T_5	VCLK Low Time	8		
T_6	PA[7:0] Setup Time	1		
T_7	PA[7:0] Hold Time	7		

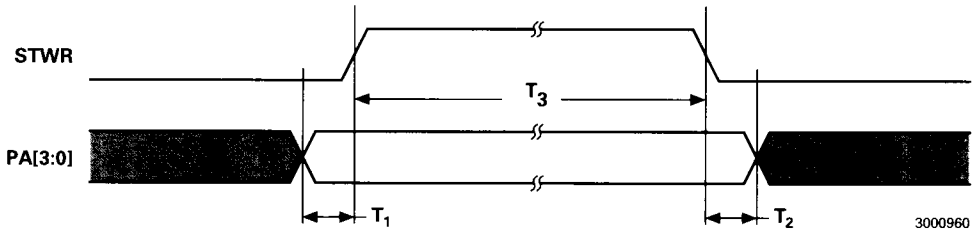

Figure 13-12. Clock Select Cycle

Table 13-14. Clock Select Cycle Timing

Symbol	Parameter	Min	Max	Notes
T_1	Clock Select Lines Set-up Time	10		
T_2	Clock Select Lines Hold Time	10		
T_3	STWR Pulse Width	3 DCLK		For display off; if display is on, the minimum pulse width is 8 DCLKs.