

# Mainboard Layout

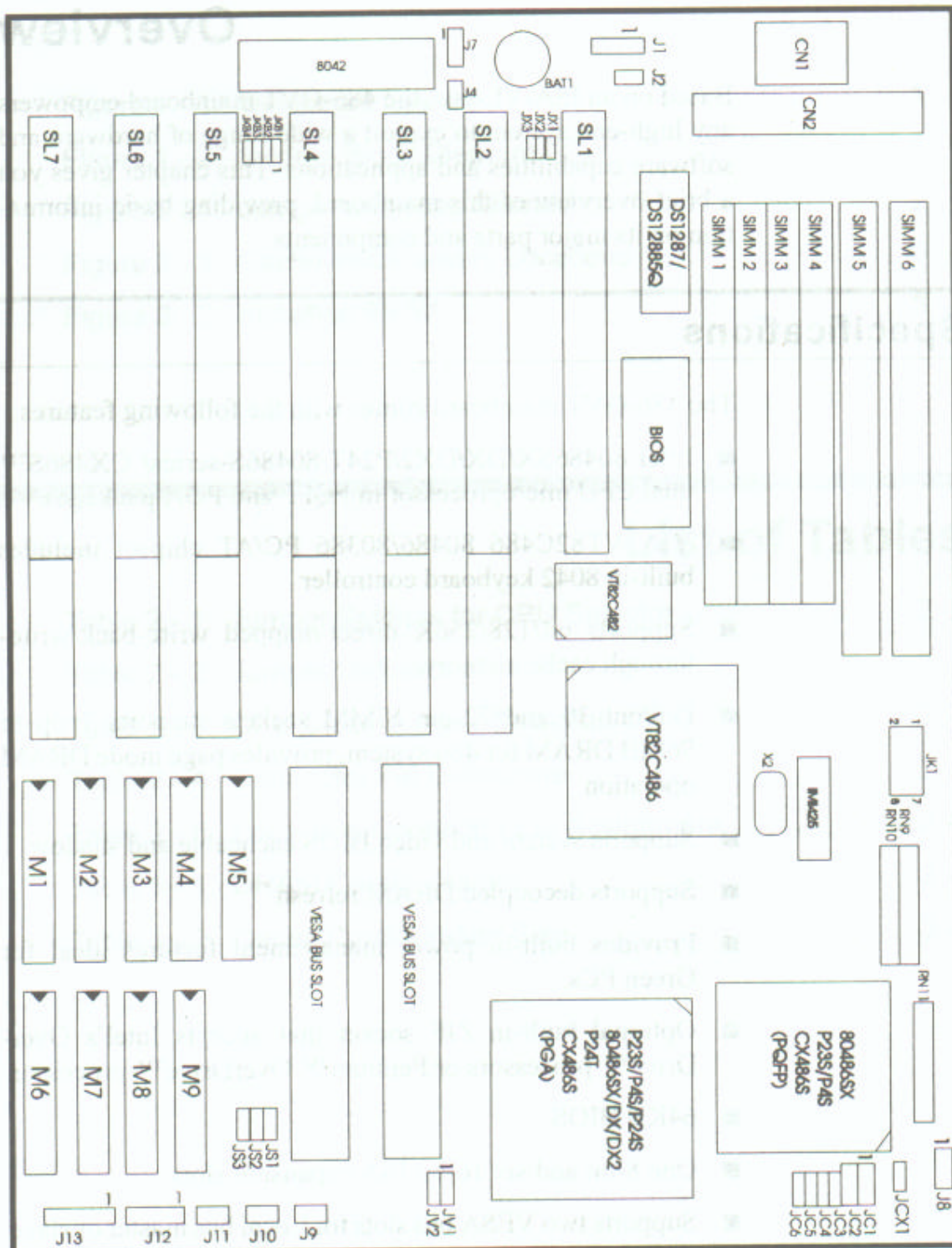


Figure 1-1. Mainboard Layout

# Mainboard Settings

486-GVT has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

## Jumpers

Jumpers are used to select the operation modes for your system. Each jumper on the board has three metal pins with each pin representing a different function. To “set” a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be “shorted” when the black cap has been placed on one or two of its pins, as shown in the figure below:



*Figure 2 - 1 Jumper with Pins Shorted*

## CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GVT provides ten jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next two table summarizes the settings of the CPU Selector jumpers.



JUMPER	486SX/P23S (PGA)	P24S/P4S/ 486DX/DX2 (PGA)	P24T (PGA)	CX486S (M6) (PGA)	CX486DX (M7) CX486S+CX487S (M6+C6) (PGA)
JC1	2-3 short	1-2 short	1-2 short	2-3 short	1-2 short
JC2	2-3 short	1-2 short	1-2 short	2-3 short	1-2 short
JC3	open	short	open	short	short
JC4	open	open	short	open	open
JC5	short	short	open	open	open

JUMPER	P23S/P4S/P24S (PGA)	486DX/DX2/SX (PGA)	CX486S CX486S+CX487S CX486DX (M6, M6+C6, M7) (PGA)	P23S/P4S/ CX486S (PQFP)
RN9 (10p5R 0 ohm)	empty	empty	inserted	empty
RN10 (10p5R 0 ohm)	inserted	empty	empty	empty
RN11 (8p4R 0 ohm)	empty	empty	empty	inserted

Table 2-1. Jumper Settings for CPU Selector



**NOTE :** Users are not encouraged to change the non-specified jumper settings as they are considered factory defaults which may adversely affect system performance.

JUMPER	PIN DEFINITION
J2	External, Internal Battery Select 1-2 External battery 2-3 Internal battery
J4	Display Type Select Open Mono/EGA/VGA (default) Close Color
J7	Password Clear (Award/AMI BIOS Select) 1-2 Award BIOS 2-3 AMI BIOS
JC6	80486SX/P23S/P4S/CX486S PQFP Select Short Disable on-board Open Enable
JCX1	CPU Type Select Short CX486S Open Intel S-series CPU
JKB1, JKB2, JKB3, JKB4, JX3	Internal/External Keyboard Select 1-2 External keyboard 2-3 Internal keyboard
JX1	CPU Clock Select 1-2 1 X 2-3 2 X
JX2, J8	1-2 IRQ15 2-3 -SMI

Table 2-2. Jumper Definitions



**IMISC425 (OSC2) CPU Clock (JK1)**

CLK	1-2	3-4	5-6	7-8
80 MHz	Short	Short	Open	Short
66.6 MHz	Open	Short	Open	Short
	Short	Open	Open	Short
50 MHz	Open	Open	Short	Short
	Open	Short	Open	Open
40 MHz	Short	Open	Short	Short
	Short	Short	Open	Open
33.3 MHz	Short	Open	Open	Open
25 MHz	Open	Open	Short	Open

*Table 2-3. IMISC425 CPU Clock Jumper Selection (JK1)***VIA VT 8225 (OSC2) CPU Clock (JK1)**

CLK	1-2	3-4	5-6	7-8
100 MHz	Open	Short	Open	Short
80 MHz	Open	Open	Short	Short
66.6 MHz	Short	Short	Open	Short
50 MHz	Short	Open	Short	Short
	Open	Short	Open	Open
40 MHz	Open	Open	Short	Open
	Open	Short	Short	Short
33.3 MHz	Short	Short	Open	Open
25 MHz	Short	Open	Short	Open

*Table 2-4. VIA VT 8225 CPU Clock Jumper Selection (JK1)*

## Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. The next table gives the functions of each connector. Some malfunction problems encountered with your system may be caused by loose or improper connection. Ensure that the all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
CN1 Keyboard Connector	1	Keyboard clock
	2	Keyboard data
	3	NC
	4	Ground
	5	+5V
CN2 Power Connector	1	Power good
	2, 10, 11, 12	+5V
	3	+12V
	4	-12V
	5, 6, 7, 8	Ground
J1 External Battery Connector	9	-5V
	1	Anode+
	2, 3	NC
J9 Turbo LED	4	Cathode -
	1	VCC
J10 Turbo Switch	2	LED
	1	Turbo Signal
J11 Hardware Reset	2	Ground
	1	Reset signal
J12 Speaker Connector	2	Speaker signal
	3	NC
	4	Ground
	1	+5V

Table 2-5. Connector Pin Definitions (Continued)



CONNECTOR	PIN OUTS	SIGNAL NAME
J13	1	Power signal
Keylock and Power LED Connector	2	Spare
	3, 5	Ground
	4	Keylock

*Table 2-5. Connector Pin Definitions*

## **VESA Bus Connector**

The cache system board provides two high-performance VESA bus connectors, SL14 and SL15, for use with VESA peripherals. These connectors can be utilized for Local bus (SL14) and (SL15).



**NOTE :** The two VESA Local Bus slot can accommodate either one VESA Master with one VESA Slave or two VESA Slaves.

The following tables give the pin assignments for SL14 and SL15. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV1 and JV2 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN DEFINITION
JV1	CPU Speed Select
	1-2 Greater than 33 MHz
	2-3 Less than or equal to 33 MHz
JV2	High Speed Write
	1-2 One wait write
	2-3 Zero wait write (default)

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
	PIN	OUT	PIN	OUT
SL14 — Local Bus	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV1#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK1
			58	LBS16#

Table 2-6. Local Bus Connector Pin Assignment (Continued)



CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL15 — Local Bus	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV0#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK0
			58	LBS16#

Table 2-6. Local Bus Connector Pin Assignment

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
21MB	256K x 4	4M x 1	16M x 1
	256K x 4	16M x 1	4M x 1
	1M x 4	1M x 1	16M x 1
	1M x 4	16M x 1	1M x 1
	4M x 4	1M x 1	4M x 1
	4M x 4	4M x 1	1M x 1
24MB	1M x 4	4M x 1	16M x 1
	1M x 4	16M x 1	4M x 1
	4M x 4	4M x 1	4M x 1
32MB	4M x 4	16M x 1	
	4M x 4		16M x 1
		16M x 1	16M x 1
33MB	256K x 4	16M x 1	16M x 1
	4M x 4	1M x 1	16M x 1
	4M x 4	16M x 1	1M x 1
36MB	1M x 4	16M x 1	16M x 1
	4M x 4	4M x 1	16M x 1
	4M x 4	16M x 1	4M x 1
48MB	4M x 4	16M x 1	16M x 1
64MB	16M x 4		
65MB	16M x 4	1M x 1	
	16M x 4		1M x 1
66MB	16M x 4	1M x 1	1M x 1
68MB	16M x 4	4M x 1	
	16M x 4		4M x 1
69MB	16M x 4	1M x 1	4M x 1
	16M x 4	4M x 1	1M x 1
72MB	16M x 4	4M x 1	4M x 1
80MB	16M x 4	16M x 1	
	16M x 4		16M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

### Installation Instructions

→ **NOTE :** Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

Assuming the 486-GVT has been mounted on your computer system unit, follow the instructions below:

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 75 degree angle onto the socket.

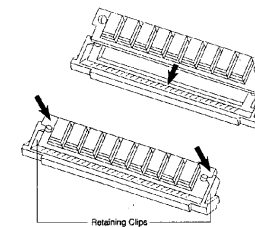


Figure 3-2. Installing SIMMs



## Installing DRAM

### SIMM Banks

486-GVT can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

### DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table.

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256K x 4		
		1M x 1	
2MB			1M x 1
	256K x 4	1M x 1	
		1M x 1	1M x 1
3MB	256K x 4	1M x 1	1M x 1
	1M x 4		
4MB		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table 3-1 DRAM Configurations

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
	4M x 4		
15MB		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
	1M x 4	1M x 1	16M x 1
18MB		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
19MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4	4M x 1	
	4M x 4	4M x 1	
21MB		4M x 1	16M x 1
		16M x 1	4M x 1
		16M x 1	4M x 1

Table 3-1 DRAM Configurations (Continued)

# Memory Subsystem

486-GVT can be equipped with the memory necessary for running all your applications. Memory comes in the form of DRAM (SIMMs) and cache SRAM. This chapter describes these two kinds of memory and gives instructions on how to install each kind on the mainboard.

## Memory Locations

The board layout below shows the locations of the DRAM memory banks and the cache SRAM:

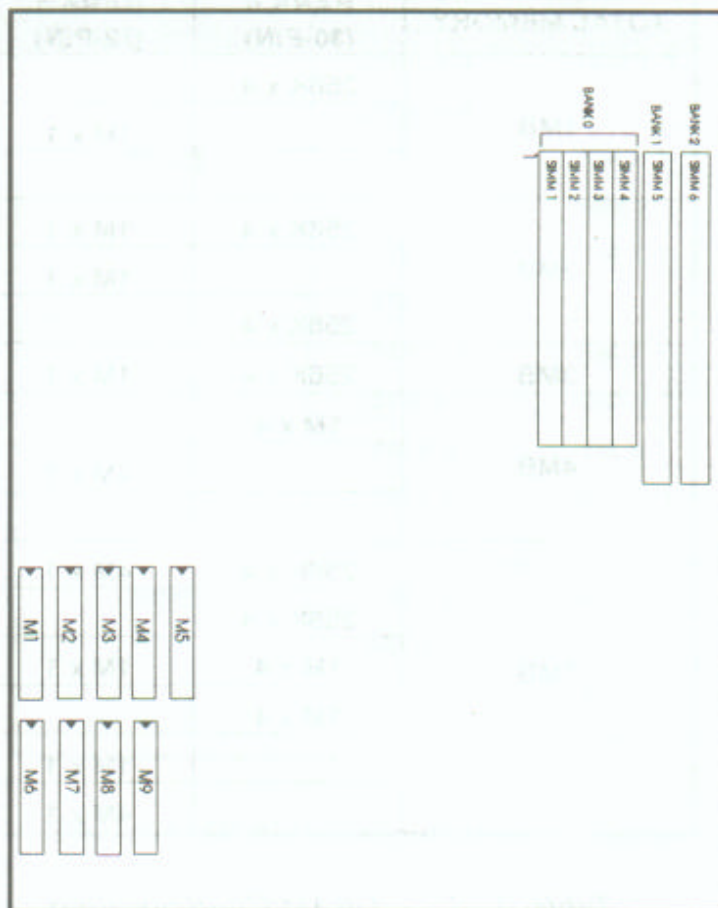


Figure 3-1. Cache and Memory Locations



## Installing DRAM

### SIMM Banks

486-GVT can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, 1MB, 4MB, or 16MB SIMM in each socket.

### DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256K x 4		
		1M x 1	
			1M x 1
2MB	256K x 4	1M x 1	
		1M x 1	1M x 1
	256K x 4		1M x 1
3MB	256K x 4	1M x 1	1M x 1
4MB	1M x 4		
		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table 3 - 1 DRAM Configurations

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
16MB	4M x 4		
		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
		1M x 1	16M x 1
		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
18MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4		16M x 1
	4M x 4	4M x 1	
	4M x 4		4M x 1
		4M x 1	16M x 1
		16M x 1	4M x 1

Table 3-1. DRAM Configurations (Continued)



TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

## Installation Instructions

→ **NOTE :** Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

Assuming the 486-GVT has been mounted on your computer system unit, follow the instructions below:

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 75 degree angle onto the socket.

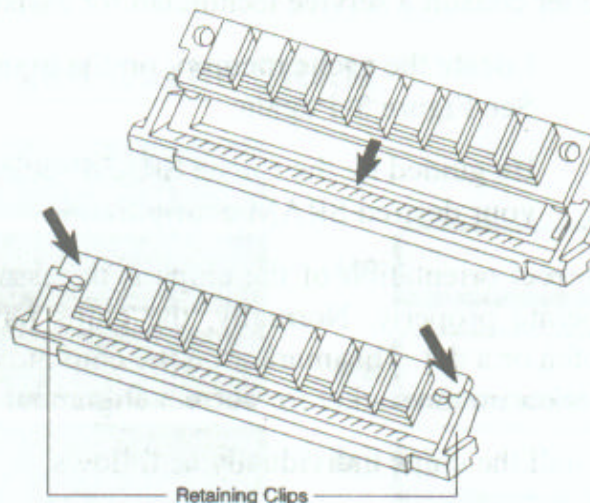


Figure 3-2. Installing SIMMs

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

## Installation Instructions

→ **NOTE :** Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

Assuming the 486-GVT has been mounted on your computer system unit, follow the instructions below:

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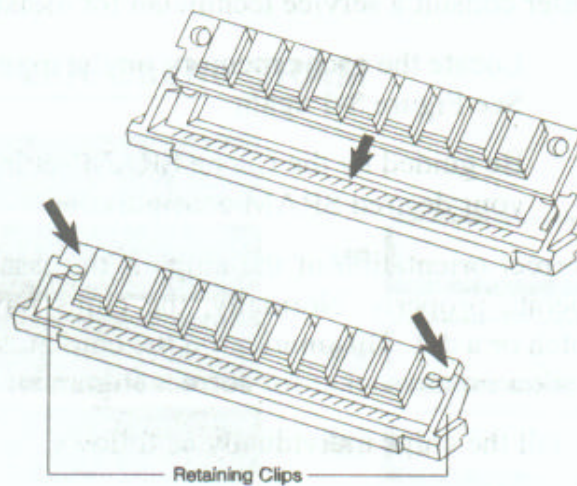


Figure 3-2. Installing SIMMs



3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

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## Cache Memory

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The 486-GVT can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM. Alter RAM type is always the same as Tag RAM.**

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## Installing Cache Memory

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→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard.  
See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration:

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.

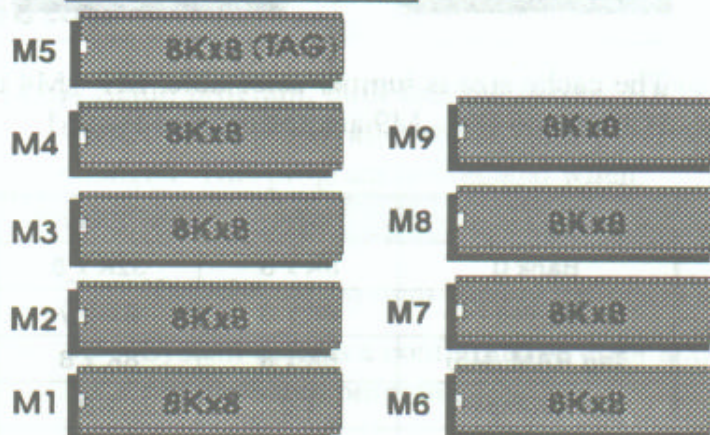
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

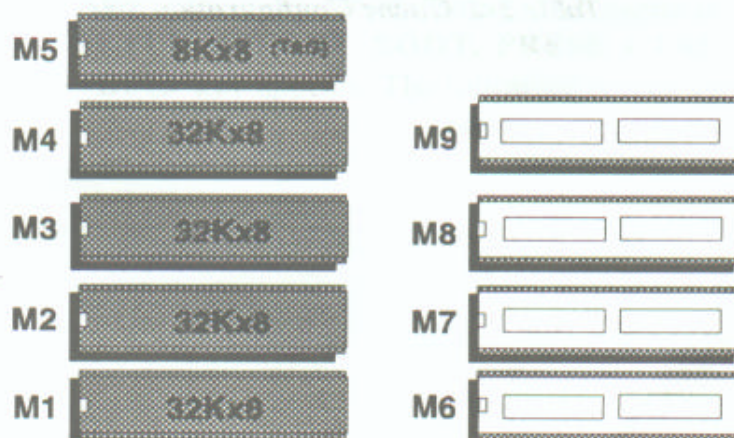
5. Press the chip completely into the socket so that the pins are properly seated.

## Cache SRAM Specifications and Settings

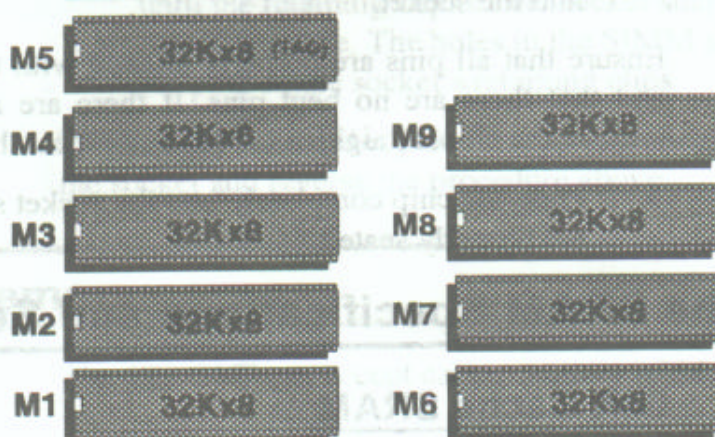
### 64K Cache SRAM



### 128K Cache SRAM





**256K Cache SRAM**

The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

*Table 3-2. Cache Configuration Size*